

SMART POWER

APPLICATION MANUAL

1st EDITION

JUNE 1989

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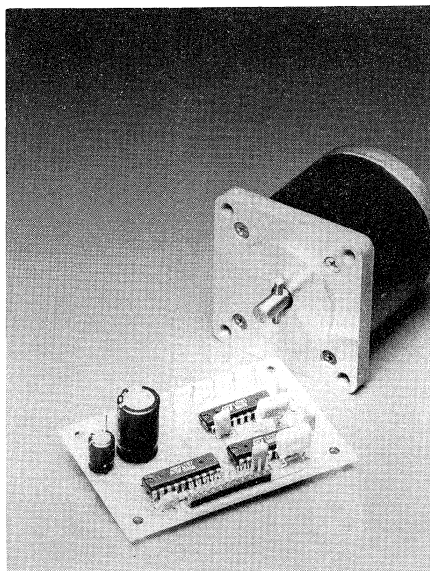
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SGS-THOMSON MICROELECTRONICS SMART POWER: THE BRIGHTEST TECHNOLOGY, THE BRIGHTEST SUPPORT

SGS-THOMSON was making smart power ICs even before the name was coined and has long been recognized the technology leader in this field. Today leading market research companies also name SGS-THOMSON as the leader in smart power sales.

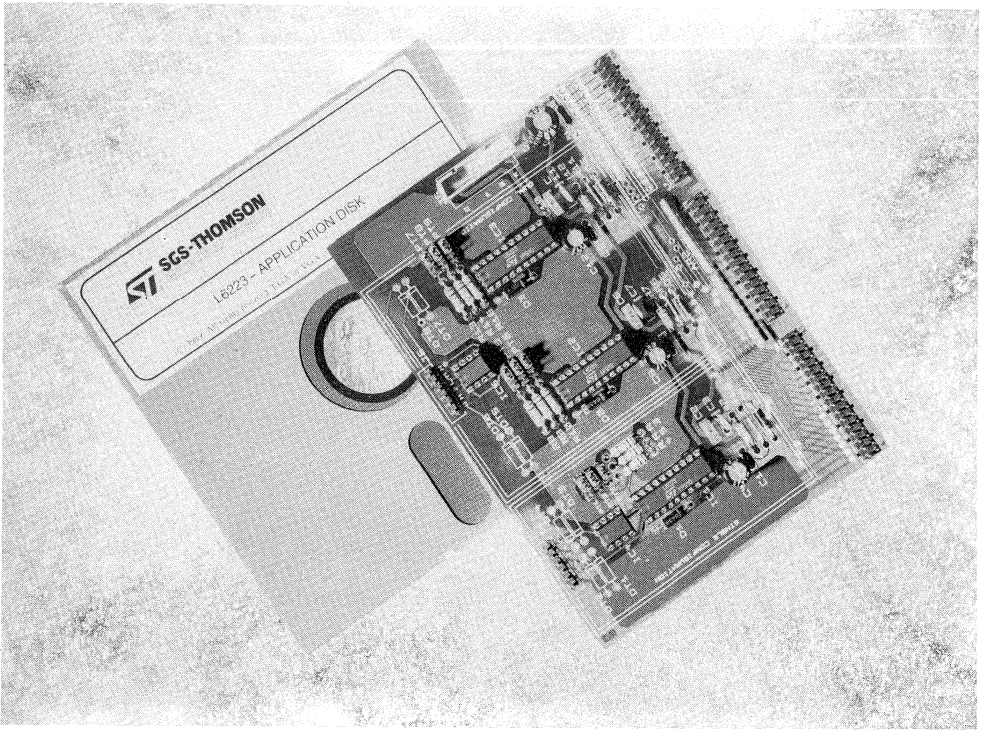


The brightest technology. SGS-THOMSON's unrivalled smart power product range includes ICs like the L6202 DMOS H-bridge motor driver. In this application two L6202s drive a bipolar stepper motor. Because these ICs have a very high conversion efficiency no heatsink is needed.

Many of the standards in this young market began as SGS-THOMSON innovations: products like the L293 and L298 dual H-bridge motor drivers, packages like the Multiwatt and Powerdip. But continued innovation keeps the company always one step ahead. While other companies strive to match recent introductions like the L6202 DMOS H-bridge motor driver SGS-THOMSON is ready to deliver new, smarter ICs like the L6223 unipolar stepper motor driver.

Commitment to staying ahead implies also a commitment to support; you won't find textbooks very helpful in applying the latest products. SGS-THOMSON demonstrates this commitment with support engineers in every semiconductor market, with software and hardware that turns your IBM PC into a Smart Power Development System and, of course, books like this Smart Power Application Manual.

Contact your nearest SGS-THOMSON office if you'd like an engineer to come and discuss your application. You can count on us to provide support that's as good as the product.



The Brightest support. Testing and optimizing applications for complex smart power chips need no longer be a headache. SGS-THOMSON provides special hardware and software that turns your PC into a Smart Power Development

Note: Datasheets for the products described in this manual are included in the SGS-THOMSON Industrial & Computer Peripheral ICs databook: (ORDER CODE: DBINDCOMPST/1)

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TECHNOLOGY AND BASICS

NEW DEVELOPMENTS IN INTELLIGENT POWER TECHNOLOGY

Recent developments in power IC technology greatly expand the capabilities of integrated circuits combining control circuits and high power drive stages. This note describes the new power processes, new packages and the latest generation of power ICs.

While chips integrating both signal and power elements have been with us for several years, recent developments have greatly expanded the capabilities of these technologies. With the latest processes designers can integrate many circuits that were previously uneconomic or simply impossible. Moreover, the enlarged horizons of intelligent power technology - and packaging - are prompting new trends in the partitioning of systems.

Not only are intelligent power ICs becoming more common, they are also becoming more intelligent, to the point where designers can aim to integrate a complete power subsystem. Moreover, the current and voltage capabilities of these technologies have increased dramatically, enlarging the field of applications.

Since system designers are often responsible for partitioning electronic systems and specifying new devices it is important for them to understand the capabilities of the latest technologies. This is now more true than ever, both because IC technology has advanced so rapidly and because the latest generation of power ICs have a much greater 'system' content.

THE NEW TECHNOLOGIES

Intelligent power technologies have evolved from two earlier species : linear IC technology and discrete transistor technology.

Processes of the first type are enhancements of the basic planar IC structure where all of the connections are on the top surface of the chip. In contrast, those intelligent power technologies that have been developed from discrete transistor processes have a collector, or drain, contact on the lower surface of the die. A fundamental consequence of this structural difference is that with processes of the first type it is possible to integrate any number of isolated power transistors and interconnect them in any configuration. SGS-THOMSON Microelectronics calls these Multipower processes.

Where a bottom contact is used it is only possible to integrate a single power transistor, or several with

common collectors (or drains), therefore configurations such as the H-bridge cannot be integrated but higher current and voltage capability of several hundred volts is possible. SGS-THOMSON has named this type of process VIPower™ (Vertical Intelligent Power). Both technologies can be further subdivided into those which are pure bipolar and mixed technologies containing a mixture of bipolar and MOS structures. In both fields significant progress has been made recently.

PURE BIPOLAR MULTIPOWER PROCESSES

Just how far bipolar technology has advanced is illustrated by SGS-THOMSON' new Multipower-S² P² and Multipower-HDS² P² processes.

Multipower-S² P² (figure 1) is a 60V process that integrates bipolar linear, IIL logic, NPN and PNP power transistors and a new low leakage diode structure.

One of the most important characteristics of this process is that it offers a new Isolated-Collector Vertical PNP (ICV PNP) structure which is much closer to discrete PNP transistors in performance terms than the usual lateral PNP type. These ICV PNP transistors provide, in fact, a current density of 0.8 A/mm² at V_{sat} = 1 V - compared to 2 A/mm² for NPN types - and a cutoff frequency of 20 to 30 MHz.

The possibility of integrating high performance power PNP transistors on an intelligent power IC allows designers to choose any output configuration. Moreover, the ICV PNPs low voltage drop can be exploited for applications where drop-out is a critical parameter. Another advantage, specifically for automotive applications, is that an ICV PNP output stage can withstand battery reversal indefinitely.

Another important feature of Multipower-S² P² is the inclusion of a new low leakage diode structure that has a parasitic PNP gain about four orders of magnitude lower than conventional structures. This new structure is ideal for the recirculation diodes in high power ICs driving inductive loads such as motors and solenoids.

Figure 1 : Multipower-S²P², a 60V Bipolar Process, Combines Linear, IIL Logic, ICV PNP Power Transistors and Low Leakage Diodes.

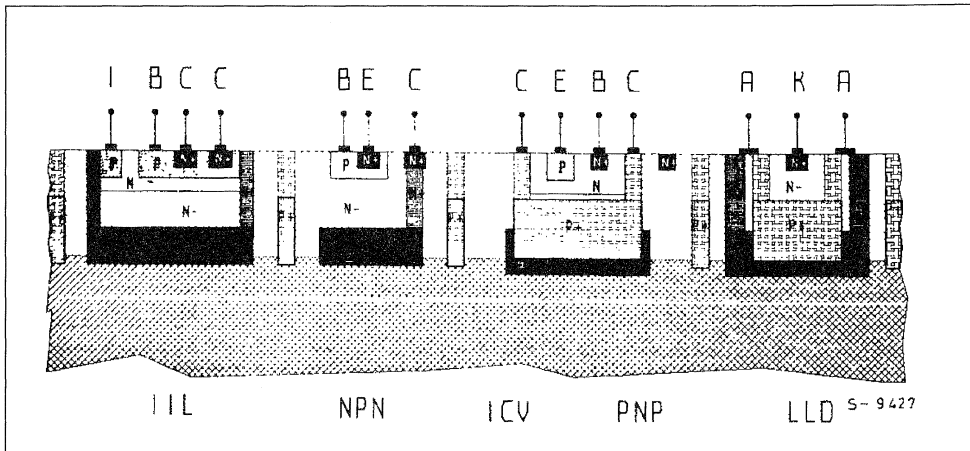
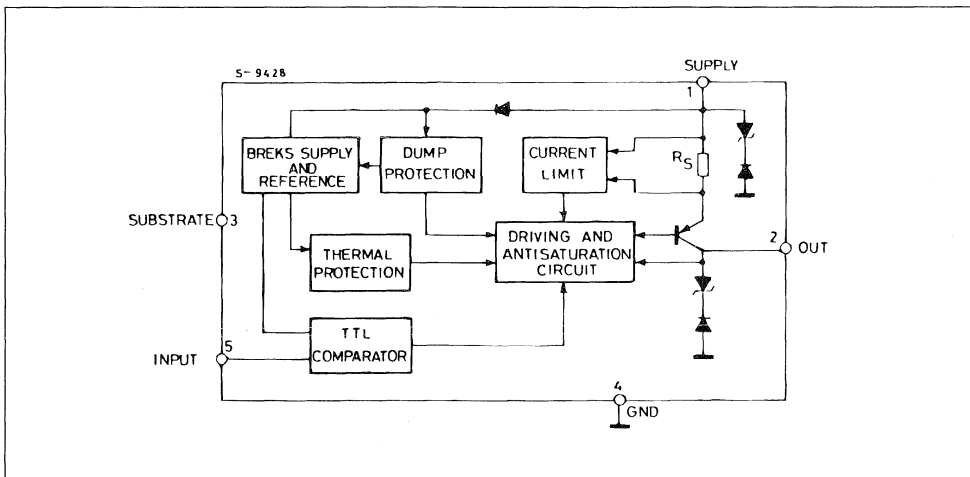


Figure 2 : Designed Primarily for Automotive Applications, the L9350 High Side Solenoid Driver Exploits Multipower-S²P²'s ICV PNP Structure to Obtain Very Low Saturation Voltage.



The first device to be produced with this process is a relatively simple high side driver, the L9350, originally designed to the specification of a customer in the automotive electronics market (figure 2). An ICV PNP output transistor is used in this device to obtain very low saturation, high gain (about 30 with 1A output current) and the ability to withstand load dump transients.

Another device realized with this technology is a single-chip alternator regulator (figure 3) which integrates for the first time all of the power and signal

devices needed to regulate the output voltage of a car alternator. Perhaps the most interesting aspect of this IC is that it needs no external components. Multipower-HDS² P³ (figure 4) is a similar pure bipolar process. Like Multipower-S² P² it integrates linear, IIL, LLD and ICV PNP structures. In addition it also offers ECL logic.

But the most important characteristic of this process is high density. Dimensioned for 20V capability, it is aimed at low voltage applications where more complex signal processing circuits are needed - up to

270 IIL gates can be shoehorned into one square millimeter of silicon.

Multipower-HDS²P² is also characterized by an exceptionally high current density : 6A/mm² for NPN transistors ; 2A/mm² for PNP (at $V_{sat} = 1V$ and $H_{fe} = 10$).

This process has been applied to produce a custom stepper motor control/drive chip, where the high density of the process allows translator and chopper circuits to be integrated economically on the power drive chip. It is also used for a new 1.5A voltage regulator, the L4940, where the ICV PNP provides very low voltage drop and low quiescent current.

Figure 3 : Another Multipower-S²P² design, the L9480 Alternator Regulator is a Circuit which Needs no External Components.

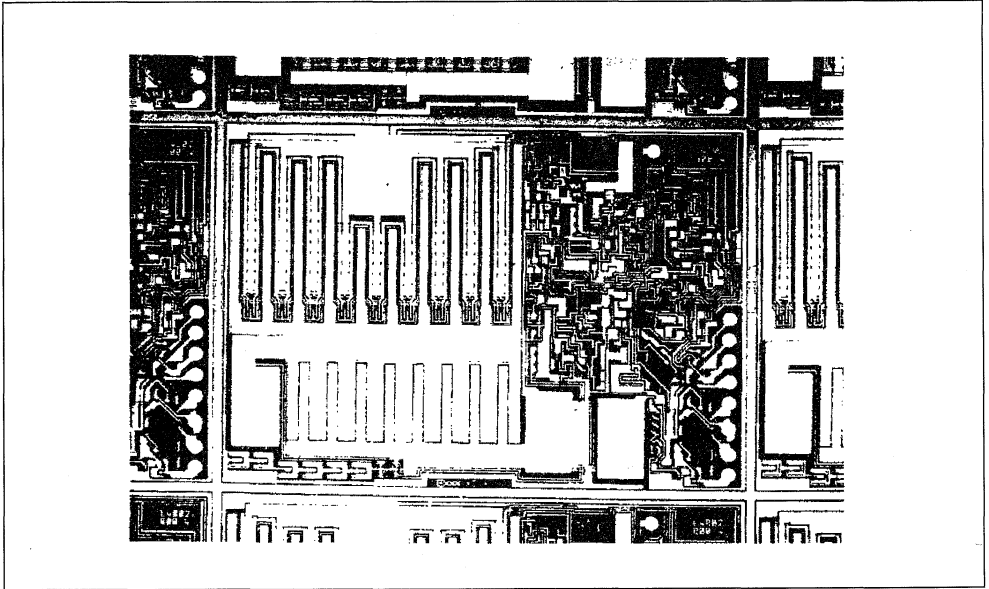
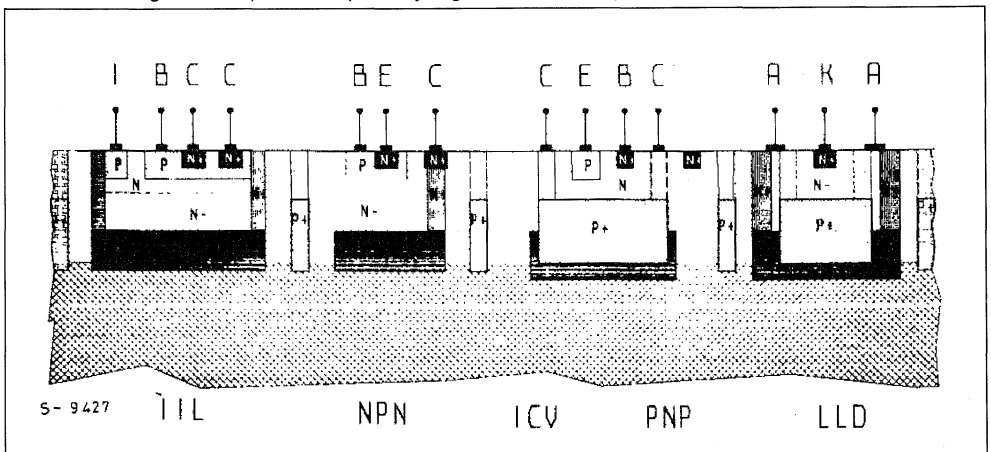


Figure 4 : Multipower HDS²P² is a 20V Process Characterized by Very High Density in the Signal Part (270 IIL gates/mm²) and exceptionally High Current Density.



MIXED MULTIPOWER TECHNOLOGY

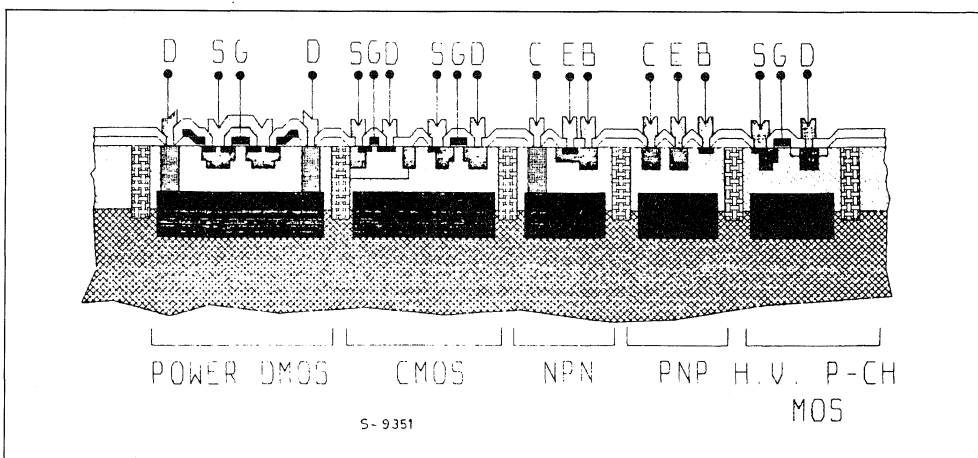
Another area where remarkable progress has been made is in mixed bipolar/MOS technology. Though several mixed technologies of the 'vertical' type are available, a much more significant development is SGS-THOMSON' Multipower-BCD process (figure 5), which combines linear, CMOS logic and DMOS power transistors without placing any limit on the number and connection of the power devices.

Thanks to the DMOS power transistors this process allows efficiencies above 95 % and switching frequencies up to 500 kHz. In addition, there are no secondary breakdown limitations, paralleling of devices is simpler and there is an intrinsic 'fast' recirculation diode in the power DMOS structure which is adequate for most applications.

For intelligent power devices the very high efficiency of power DMOS is an important advantage. The power output of a chip is limited by the maximum dissipation allowed in the package. By reducing dissipation in the chip it is possible to put power ICs in low cost packages with modest power handling capability. Alternatively, packaged in existing high power packages, DMOS chips can deliver hitherto unreachable power levels.

Moreover, the saturation loss of a power DMOS transistor can be reduced by increasing the area. Designers therefore have the possibility of trading costly copper and aluminum, materials used in packages and heatsinks, for silicon, which tends to decrease in cost as wafer fabrication techniques are improved and automated.

Figure 5 : A Mixed technology, Multipower-BCD Integrates Linear, CMOS Logic and Power DMOS Devices on the Same Chip. Unlike Other Mixed Technologies it Places no Limit on the Number or Connection of the Power Transistors.



Another important way in which Multipower-BCD differs from pure bipolar technologies is that it allows the mixing of low voltage and medium voltage elements on the same chip : lateral DMOS transistors with a breakdown voltage of 60V can be produced in an epitaxial layer dimensioned for 20V linear and CMOS circuits.

The first product to be developed using this process is the L6202 motor driver (figure 6) which uses four DMOS power transistors in a H-bridge output stage.

Assembled in a powerdip package this device can deliver 1.5A at 54V with no external heatsink. In the photograph, figure 7, the four DMOS power transistors can be clearly seen in the lower part of the die.

VERTICAL PROCESSES

While the "Multipower" processes are more versatile SGS-THOMSON is also developing bipolar and mixed vertical technologies, called VIPower-M1 and VIPower-M2.

VIPower-M1 (figure 8) combines 400V NPN power transistors and bipolar low voltage (up to 30V V_{ce0}) drive circuits, while VIPower-M2 (figure 9) will offer 80V DMOS power transistors and mixed CMOS/bipolar drive circuits.

Though these processes cannot be used for devices with bridge and half-bridge output stages, they offer higher voltage capability and VIPower-M2 features a lower ON resistance than Multipower-BCD.

VIPower-M2 is suitable for applications such as high current high side drivers and DC-DC converters

Figure 6 : A Motor Driver Chip, the L6202, is the First Product to be realized with the Multipower-BCD process. The DMOS H-Bridge Output of This Chip Delivers 1.5A at 54V but Thanks to the high Efficiency no Heatsink is Needed.

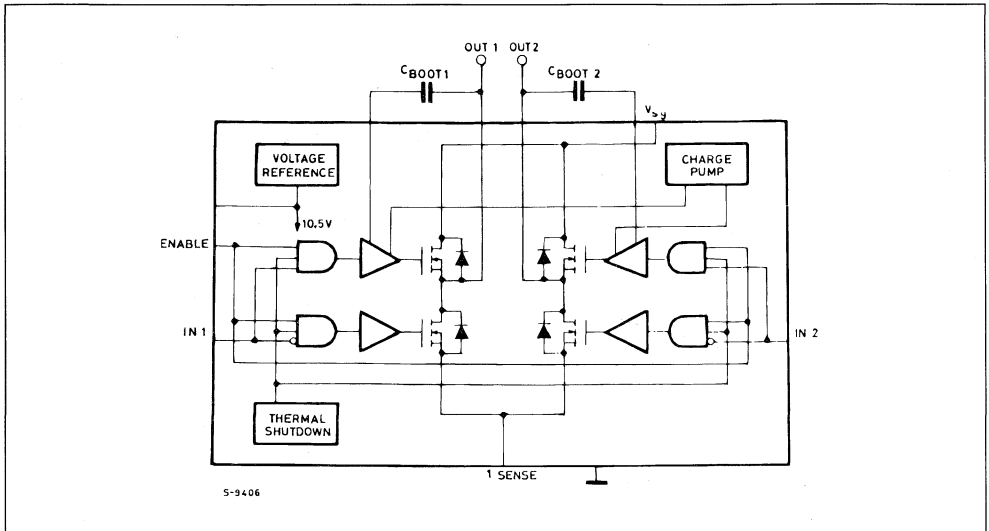
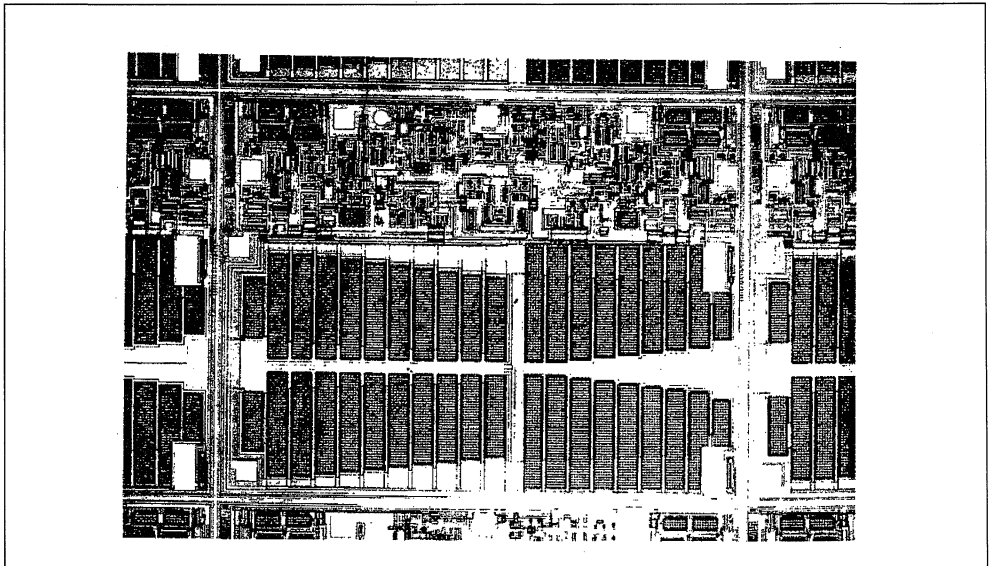


Figure 7 : The Four DMOS Power Transistors Occupy about 2/3 of the L6202 Die.



while VIPower-M1 is suitable for applications like high voltage solenoid drivers, motor drives and off-line power supplies.

The first products proposed in VIPower-M1 are 400V 5A to 10A NPN darlington switches (figure 10) with direct logic compatible drive. In addition on chip

thermal, overcurrent and overvoltage sensing can shutdown the power switch and provide a diagnostic output to inform the system microprocessor of the overload condition.

CHOOSING THE RIGHT PROCESS

The choice of process depends on the output stage configuration, current, voltage and the complexity of the signal processing section.

Mixed bipolar/DMOS is the best for lower current devices where the signal processing circuitry is very complex. Pure bipolar processes, in contrast, are better for low voltage, high current applications because the current density is much greater. However future developments of Multipower-BCD are likely to erode this advantage in a few years.

One area where mixed technology will not replace pure bipolar processes completely is automotive electronics. This is because of the high energy load dump transients which occur on the battery rail.

To withstand these transients a DMOS technology must have a BV_{dss} breakdown voltage greater than the peak dump voltage, while a bipolar NPN transistor can be turned off to take advantage of the BV_{cbo} breakdown voltage, which is much greater than the BV_{ceo} breakdown voltage.

Mixed bipolar/DMOS technology will become increasingly important in very complex power devices. In the near future the Multipower-BCD process will be applied to produce specialized peripheral drivers,

optimized for one load type. Multipower-BCD is ideal for these applications because it offers high precision bipolar linear circuits (for signal conditioning etc), high density CMOS (for complex logic) and high efficiency DMOS (for the power stage).

POWER PACKAGE DEVELOPMENTS

For a power IC the package is extremely important, since it determines both the power capability and the cost.

At present SGS-THOMSON assembles most high power ICs of the Multipower type in power-tab packages like the Pentawatt, Heptawatt and Multiwatt® (which are attached to a heatsink), or in special DIP packages with a leadframe designed to reduce thermal resistance. All of these packages are 'insertion' types. However, several trends have now emerged which call for the design of completely new power packages.

Firstly, the increasingly widespread use of surface mounting techniques and automatic assembly has brought the need for surface mounting power packages. For medium power (up to 2W) one solution, which SGS-THOMSON already has in production, is a plastic chip carrier with a special leadframe.

Derived from the 44-lead PCC, this package uses 33 leads for connections and the other 11 leads to transfer heat to the substrate (figure 11). This package has a junction-case thermal resistance of less than 7°C/W, allowing dissipation up to 2W.

Figure 8 : VI power-M1 Technology integrates 400V NPN Power Transistors and 30V Drive Circuitry.

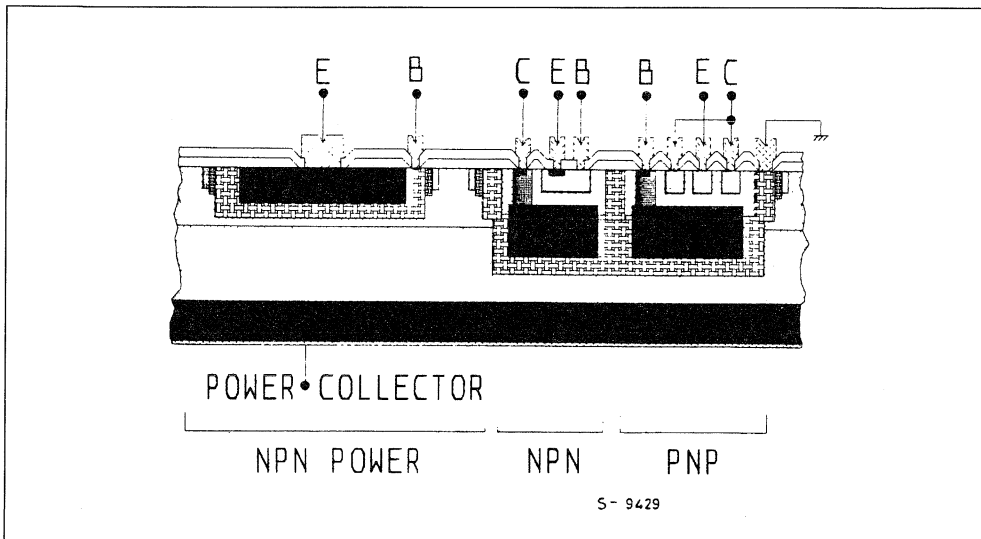


Figure 9 : Another "vertical" Power Process, VIPower-M2 Combines 80V DMOS Power Transistors and Mixed CMOS/bipolar Drive Circuits.

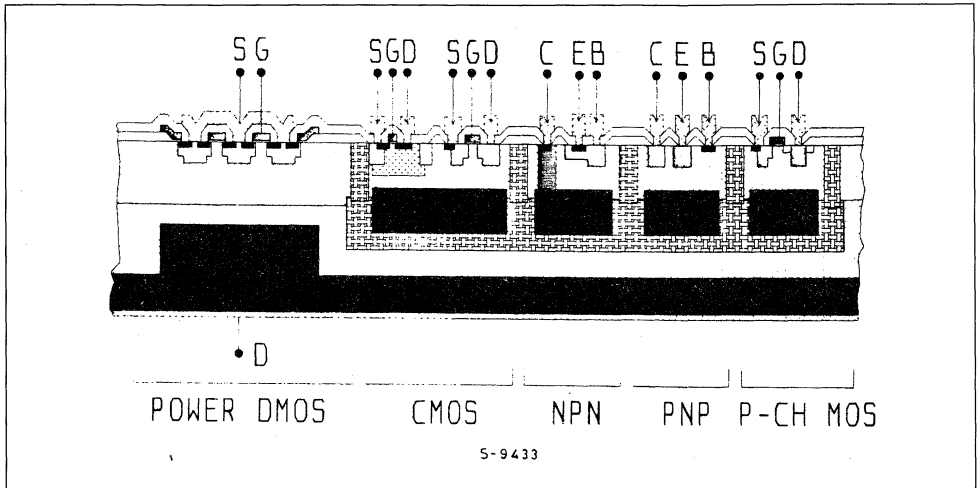
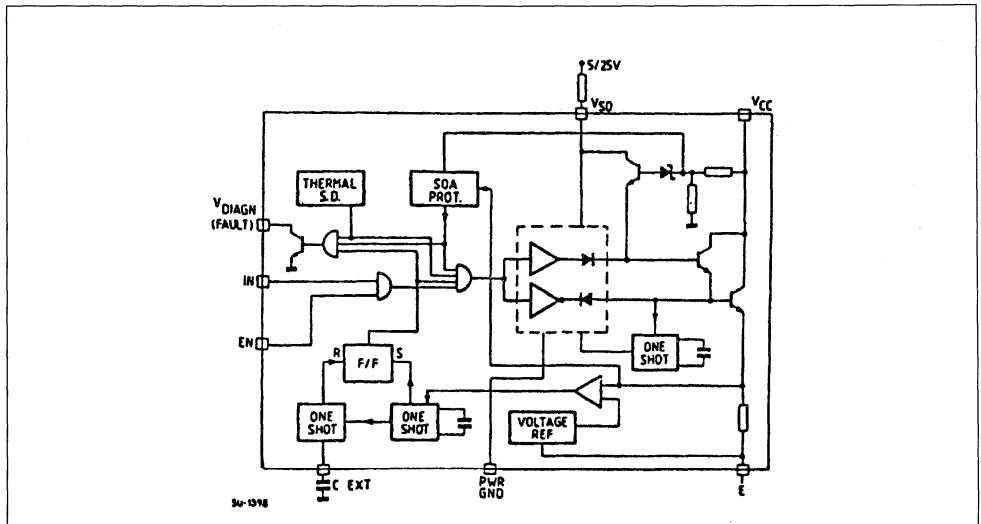


Figure 10 : VI Power-M1 will be used to produce a 400V/10A NPN Darlington Switch Which Connects Directly to Standard Logic.



For higher power devices development is concentrated on a new generation of packages. One package family being studied (figure 12) has a junction-case thermal resistance of less than 5°C/W , 3-17 pins and a lead spacing of 50 mils. These packages will have an SO-width body and gull-wing leads, allowing the use of SO package handling

equipment. The low thermal resistance of these packages is obtained by a copper heat spreader on the lower surface of the package. When the package is soldered in place the spreader is in contact with the substrate. Clearly the amount of power that can be dissipated in the device depends on the conductivity of the substrate.

Figure 11 : The Leadframe of a Plastic Chip Carrier can be Modified to Reduce Thermal Resistance. This '33 + 11' Lead Configuration Allows Power Dissipation up to 2W.

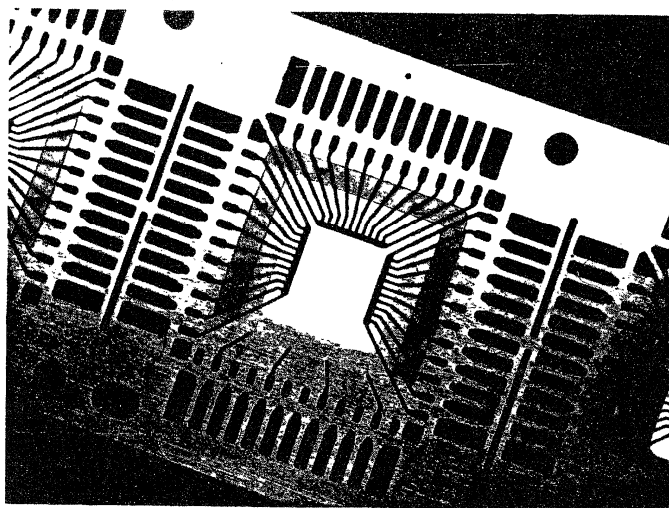
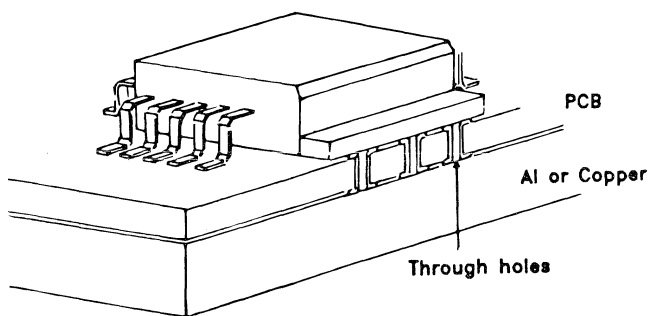


Figure 12 : For Power Dissipation above 2W New Surface Mounting Packages are being Developed. This Type, Compatible with SO-package Handling Equipment, has a thermal Resistance of About 5 °C/W.



In view of this trend there is now considerable interest in high conductivity substrates and the various alternatives, such as a plastic board bonded to an aluminum or copper sheet. Plated-through holes in the PCB reduce the thermal resistance between the package and the metal sheet.

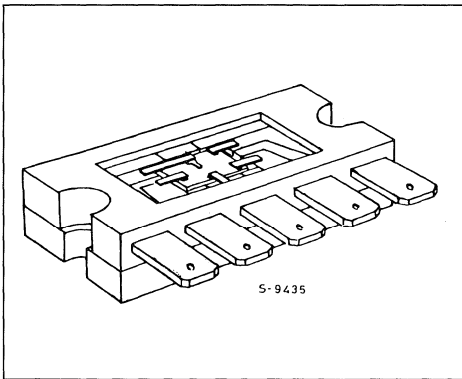
Another development area is the inclusion of a copper heat spreader on the under-side of plastic chip carriers. These power chip carriers will, like many new packages, be pre-molded types, which eliminates stress on the die caused by polymerization shrinkage of the molding resin.

New packaging concepts are being studied for chips like the L9480 which need no external components. Since there is no need to mount such devices on a substrate they will probably be assembled in packages designed to be bolted to the load (figure 13) and equipped with 'Faston'-type connectors.

ISOLATED PACKAGES

ICs produced using VIPower™ technology pose a different problem because the lower surface of the die is the collector (or drain) contact and because greater heat dissipation capability is needed. For

Figure 13 : New Packaging Concepts are being Studied for 'Silicon-only' Circuits where there is no Point in Mounting the Device on a Conventional Substrate because there are no other Components needed.



these ICs SGS-THOMSON Microelectronics is developing multi-lead versions of the ISOWATT-218™ plastic package (figure 14) where a copper frame is completely surrounded by molding resin - even on the lower surface - to provide electrical isolation. Low thermal resistance is assured by the thickness and high thermal conductivity of the resin.

One of the new packages in development is shown in figure 15. This packages will achieve better than 2.5°C/W thermal resistance and 2500V AC isolation.

Figure 14 : In the ISOWATT-218 Package the Copper Frame is Completely Surrounded by Molding Resin to Isolate the Device from the Heatsink.

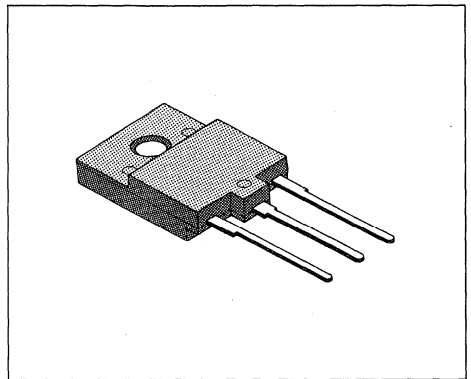
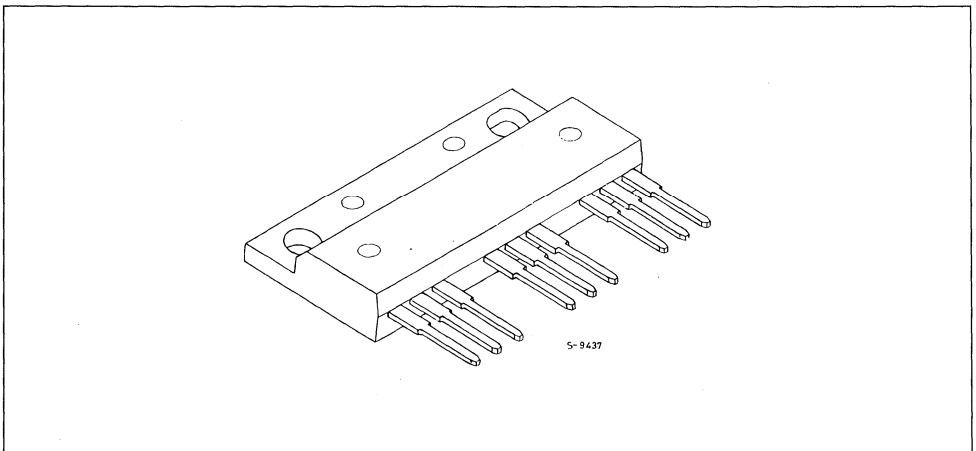


Figure 15 : Isolated Packages with Higher Pin Counts are in Development.



REDUCED DISSIPATION IN POWER ICs ENHANCES RELIABILITY, CUTS COSTS

By Carlo Cini & Andrea Cuomo

High power integrated circuits were originally limited by technological constraint. The current density that could be obtained in an integrated power transistor was fairly low, the complexity of the control part was limited -- to about 50 transistors -- and satisfactory yields could only be obtained with what would today be called small die sizes (5000 square mils).

But in the late seventies and early eighties power IC technology developed rapidly, overcoming these limitations. The most serious limitation then became the power dissipation capability of the package and, if one is used, the heatsink.

Clearly higher power could be achieved by developing packages with lower thermal resistance. However, such packages are relatively expensive. Development in this direction has, in fact, stopped at around the 3° C/W level achieved by the Multiwatt 15-lead power IC package. Though other packages with lower IC package. Though other packages with lower thermal resistance exist they either have small pin counts or they are too costly for high volume applications.

Heatsinks, too, pose a problem. Automatic assembly is gaining ground rapidly so designers are increasingly avoiding any parts which need to be added manually. Moreover, a heatsink occupies valuable space and it costs money.

THE COOL ALTERNATIVE

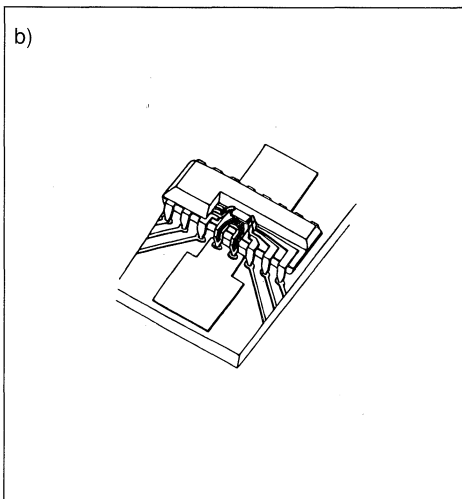
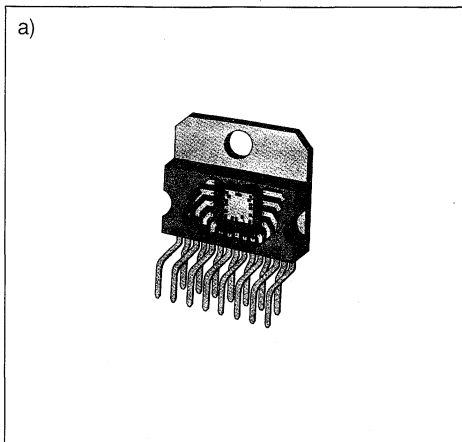
An alternative solution is to approach the problem from another direction : rather than develop packages to cope with higher dissipation, why not reduce the dissipation ?

This approach has many advantages. By reducing dissipation in an IC it is possible to obtain more output power without using a more costly package. Alternatively, the same power can be obtained with a less expensive and more convenient DIP package, which can be automatically inserted (figure 1).

Lower dissipation also means cooler running, which enhances reliability -- a benefit now greatly in demand.

Even the low-power control section of a power IC benefits from reduced dissipation. Firstly, if the

Figure 1 : By reducing the dissipation in a power IC it is possible to obtain more power from power packages like the Multiwatt (a) ; alternatively, chips can be packaged in the less expensive powerdip packages (b), which are more convenient for automatic assembly.



power section runs cooler thermal effects in the chip are reduced. In addition, if the control section itself dissipates little power it can be made much more complex without causing dissipation problems.

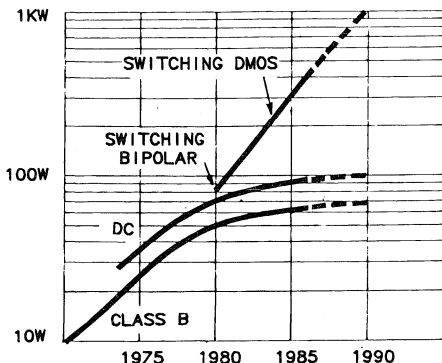
Low dissipation in high power integrated circuits is obtained in several ways: the use of switching techniques, increasing the switching speed, transistors with a low saturation voltage and -- the shape of things to come -- mixed technology devices with DMOS power Transistors.

SWITCHING TECHNIQUES

The introduction of switch mode power ICs was responsible for a sudden increase in IC power capability at the beginning of the eighties (figure 2) and today it is very common in fields such as motor control ICs. Though these ICs are generally more complex than purely linear ICs the advantage of switching operation is evident: today linear power ICs in the Multiwatt package, capable of dissipating 20-25W, can deliver up to about 40W to the load. Switching power ICs in the same package deliver up to 250W.

In switch mode power ICs dissipation can be reduced by technology improvements which cut the transistor turn-on/off times. This is because the dissipation depends on the ratio of these switching times to the repetition period of the circuit. Reduction in switching times has become a more important aim today because designers prefer to operate at high switching frequencies to reduce the size and cost of filter components.

Figure 2 : The power output available from commercial power ICs increased dramatically when switching techniques were introduced; now the use of technologies with DMOS power transistors are bringing another rapid increase.



LOWER SATURATION

Reducing the saturation voltage of power transistors in another way to reduce the power dissipated in an IC.

Low saturation can be obtained with standard integrated NPN power transistors, though the lowest is achieved with PNP transistors. But the lateral power PNP structure normally used in integrated circuits has a low gain (typically 3-10 at high current), so the power dissipated as a result of the high base drive current offsets the reduction gained by having a low saturation voltage.

Recent developments in bipolar IC technology, however, have overcome the limitation. In a new-generation process called Multipower-HDS2P2 (figure 3) a vertical PNP structure with high gain is used. This structure gives performance much closer to that of power NPN transistors, allowing a very low saturation voltage, low base current and a current density one third of that of an NPN transistor. A solenoid driver IC developed using this technology has a saturation voltage of only 0.7V at 1A output current.

THE FUTURE LIES IN DMOS

The trend for the 1990's, however, will be the application of embryonic mixed technologies combining DMOS power transistors with bipolar/CMOS control circuits to achieve extremely low power dissipation (figure 4).

From a power IC designers point of view DMOS power stages have several important advantages. They need no driving power in DC conditions, they dissipate little power, there is an intrinsic recirculation diode in the DMOS structure and there are no second breakdown limitations. Moreover, DMOS power transistors can be paralleled without limit and it is possible to 'buy' low on resistance by increasing the silicon area.

Dissipation is so low in DMOS power stages that high power packages will only be needed for ICs delivering power levels are yet never reached and heat-sinks will simply disappear in most applications.

Already mixed Bipolar-CMOS-DMOS technology is sufficiently advanced to allow a direct comparison between practical circuits based on the old and new approaches. Figure 5 shows a conventional circuit used in a typewriter to drive two bipolar stepper motors. Two bipolar dual bridge ICs in the Multiwatt package are used and a heatsink is needed. Figure 6, in contrast, shows the same circuit redesigned using four DMOS bridge driver ICs. Though

Figure 3 : SGS THOMSON Multipower-HDS2P2 technology represents the current state of the art in pure bipolar technology. This process features a new vertical PNP power transistor structure which combines the low saturation voltage of PNP transistors with performance close to that of NPN power transistors.

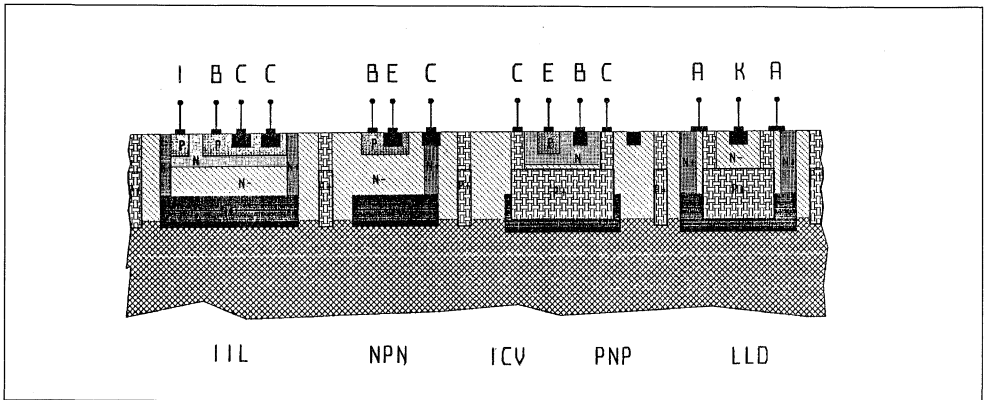
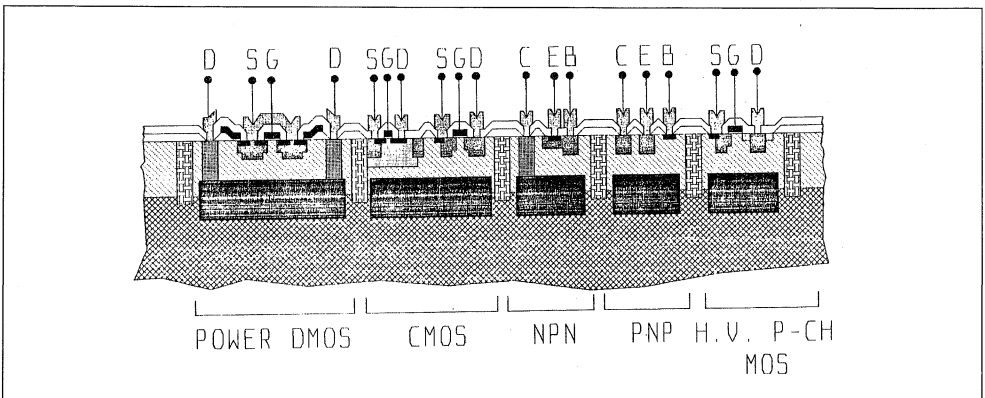


Figure 4 : The shape of things to come : In the 1990's mixed technologies like Multipower-BCD, combining bipolar, CMOS and power DMOS, will dominate the power IC field. The extremely low dissipation of DMOS power stages will change the approach to system partitioning and packaging.



the DMOS bridge driver ICs. Through the DMOS bridge driver ICs cost more (at present) an overall saving is possible because :

- Recirculation diodes are intrinsic in the DMOS structure -- and they are 'free', occupying no silicon area -- the 16 external diodes are not needed on the DMOS version.
- No heatsink is needed for the DMOS version, saving the cost of the heatsink itself and a manual assembly step.
- The DMOS bridge ICs are assembled in DIP packages, which are inexpensive and easy to handle.
- For the same output power, 16W less is drawn from the supply so the supply cost, size and weight are all reduced.
- The charge pump technique allows the upper N channel DMOS transistor to be driven as like a p-channel transistor (i.e. with TTL levels), reducing size and complexity (figure 7).

Figure 5 : This circuit based on two bipolar dual bridge chips drives two bipolar stepper motors in an electronic typewriter.

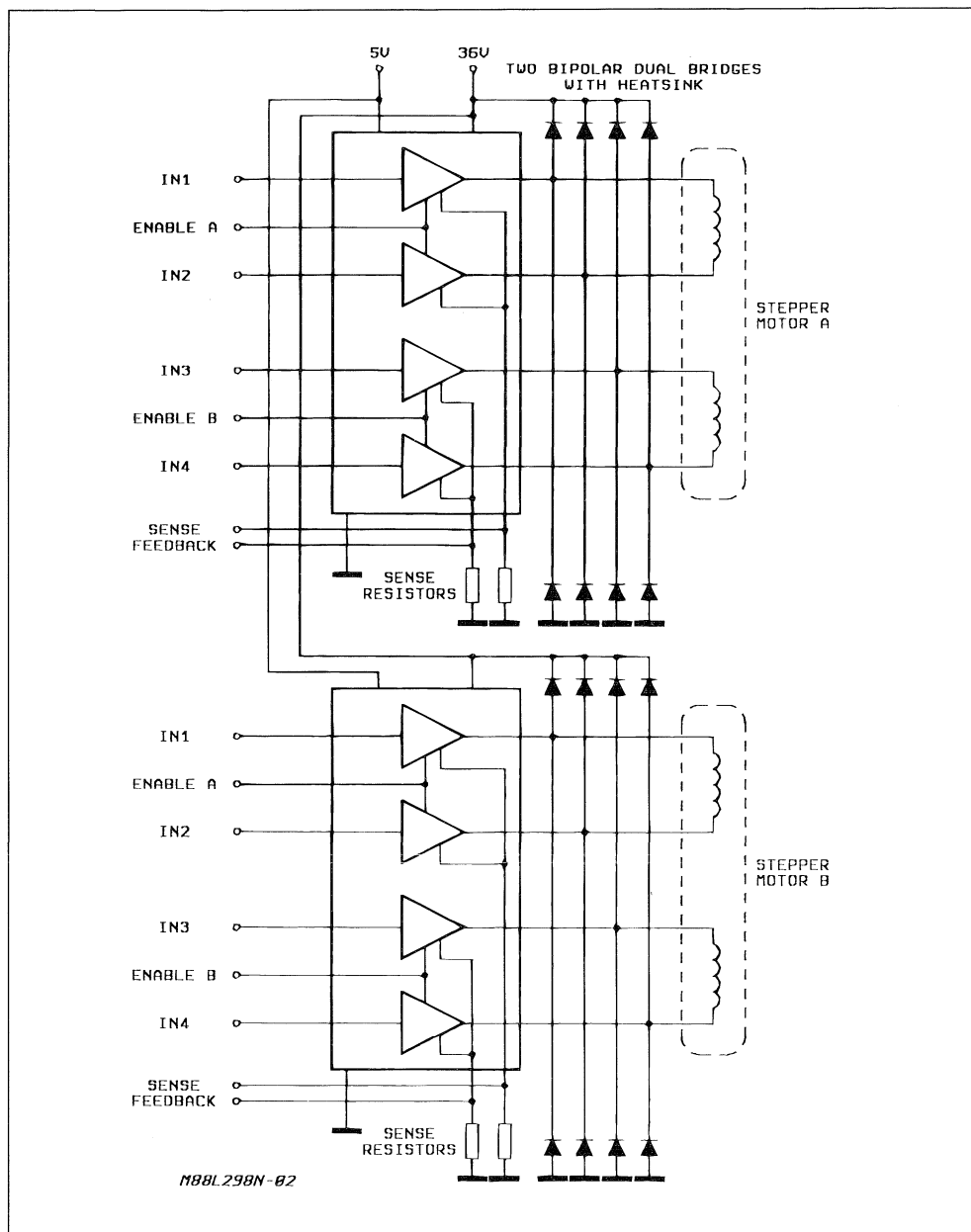


Figure 6 : The figure 5 circuit is now being replaced by this version, based on four DMOS bridge ICs. This version needs no heatsink and uses DIP packages rather than the high power Multiwatt package, reducing the overall cost.

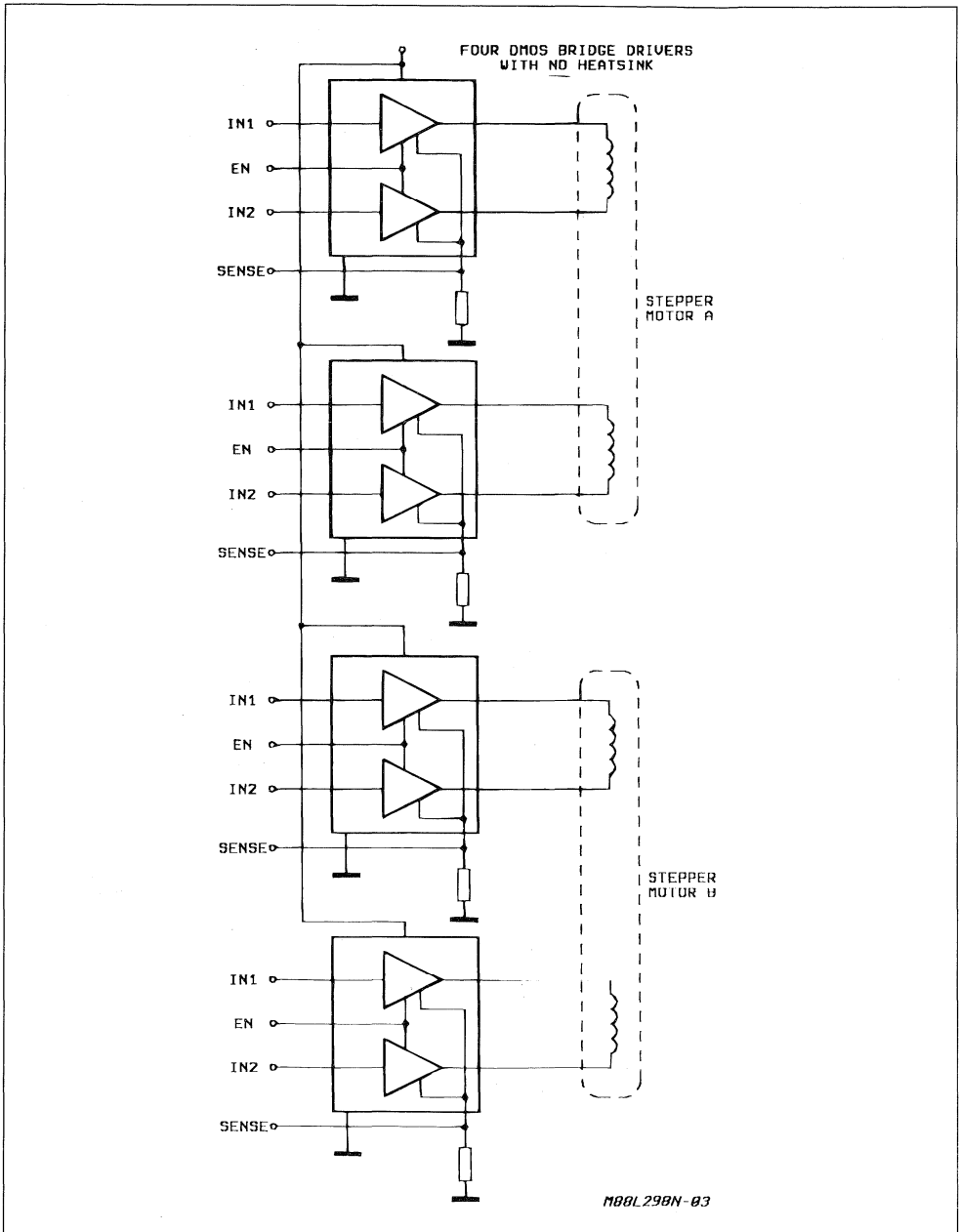
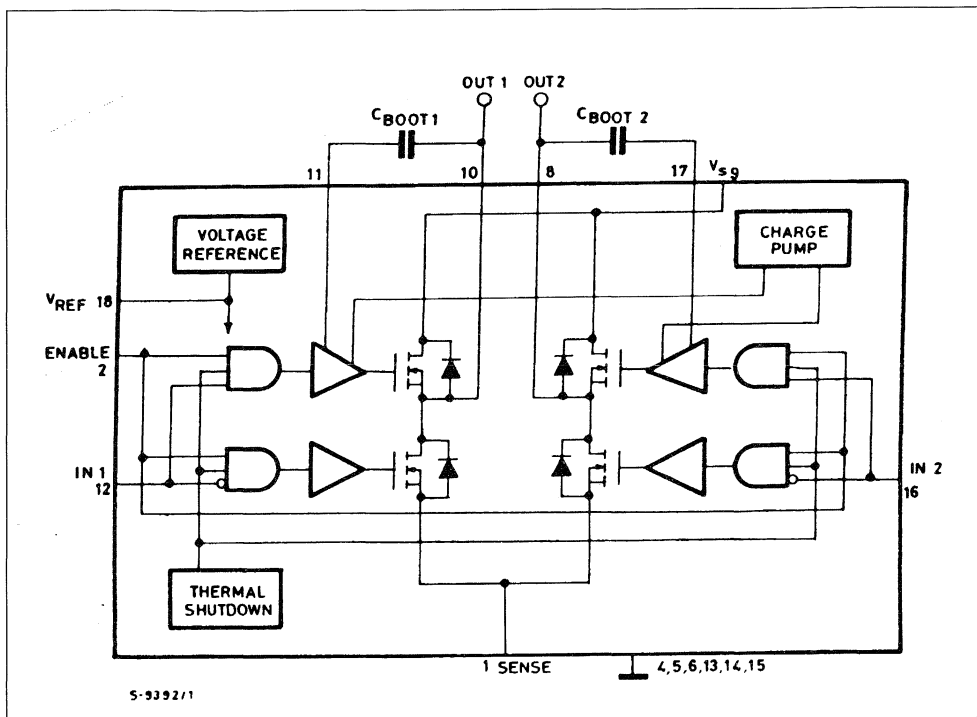


Figure 7 : The DMOS bridge IC used in the figure 6 circuit includes four high current DMOS transistors plus driving circuits and a charge pump which allows the upper N-channel DMOS transistors to be driven like P-channel devices.



The DMOS bridge IC in this example illustrates two important trends for the second half of the eighties. Firstly, DIP packages will become the most common type for power ICs delivering up to about 2A output current. Second, heatsinks will disappear very rapidly in applications requiring currents of this magnitude.

Looking further ahead, in the 1990's mixed technologies will have developed to the point where very complex control circuits (1000+ gates) and power stages with a very high current density (0.05ohms) can be integrated on the same chip. The limits to power circuit complexity imposed by dissipation and silicon area will be greatly expanded. It will, in fact, be feasible -- technically and economically -- to integrate multiple power and all the necessary control circuits on one chip, bringing power ICs into the realm of true LSI.

Another important trend will be the move towards "cold" chassis which, using CMOS and power DMOS ICs all operating at temperatures close to ambient temperature. Since the reliability of semiconductor devices -- and other parts of the chassis -- is inversely proportional to the operating temperature this will bring a significant improvement in reliability.

Finally, the advent of ultra-low dissipation power ICs has coincided with the large-scale adoption of surface mounting. Using conventional power IC packages surface mounting is impractical so the assembly process is complicated by manual steps. To take full advantage of reduced dissipation a new generation of surface mountable power packages with modest thermal performance will emerge in the next few years.

POWER IC's PROMISE GREATER SYSTEM RELIABILITY

F. Longo, M. Pesce & I. Wilson

INTRODUCTION

This article discusses an intelligent power switch that, using VIPower™ technology, includes in the same chip a 400V-7A power darlington and a low voltage circuit that provides protection and diagnostic features, as well as the driver for the power stage. The circuit operation is explained and the advantages in terms of reliability and cost reduction are explained. An open-loop, single switch, motor drive circuit is shown as the basis from which typical power supply applications may be developed.

A power transistor used in a switching application needs external circuitry to be driven in normal operation and protected when a fault condition occurs. In many applications power transistor failures are caused by external influences ; the major problem is that often these failures result in device short circuits, which cause failure of surrounding components. Some, such as resistors, may temporarily flame until fuses open circuit or the resistors burn out. At the same time, PCB's are irreparably dama-

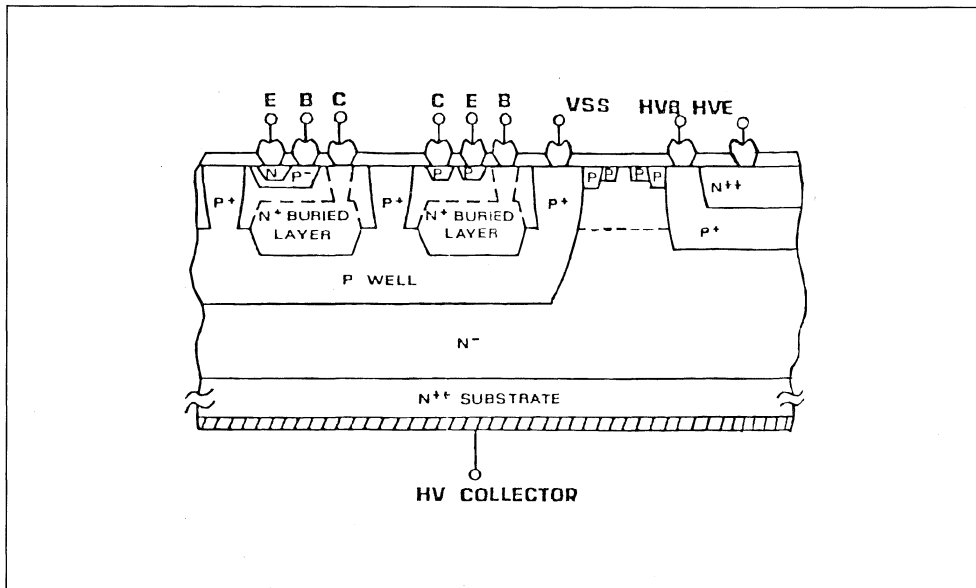
ged. To provide adequate external protection circuitry is too expensive to be practical for many applications. VIPower (Vertical Integrated Power) technology makes it possible to integrate the power stage and the control circuit, which may include driver, protection and diagnostic output in a single chip. This technique has been used to make VIPower IC's that are reliable, easy to use and capable of handling switchable power over 2kW.

DESCRIPTION OF TECHNOLOGY

VIPower technology involves the fabrication of a low voltage integrated circuit inside a p-type well, on the same n-type substrate as a vertical current npn power transistor. The p-type well must be connected with the most negative point of the supply.

This reverse-biased, p-type well/n-type substrate junction isolates the low voltage section from the high voltage collector. Fig. 1 shows a cross section of the structure.

Figure 1 : VIPower Structure Cross Section.



DEVICE FEATURES

Current device development concentrates on two versions of this VIPower IC, the VB010 and an enhanced version, the VB040. Both are capable of withstanding 400V and supplying a current up to 7A to the load. The typical device characteristics are listed in table 1. Fig. 2 shows the block diagram of the device.

The control circuitry consists of a driver, input stage, voltage reference, safe operating area protection, collector voltage clamp, thermal protection and diagnostic output. The built-in thermal protection circuit turns off the device whenever the junction temperature exceeds the internally set temperature threshold of 150°C, with a typical 20°C hysteresis.

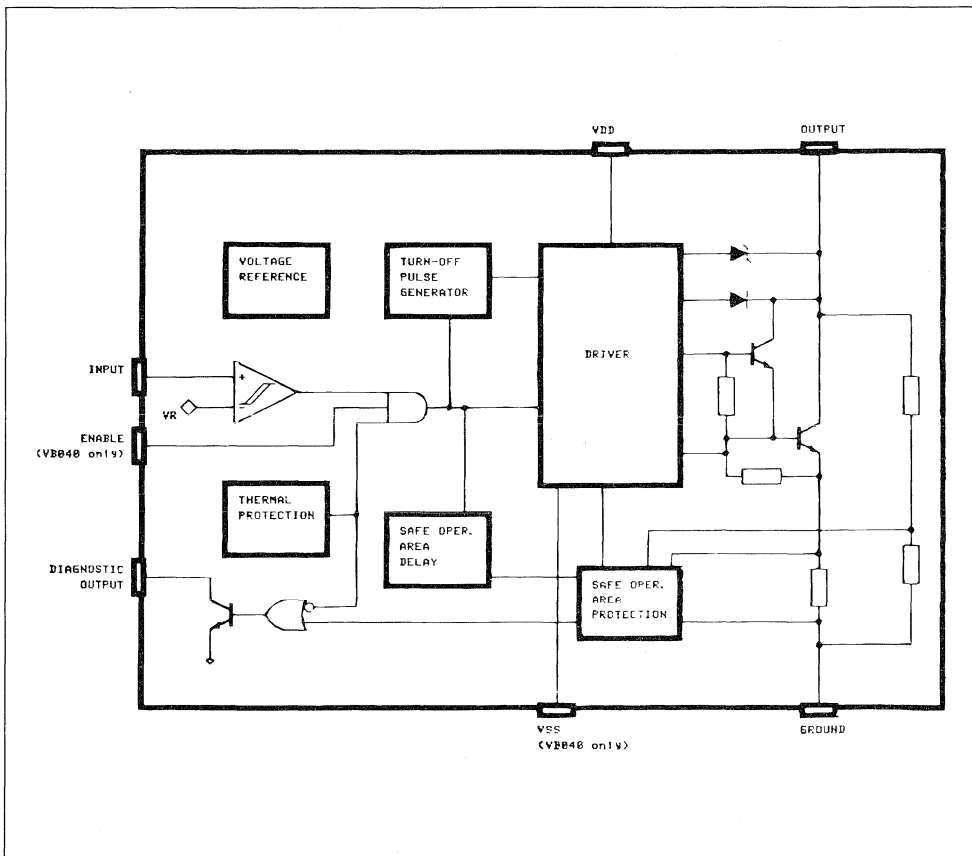
The input stage is a comparator with hysteresis in which the inverting input is set to an internal reference voltage and the non-inverting input is the ex-

ternal logic level input (TTL/CMOS). The chip includes a bandgap voltage reference circuit that is used internally in the comparators, as well as in the thermal protection circuit and to obtain reference current in the current mirrors.

When the thermal protection or safe operating area protection are operating, an open collector diagnostic output gives a low level logic signal (TTL/CMOS) indicating that an overload condition exists.

These first SGS-THOMSON VIPower devices were conceived primarily as power switches with a logic level input for industrial applications with resistive or inductive loads. The chips are assembled in fully isolated plastic packages similar to TO-218 outline, ISOWATT5(tm) for the VB010, or ISOWATT7(tm) when negative supply and inhibit facility are required for the VB040.

Figure 2 : Block Diagram of the Devices.



DRIVER AND POWER STAGE

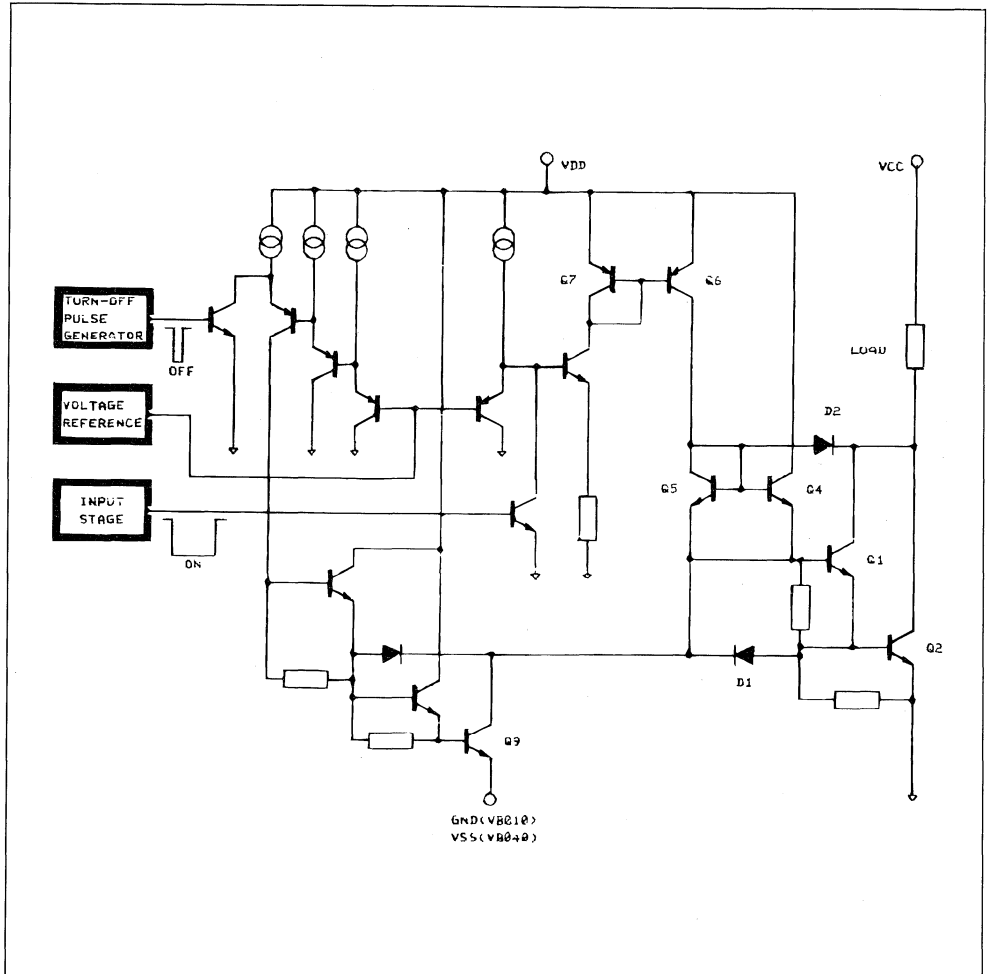
A simplified schematic of the driver stage is shown in fig. 3. The current generator formed by Q4, Q5, Q6 and Q7 supplies up to 200mA to the base of Q1 during the conduction phase. The high voltage, anti-saturation diode D2 keeps Q1 out of saturation. In this way the storage time of the power darlington is minimized.

When the input signal goes low, the current generator that supplies the power darlington base is turned off. At the same time, transistor Q9 is turned on, sinking current from the base of Q1 and Q2. The

emitter of Q9 is connected to ground in the VB010 and in the VB040 can be connected to a negative voltage, allowing a reduction in the turn-off time of the power darlington.

Transistor Q9 is kept on for about 15 μ s beginning from the leading edge of the input signal. This is done in order to reduce the total power dissipation of the control circuit when the power darlington is turned off. The 15 μ s turn-off pulse is generated internally by means of a comparator and a capacitor that is charged with a constant current. This sets, for these devices, a minimum off-time of around 15 μ s.

Figure 3 : Driver Stage.



SAFE OPERATING AREA PROTECTION

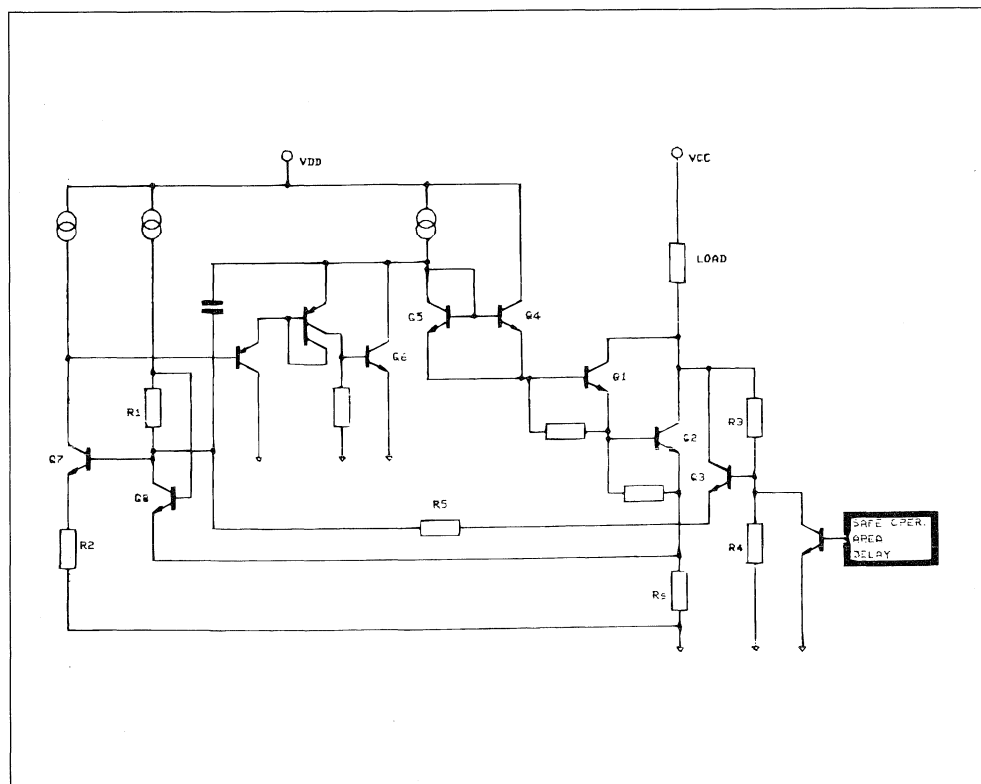
Safe operating area protection, shown in fig. 4, is implemented completely in the chip and does not need any external components. The output current is sensed by an internal metal resistor, of the order of a few milliohms, in series with the emitter of the power darlington. The threshold is fixed by the sum of the voltage drop on R1 and R2 and corresponds to an output current of 8A. When this threshold is reached, transistor Q6 begins to take current from the base of Q4 and Q5 and the power darlington is made to operate in its activate region. As soon as the collector voltage of the power darlington exceeds 10V, the base of Q3 is biased on by R3 and R4 and begins to conduct. A current, fixed by R5 and proportional to the collector voltage of the power darlington, begins to flow in the differential stage

Q7 and Q8, and reduces the threshold voltage and hence the output current in the power stage. With this protection the power darlington is forced to work within its direct safe operating area.

The output current is reduced to zero when the collector voltage of the darlington exceeds 100V. In order to allow the power darlington turn on, the threshold is kept to its maximum value for about 5 μ s, beginning from the rising edge of the input signal, independently of collector voltage. This 5 μ s delay is obtained internally by means of a comparator and the charging time of capacitor.

The device also includes a collector voltage clamp (zener diode D3) that turns on the power darlington as soon as its collector voltage exceeds 450V, which may be caused by the presence of leakage inductance in the power circuit or some fault conditions.

Figure 4 : Safe Operating Area Protection.



APPLICATION EXAMPLE

A simple application is an open-loop, single switch motor drive. Using this configuration, shown in fig. 5, some tests were carried out on the devices. A permanent magnet d.c. motor, having the characteristics listed in table 2, and a d.c. generator, with a variable resistive load, have been used as a mecha-

nical load. The built-in protection ensures complete reliable system operation, even during transient conditions, without the need for external components. In fact, during the starting transient, the device will provide a soft start, by limiting the motor current and reducing the duty cycle. This also happens during mechanical overload.

Figure 5 : Open Loop Single Switch Motor Drive.

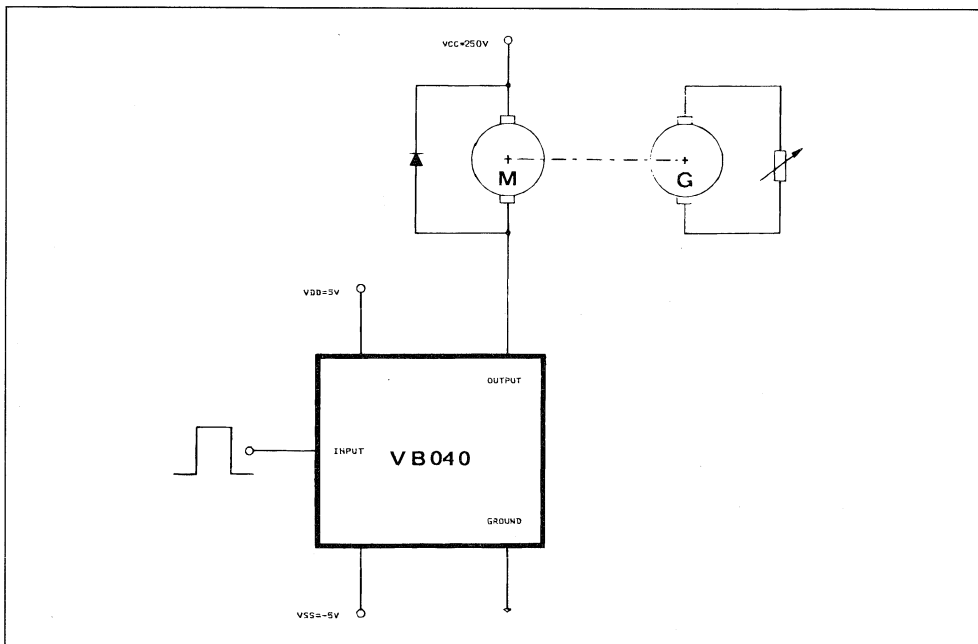
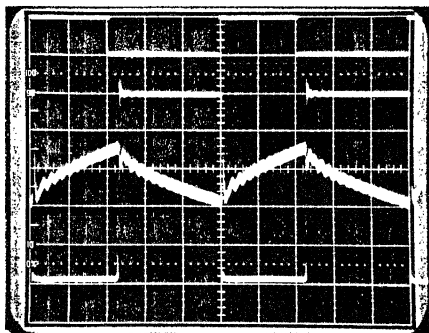


Fig. 6 shows output current and voltage during turn-off where the fall time is approximately 100ns from 3.6A peak current.

Figure 6 : Output Current and Voltage during Turn-off for VB040 ($V = 50V/div$, $I = 1A/div$, $t = 500ns/div$).



CONCLUSIONS

Fabricating the control circuitry and power actuator on the same silicon chip provides the industry with single power ICs to replace often complex circuits. This will benefit the user with simpler design processes, more reliable circuits due to the reduced

number of interconnections, as well as the built in protection features and reduced component count to minimize costs. The future development of application specific versions of the VB010/VB040 have the potential to benefit many power supply designs that will operate in the 20kHz to 30kHz range.

Table 1 : Electrical and Thermal Characteristics.

Parameter	VB010	VB040	Unit
Power Device Supply Voltage	400		V
Output Current (internal limit)	7		A
Saturation Voltage (V_{CEsat})	2		V
Control Circuitry Supply Voltage	5/18	5/13	V
Negative Supply Voltage		- 5	V
Power Dissipation	Internally Limited		
Operating Junction Temperature	- 45/150		°C
Thermal Resistance Junction-case	2.5		°C/W max
Turn on Time	0.5		µs
Storage Time	8	4	µs
Fall Time	1	0.2	µs

Table 2 : Permanent Magnet d.c. Motor Characteristics.

Parameter	Value	Unit
Nominal Current	1.8	A
Nominal Voltage	220	V
Maximum Operating Speed	15000	rpm
Moment of Inertia	6×10^{-4}	kg x m ²
Torque Constant	0.17	Nm x m/A
Armature Resistance	0.96	
Armature Inductance	6.6	mH
Voltage Constant	0.17	V x s

ANALYSIS AND OPTIMISATION OF HIGH FREQUENCY POWER RECTIFICATION

BY J.M.PETER

How can the performances of power electronics be improved ? Today in many cases it is the job of the designer. The fast rectifier switching behaviour depends on the operating conditions. The analysis and the optimisation of this condition can be an important source of improvement in performances.

1. SWITCH-OFF OF FAST RECOVERY RECTIFIERS

One can define theoretically two types of switch-off. See reference [1].

1.1. "FREE-WHEEL MODE" (fig. 1 & 2)

When the rectifier switches-off it is always in parallel with a voltage source. In this case the assumption is that the parasitic inductances are negligible. This type of behaviour can be met in the majority of rectifier applications like free-wheel rectifiers in step-down and step-up converters, full wave rectifiers, etc... (fig. 2). Generally speaking, a rectifier in "free-wheel" mode is always in parallel with a voltage source when it turns-off.

1.2. "RECTIFIER MODE" (fig. 1 & 3)

An inductance defines the di/dt (decreasing slope of the rectifier current) and when the rectifier swit-

ches-off it is always in series with this inductance. This type of behaviour can be met in some applications like rectifier in flyback converters, and many functions in thyristor circuits, (fig. 3). Generally speaking a rectifier in "rectifier mode" is always in serie with an inductance L and this inductance L defines the di/dt . The fundamental difference between these two behaviours is that in the "rectifier mode" there is a stored energy $1/2 L I_{RM}^2$ due to the serie inductance. After the turn-off this energy is dissipated in the rectifier and/or in the associated circuits.

1.3. TURN-OFF LOSSES

"Free-wheel" mode

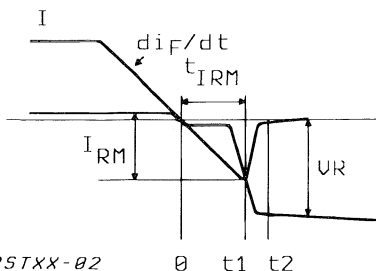
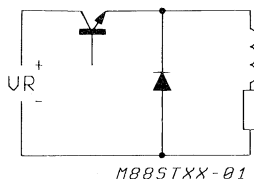
W_{OFF} is the energy dissipated in the rectifier during turn-off.

$$WFR = \int_{t1}^{t2} v_i dt$$

Low voltage (< 200V) fast rectifiers have a high internal capacity and the minority carriers have a very short life time. High voltage fast rectifier have a thicker N silicon layer, and the minority carriers have longer life time and consequently different behaviour during the blocking state. (higher I_{RM} and t_{IRM} - more damping.

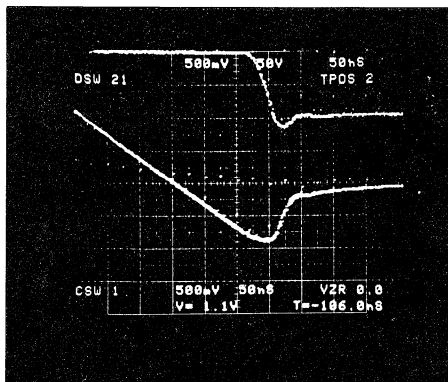
Figure 1 : Fast Rectifier : The Two Turn-off Behaviours.

"FREE-WHEEL" MODE

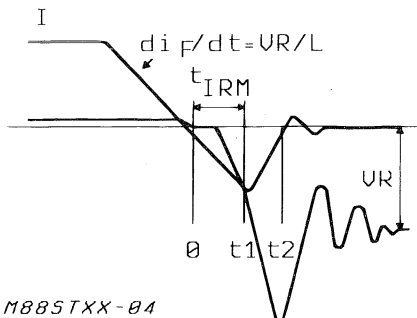
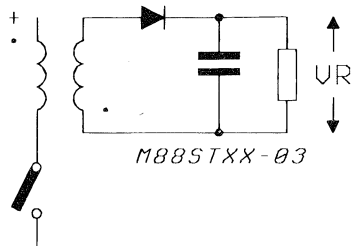


di/dt fixed by the transistor (or by the external circuit)
Low Losses in the Rectifier
 $W_{OFF} = K \cdot V_R \cdot I_{RM} \cdot t_{IRM}$
($0.15 < K < 0.35$)

NO OSCILLATIONS AND OVERVOLTAGE

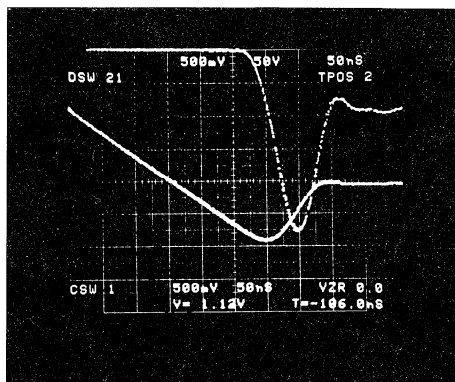


"RECTIFIER" MODE



di/dt fixed by the inductance
 $di/dt = V_R/L$
High Losses in the Rectifier
 $W_{OFF} = K \cdot V_R \cdot I_{RM} \cdot t_{IRM} \cdot 1/2 \cdot \tau^2_{RM}$
In case of snubber a part of his energy is dissipated in the snubber

ALWAYS OVERVOLTAGE AND OSCILLATIONS IN SOME CONDITIONS



BYT30-1000 - $I_F = 30A$ - $di/dt = -75A/\mu s$ - $V_R = 100V$ - $T_{case} = 25^\circ C$ (5A/C - 50V/C - 50nS/C)

According to the experimental results the turn-off lost energy $(W)_{FR}$ in free-wheel mode can be written :

$$(W)_{FR} = K \times V_R \times I_{RM} \times t_{IRM} \quad (1)$$

Max Voltage Rating	200	400	800	1000	1200
K	0.12	0.14	0.22	0.28	0.35

RECTIFIER MODE

Losses in this mode are the sum of the storage energy $1/2 L I_{RM}^2$ and the recovery energy $(W)_{FR}$:

$$(W)_{REC} = (W)_{FR} + 1/2 L I_{RM}^2 \quad (2)$$

In some cases, oscillations can occur. This depends on the damping due to the current tail effect after switch-off. When oscillations occur energy is dissipated during the oscillations partly in the rectifier and partly in the circuit. When snubbers are used a significant part of the energy is dissipated in the snubber.

2. PRACTICAL SWITCH-OFF BEHAVIOUR

The two cases, "free-wheel" mode and "rectifier mode" are "simplified cases" easy to simulate in a laboratory characterisation, but in practical equipment there is always a possible overlap between the two theoretical modes, because :

$K^{(1)}$ is a constant that depends on the thickness of the N type silicon layer.

1/ There are no circuits without parasitic inductances.

2/ The rise time (or the fall time) of the switch is not infinitely fast in comparison with the duration of the current change :

Experimental results shows that in all cases following formula can be used :

$$(W)_{OFF} = (W)_{FR} + 1/2 L_S I_{RM}^2 \quad (3)$$

Where L_S : serie inductance

This important relationship (3) is a useful tool for the designer, giving him the main parameters that influence the turn-off energy.

N.B. : The following relationship (4) is only true for pure "rectifier mode".

$$(W)_{OFF} = Q_R \times V_R \quad (4)$$

Where Q_R = recovered charge

⁽¹⁾ Experimental - Defined with SGS THOMSON fast rectifiers.

Figure 2 : Rectifiers in "Free Wheel" Mode.

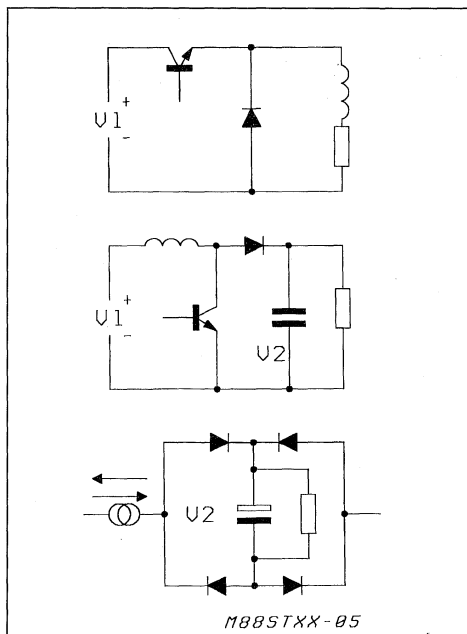


Figure 3 : Rectifiers in "Rectifier" Mode.

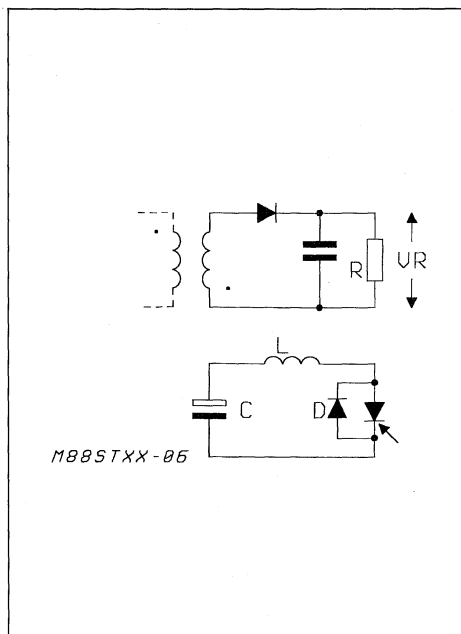


Figure 4 : Switch -off behavior of the ultrafast BYT12-400V rectifier (current rating 12A – Voltage rating 400V).

Conditions : $I_F = 13A$ $di_F/dt = -150A/\mu s$ $V_R = 100V$ $T_{case} = 25^\circ C$

In case of rectifier mode : $L = 0.6\mu H$

The turn-off lost energy calculated by the current and voltage is :

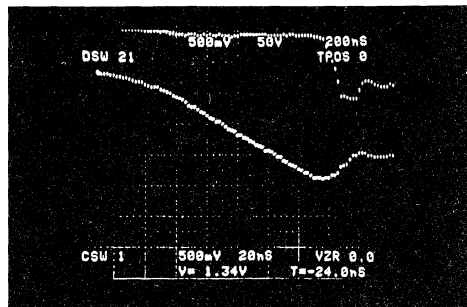
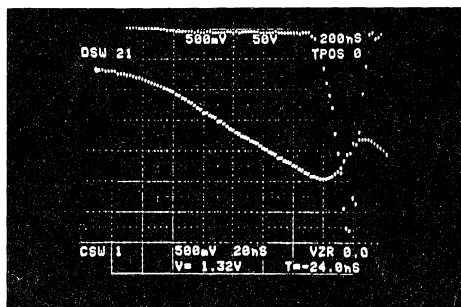
(W)_{FR} = 3μJ "free-weel" mode

(W)_{REC} = 10μJ "rectifier" mode

The storage energy in the inductance is : $1/2 L I_{RM}^2 = 7.5\mu J$

The use of this equation for a lot of practical circuits can be considered as a first approximation. It leads

to over estimated losses, if the rectifier does not operate in pure "rectifier mode".



3. CHARACTERISTICS OF FAST RECTIFIERS

The characteristics of fast rectifiers are the result of a trade off between :

- Speed (I_{RM})
- Max voltage rating (V_{RRM})
- Forward voltage drop (V_F)

Example : 12A fast rectifiers

V_{RRM}		200	400	800	1000
Type		BYW81	BYT12-400	BYT12-800	BYT12-1000
"High Efficiency Type"					
$T_j = 100^\circ$	$I_{RM}(A)$	1.8	3.7	6	7.8
$di_F/dt = -50A/\mu s$					
	$t_{IRM}(\mu s)$	0.05	0.075	0.160	0.200
V_F	(V)	$0.66 + 0.0071$	$1.1 + 0.021$	$1.3 + 0.031$	$1.3 + 0.031$

OPERATING CONDITIONS

I_{RM} increases with di_F/dt (fig. 5).

I_{RM} increases with T_j (fig. 6).

The important points that emerge are :

1/ High voltage fast rectifiers are not so fast as low voltage fast rectifiers, (comparing devices of equal current rating).

2/ T_j and di_F/dt have a strong influence on the reverse recovery current.

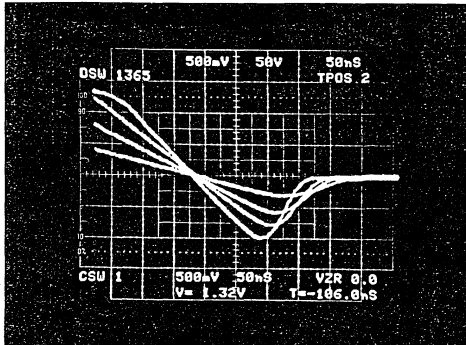
4. EXAMPLES

4.1. FLYBACK CONVERTER (fig. 7)

The behaviour is "pure rectifier" ; the current source is an inductance L always in series with the rectifier.

For a frequency less than 100kHz the switching losses are small in comparison to the conduction losses, because di_F/dt defined by V output/ L is always small, (see table fig. 7).

Figure 5 : Switch off behavior of the fast rectifier BYT12P 1000 (current rating 12A voltage rating 1000V)
Influence of the diF/dt



5A/C 50nS/C $T_J = 25^\circ\text{C}$.

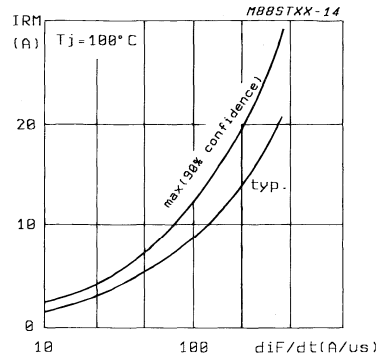
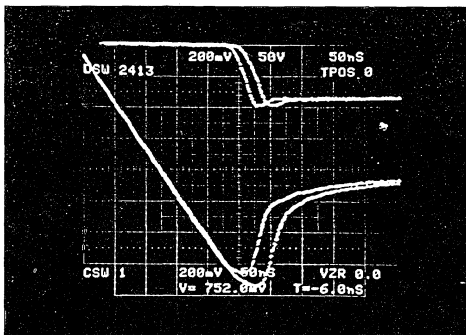
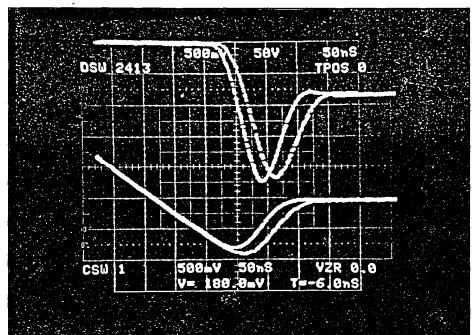


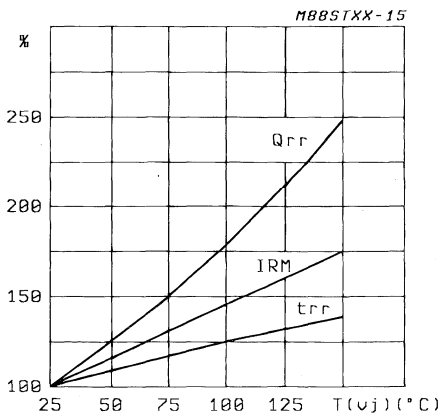
Figure 6 : Switch-off behaviour of the fast rectifier BYT12 1000
Influence of T_J
One curve $T_J = 25^\circ$, one curve $T_J = 60^\circ$



100V/C 2A/C 50nS/C.



100V/C 5A/C 50nS/C.



How can the designer reduce the losses ?

1/ The ratio I_{peak}/I_{AVG} is very unfavorable in this type of circuit. It is essential when the peak voltage is less than 200V that "high efficiency ultra fast" family which have very low conduction losses are used. When the peak voltage is greater than 200V one solution is to use one rectifier with larger current rating.

Example :

In the same circuit with :

- BYT12-800 : conduction losses = 7.6W
- BYT30-800 : conduction losses = 6W.

2/ Reduce the junction temperature. If T_j is decreased from 100° to 75°C the switching losses are reduced by 20%.

4.2. SMALL CURRENT RECTIFIER (fig. 8)

A transformer with a leakage inductance measured on the secondary side $L_S = 1\mu H$ supplies a fast diode D. The average output current is 0.8A and the output voltage is 48V.

The designer wants to use the popular diode BA157. This is not possible because the total power dissipation is 1.15W at 40kHz. At this frequency he can only use a popular 2A current rated diode (for 0.8A rectified current) and at 200kHz there is no solution with popular diodes (see table in fig. 8).

How can the designer reduce the losses ?

1/ Choose a diode in the "high efficiency family". For example he can use the BYW100 for 40kHz to 200kHz, (see table fig. 8).

2/ Reduce the leakage inductance : with a leakage inductance $L_S = 0.1\mu H$, BY218 at 200kHz (1.24W, $\Delta T_j = 93^\circ C$).

4.3. FULL WAVE OUTPUT RECTIFIER

There are two different full wave rectifying circuits.

4.3.1. VOLTAGE SOURCE-CURRENT OUTPUT. Current and voltage behaviour are indicated figure 9. The inductance L_S is the leakage inductance of the insulation transformer.

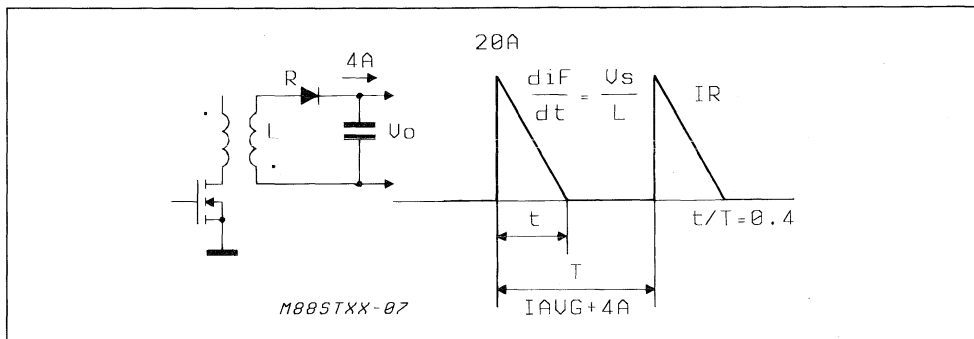
The 4 rectifiers operate in an intermediate mode between "free wheel" and "rectifier", because there are some $1/2 L_S I_{RM}^2$ losses.

4.3.2. CURRENT SOURCE - VOLTAGE OUTPUT (fig. 10). In this circuit, each rectifier operates in "free wheel" mode. The series inductance does not introduce additional losses. (This assumes there is no parasitic inductance between the rectifiers and the capacitor C).

How can the designer reduce the losses ?

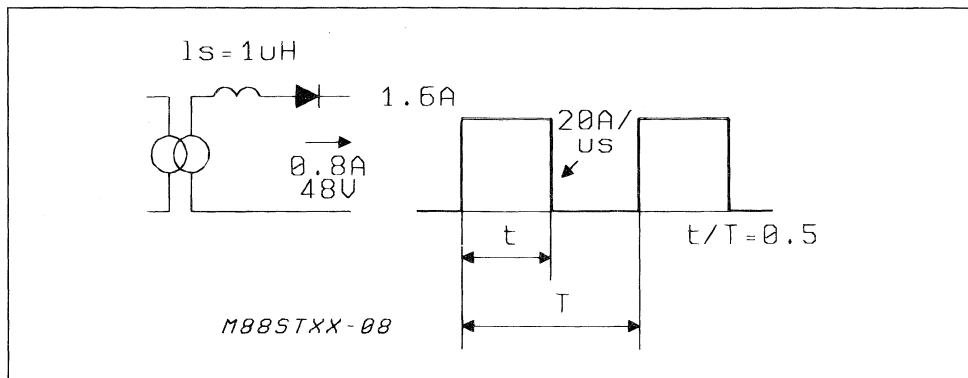
Figure 7 : Flyback rectifier output average current 4A.

Below 100kHz the switching losses are negligible, in comparison with the conduction losses. The reason is limited di/dt , consequently limited I_{RM} .



V_D (V)	12	46	100
Rectifier	BYW81-100 "High Efficiency"	BYT12-400	BYT12-800
Conduction Losses (W)	3.2	6	7.6
Switching Losses a 50kHz (W)	0.006	0.05	0.81
Switching Losses a 200kHz (W)	0.05	0.5	5.5

Figure 8 : The popular diodes BA157 –BY218 are not fast for high frequency rectifying. The BYW100 is well adapted.



Diode	BA157 Popular	BY218 Popular	BYW100-200 High Efficiency
I_{RM} a $100^\circ \text{ dI/dt} = -20\text{A}/\mu\text{s}$ (A)	2.8	2.8	0.75
t_{IRM} a $100^\circ \text{ dI/dt} = -20\text{A}/\mu\text{s}$ (A)	0.14	0.14	0.05
$(W)_{FR}$ (μJ)	2.08	2.08	0.01
$1/2 L_S I_{RM}^2$ (μJ)	3.9	3.9	0.28
Conduction Losses (W)	0.944	0.744	0.592
Switching Losses a 40kHz (W)	0.2	0.2	0.012
Switching Losses a 200kHz (W)	1.3	1.3	0.06
Total Diodes Losses a 40kHz (W)	1.15	0.44	0.6
ΔT_j a 40kHz ($^\circ\text{C}$)	115°	71°	60°
Total Diodes a 200kHz (W)	1.97	1.77	0.65
ΔT_j a 200kHz ($^\circ\text{C}$)	197°	132°	65°

a) Voltage source - current output

Reduce the transformer leakage inductance. Table of figure 11 shows that in the case of the 400V 10A 200kHz bridge circuit the suppression of the inductance L can save $4 \times 16.5\text{W} = 66\text{W}$.

Replace in the same circuit the high voltage fast rectifier BYT12-600 by 3 "high efficiency" BYW81-200 in series (see fig. 12-table). The total losses decrease from 186W to 58W. This result is very important as it shows it is more efficient to use several "high efficiency" ultra fast rectifier instead of a single high voltage, one for high frequency operations.

b) Both

Use of sinusoidal current (resonant converter) instead of rectangular waveforms. Figure 11 shows that for the same conditions (400V - 10A - 200kHz) the switching losses with a sinusoidal current are only $4 \times 7.5 = 30\text{W}$ ($4 \times 22 = 88\text{W}$ with rectangular wave forms).

4.4. STEP UP CONVERTER

The rectifier operate in "free wheel" mode. The main losses in this case occur in the transistor during the turn-on similar to the step down converter). Figure 13 shows that with 600V output at 40kHz, if the rectifier switching losses are reasonable, the transistor turn-on losses are too high.

How can the designer reduce these turn-on losses ? (fig. 13)

a) Decrease the rectifier junction temperature by more efficient cooling.

If the BYT12-800 junction temperature decrease from 100° to 70°C , the transistor turn-on losses decrease from 39.5W to 33W.

b) To replace one BYT12-800 by 4 "high efficiency" BYW81-200 in series. The total balance is a reduction in losses from 39.5 to 16.6W in the transistor and the same losses in the rectifier.

SYNTHESIS

Two major actions reduce switching losses caused by fast recovery rectifiers :

1. ADAPTED CHOICE

* The fastest rectifier compatible with the peak voltage in the application.

* If the peak voltage V_R exceeds 400V the designer must analyse carefully the switching losses :

- These losses are proportional to $I_{RM}^2 \times V_R$.
- A 800V fast rectifier has an I_{RM} approximately two times higher than a 400V fast rectifier (same current rating).

Figure 9 : Voltage Source, Output Current Full Bridge Circuit.

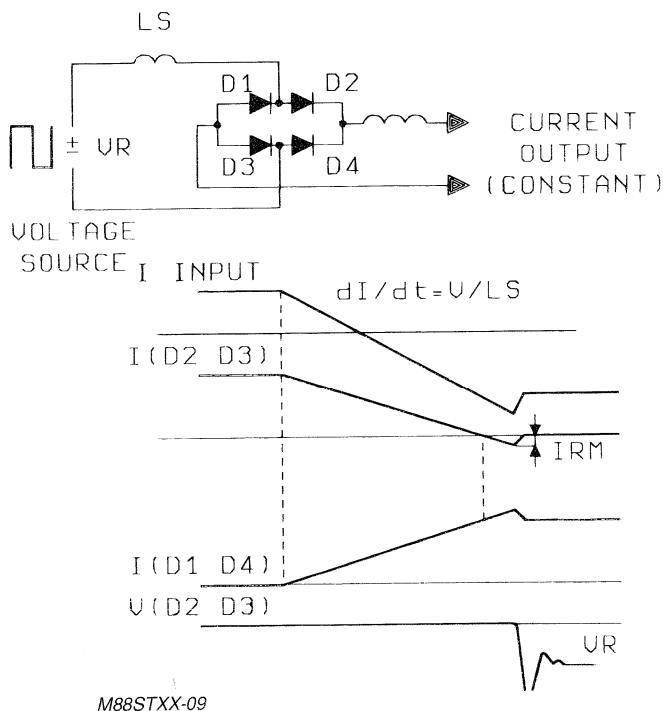


Figure 10 : Current Source, Output Voltage Full Bridge Circuit.

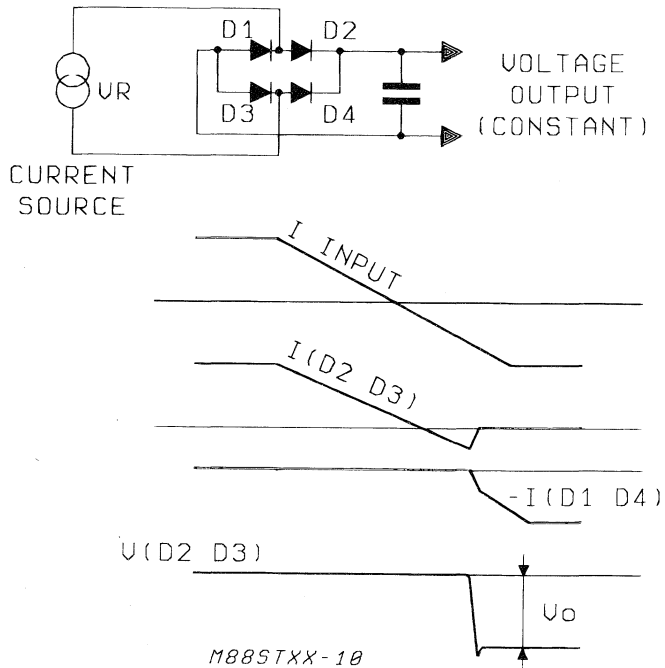


Figure 11 : Switching losses (per leg) in a full wave 200kHz bridge circuit.

Output 10A

In case of voltage source, current output, the (leakage) inductance 1 introduce 1/2 LSI2RM losses A

In case D, the losses are smaller ($7.5 \times 4 = 15W$ instead of $22 \times 4 = 88W$ because di/dt is smaller, consequently IRM smaller.

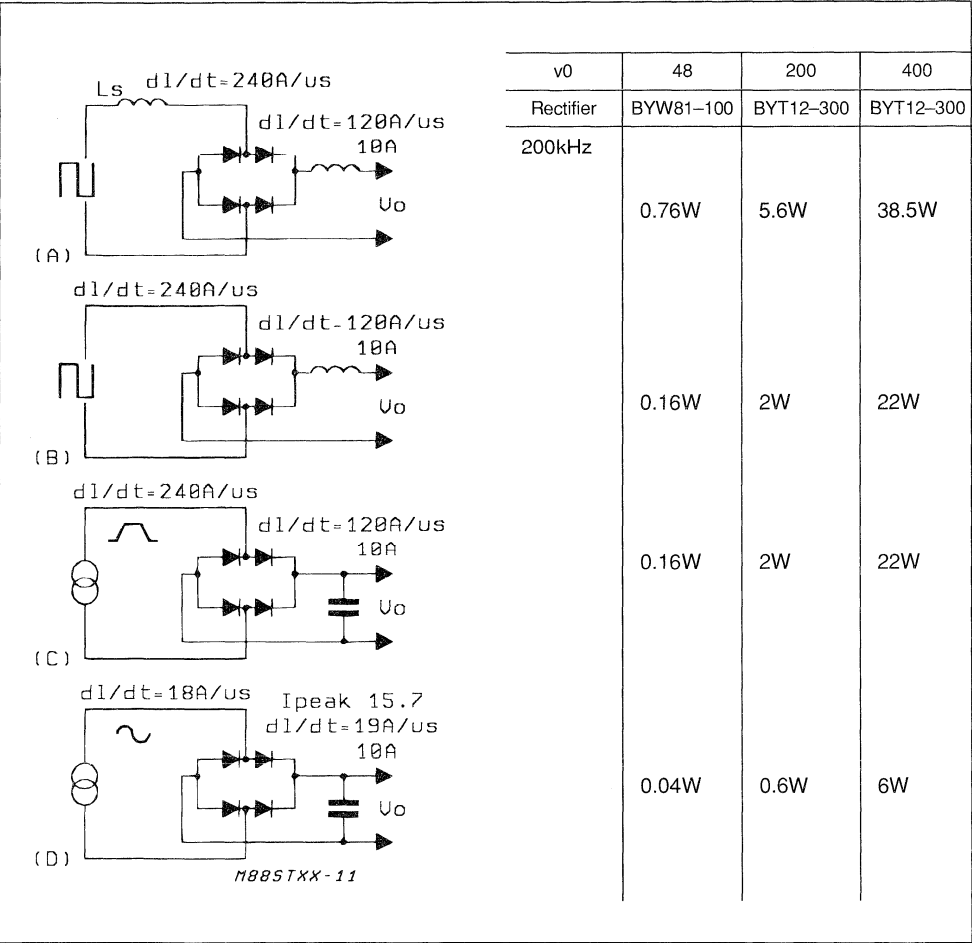
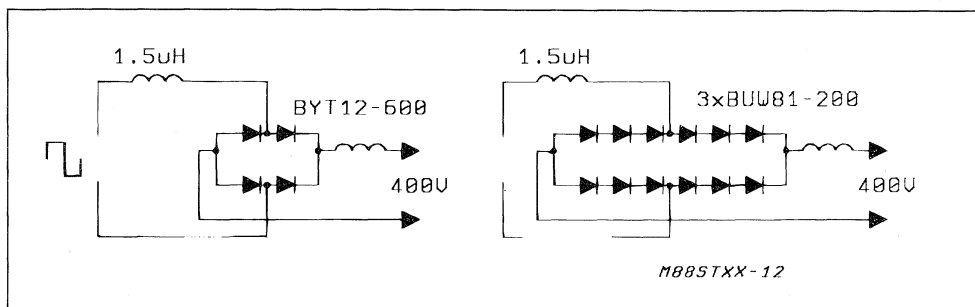


Figure 12 : Switching losses (per leg) in the full wave 400V 200kHz bridge circuit with two different "rectifiers".

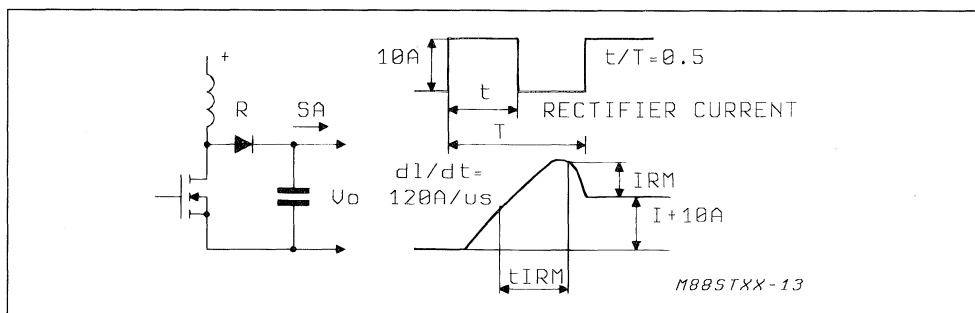
To replace the high voltage BYT12-600 rectifier by 3 "High efficiency" ultra fast BYW81-200 in series reduces dramatically the total losses. This is why the I_{RM} from BYW81 is very low and the voltage drop of this high efficiency rectifier is very low.



Rectifier	BYT12-600	3 x BYW81-200
CONDUCTION LOSSES (W)	8	11
SWITCHING LOSSES (W)	38.5	3.5
TOTAL LOSSES PER LEG (W)	46.5	14.5

Figure 13 : In the step-up (or step down) converter the majority of losses occur in the transistor, specially when high voltage rectifier is used.

In some cases replacing a high voltage rectifier by several faster rectifiers in series (consequently lower voltage rating) can minimize the total losses despite the increasing of the rectifier conduction losses.



V_D	48	300	600	600
Rectifier	BYW81-100	BYT12-400	BYT12-800	4xBYT81-200
$(di/dt = 120A/\mu s) I_{RM} (A)$	3.8	6	10.5	3.8
$(T_j = 100^\circ) t_{IRM} (\mu s)$	0.04	0.06	0.12	
Rectifier Conduction Losses (W)	3.65	6.5	8	14.6
Rectifier Switching Losses a 40kHz (W)	0.04	0.6	6.7	0.5
Total Rectifier Losses a 40kHz (W)	3.7	7.1	14.7	15.1
Transistor Turn-on Losses a 40kHz (W)	1.32	10.7	39.5	16.6

The rectifier voltage drop increases with the rating voltage.

Example : BYW81 "high efficiency" 200V rating $V_F = 0.85V$ (max).

BYT12-600 600V rating $V_F = 1.8$ (max).

Important consequences :

If the switching frequency is greater than 40kHz in many cases it will be more efficient to replace one high voltage (600 - 800 - 1000V) rectifier by a series of ultrafast rectifiers (200V or 400V). Despite the increase of conduction losses, the dramatic reduction of switching losses allows the decrease of the total losses.

2. OPTIMAL OPERATING CONDITIONS

2.1. In many cases the parasitic inductances give additional losses. A reduction of those parasitic inductances L_S decreases not only the voltage spikes but also the switching losses.

2.2. Junction temperature plays an important role. The switching losses are approximately proportional to T_J . Improving the rectifier cooling is very important for all high frequency rectifiers.

2.3. For full wave rectifying circuits, with an isolation transformer the switching losses are always lower in case of :

Current source $\rightarrow$ rectifying $\rightarrow$ voltage source
than :

Voltage source $\rightarrow$ rectifying $\rightarrow$ current source
because the impedance due to the transformer leakage inductance is integrated in the current source, and does not play any role in the additional losses.

2.4. The use of the resonant circuit with sinusoidal current waveforms allows to reduce significantly the switching losses due to the rectifier limited dI_F/dt or to the smaller V_R reapplied voltage.

CONCLUSION

Reducing the switching losses in high frequency converters is a team work.

The manufacturer has improved the fast recovery rectifier characteristics. The designer has now with some tools the possibility to analyse with a better accuracy the rectifier behaviour, and choose the optimal solution in order to minimize the losses.

STEPPER MOTORS

BIPOLAR STEPPER MOTOR CONTROL

By Pierre PAYET BURIN

This application note is intended to provide design details for the implementation of a stepper motor control, built around the TEA3717.

This integrated circuit has been developed to offer control and current regulation of up to 1A, in one winding of a bipolar motor.

Two TEA3717s and a minimum of external components are sufficient to implement the full control function of a two-phase bipolar stepper motor.

The system can be commanded, according to the desired mode of operation, by either fixed or programmable logic.

FUNCTIONAL DESCRIPTION

The circuit is organized around a H-bridge configured by four transistors and their integrated free wheel diodes.

The "Phase" input controls the switching of the bridge transistors and also determines the direction

of the current flow in the winding. The signal applied to this input is first gated through a Schmidt trigger and then through a delay element so as to avoid a simultaneous conduction of transistors when direction of current in the bridge is reversed.

Regulation of winding current is performed by chopping action on the power supply for a duration t_{off} determined by a monostable.

This monostable is triggered by the output level swing of a comparator, to the input of which a voltage proportional to delivered output current is applied.

The current spikes corresponding to the diodes reverse recovery time are filtered by a low pass filter $R_C C_C$ to not trigger the comparator.

Three comparators are available for this purpose : their thresholds are internally fixed ratios of V_R input voltage. Each of them can be selected individually by using I_1 and I_0 inputs.

Figure 1 : TEA3717 Block Diagram.

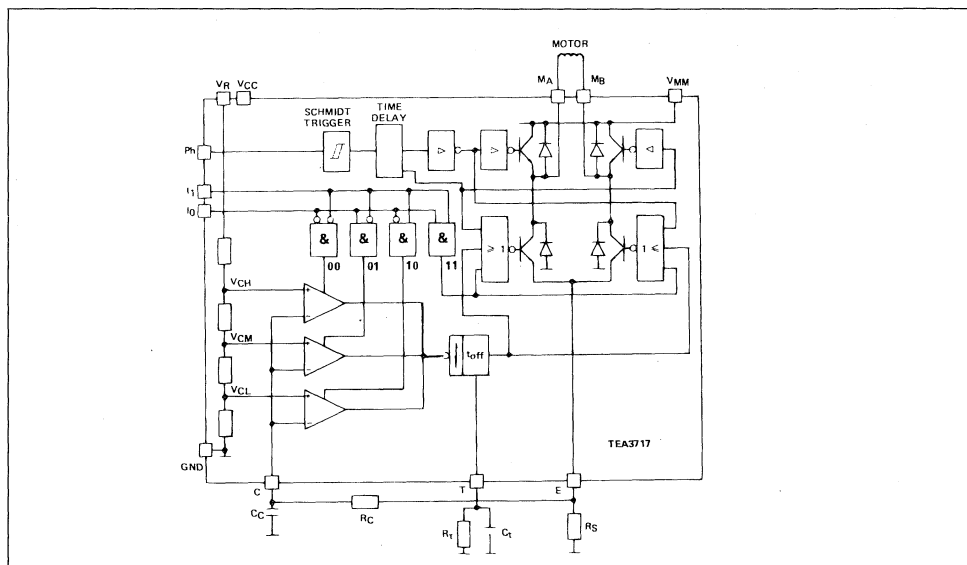
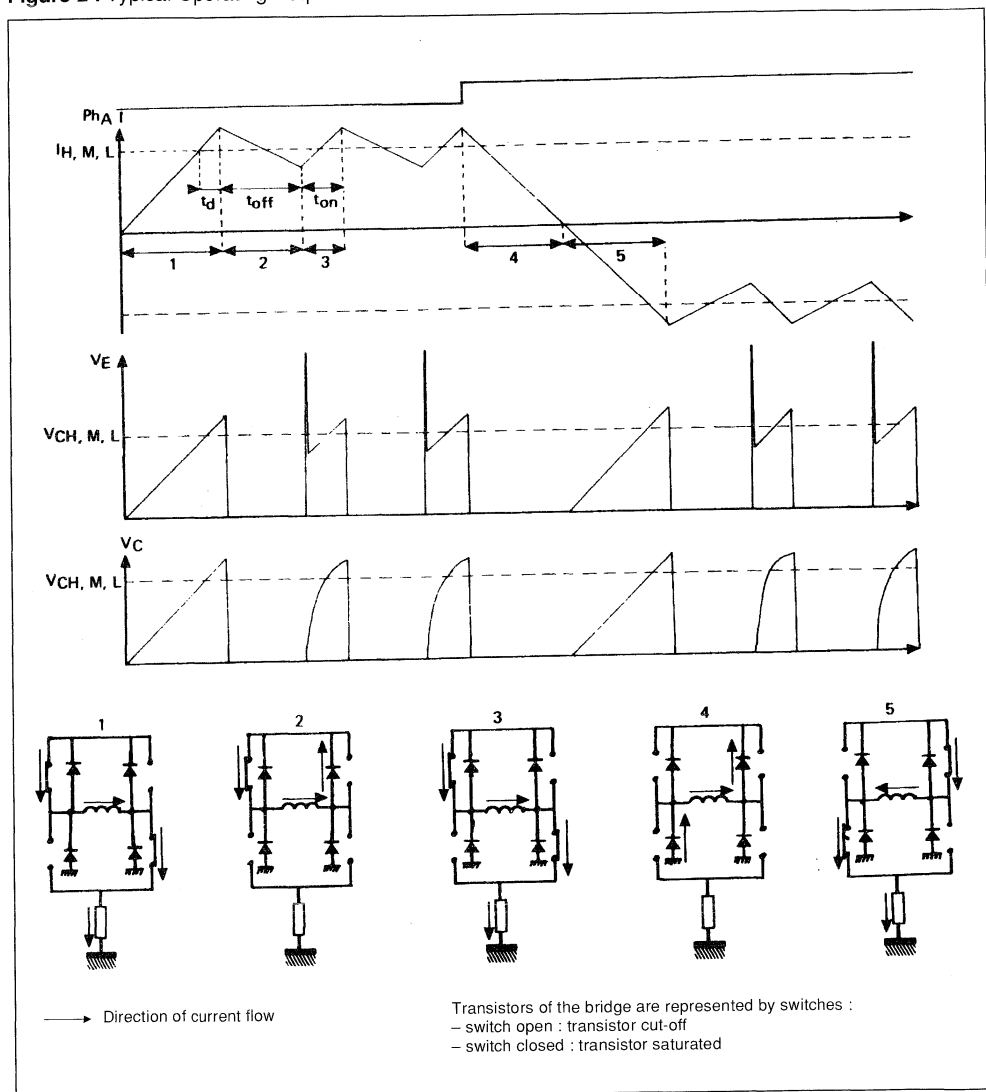


Figure 2 : Typical Operating Sequences.



CONTROL OF BIPOLAR TWO-PHASE MOTOR

The proposed diagram features two TEA3717s each controlling one winding. Full-step and fraction-of-a-step operation is performed by combined use of phase and current level selection control inputs.

Figure 3 : Control of a Bipolar Two-phase Motor.

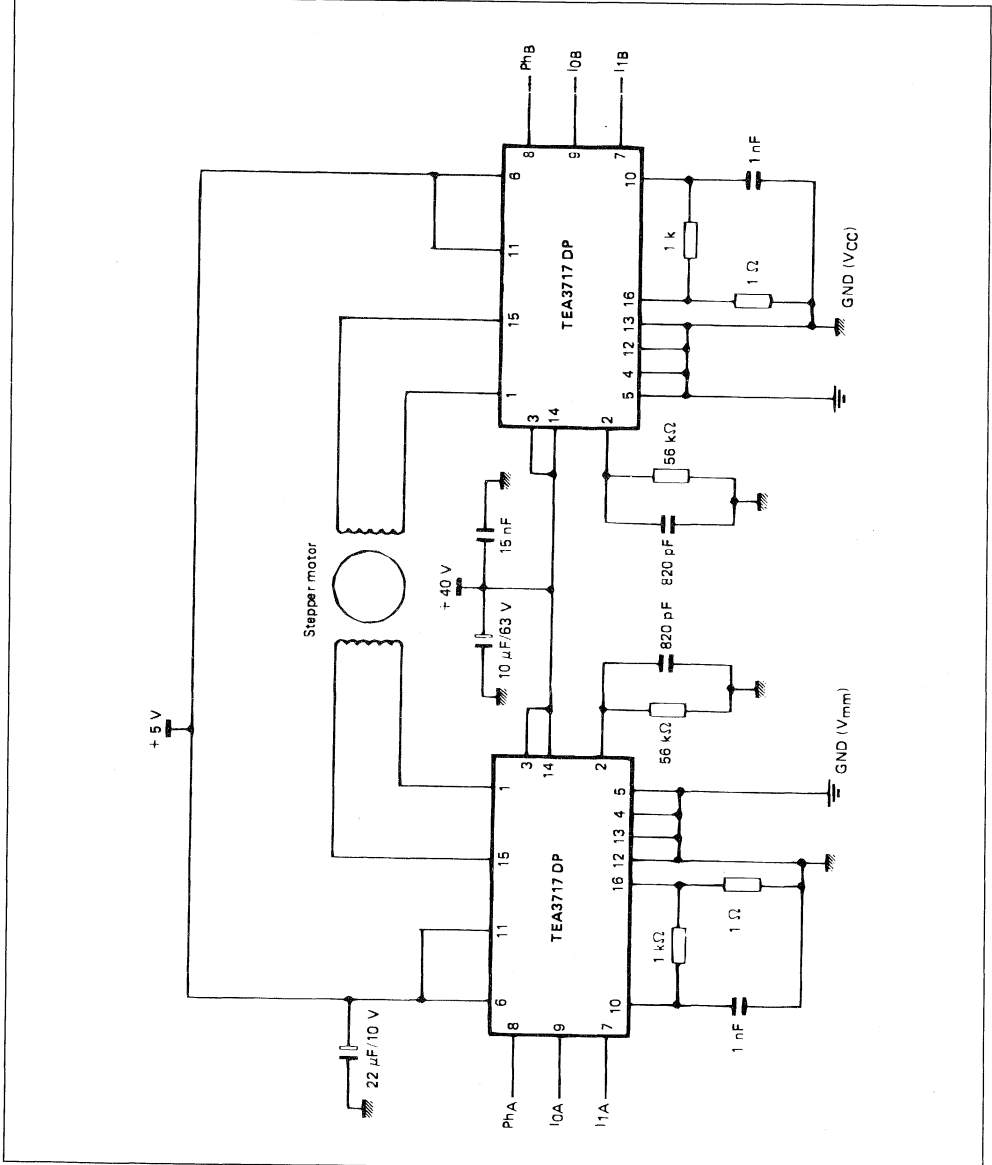
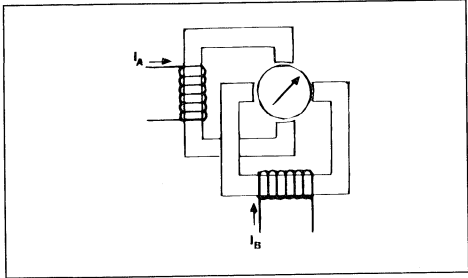


Figure 4 : Winding Currents for Rotation in Full-and Micro-steps.



I_A, I_B : Currents flowing through motor windings.
 I_H, I_M, I_L : Current thresholds selected by I_0, I_1 .
 I : any of I_H, I_M or I_L values.

I_0	I_1	I
1	1	0
0	1	I_L
1	0	I_M
0	0	I_H

N° of steps	I_A	I_B
1	I	I
2	I	$-I$
3	$-I$	$-I$
4	$-I$	I

Full step.

N° of steps	I_A	I_B
1	I	I
2	I	0
3	0	$-I$
4	$-I$	$-I$
5	$-I$	0
6	0	I
7	I	I

1/2 step.

N° of steps	I_A	I_B
1	I	I
2	I_M	I_L
3	I_M	$-I_L$
4	I	$-I$

1/3 step.

N° of steps	I_A	I_B
1	I	I
2	I_M	I_L
3	I	0
4	I_M	$-I_L$
5	I	$-I$

1/4 step.

N° of steps	I_A	I_B
1	I	I
2	I_H	I_M
3	I_H	I_L
4	I_H	$-I_L$
5	I_H	$-I_M$
6	I	$-I$

1/5 step.

N° of steps	I_A	I_B
1	I	I
2	I_H	I_M
3	I_M	I_L
4	I	0
5	I_M	$-I_L$
6	I_H	$-I_M$
7	I	$-I$

1/6 step.

N° of steps	I_A	I_B
1	I	I
2	I_H	I_M
3	I_M	I_L
4	I_H	I_L
5	I_H	$-I_L$
6	I_M	$-I_L$
7	I_H	I_M
8	I	$-I$

1/7 step.

N° of steps	I_A	I_B
1	I	I
2	I_H	I_M
3	I_M	I_L
4	I_H	I_L
5	I	0
6	I_H	$-I_L$
7	I_M	$-I_L$
8	I_H	$-I_M$
9	I	$-I$

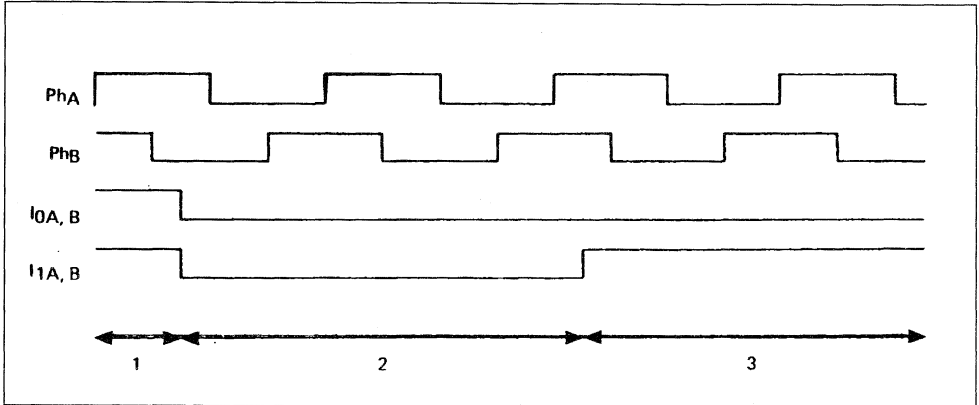
1/8 step.

FULL-STEP OPERATION :

This is moto's typical mode of operation. Simultaneous power supply to both windings guarantees availability of maximum torque.

"Phase" inputs determine the direction of current flow in the windings, while inputs I_0 and I_1 at a constant level, select the level of this current. This is the simplest type of control implementation.

Figure 5 : Signals to Provide to Controller for Full-step Rotation.



1 - Motor not controlled.

2 - Rotation of 7 steps @ I_H max. current.

3 - Rotation of 6 steps @ I_L low current.

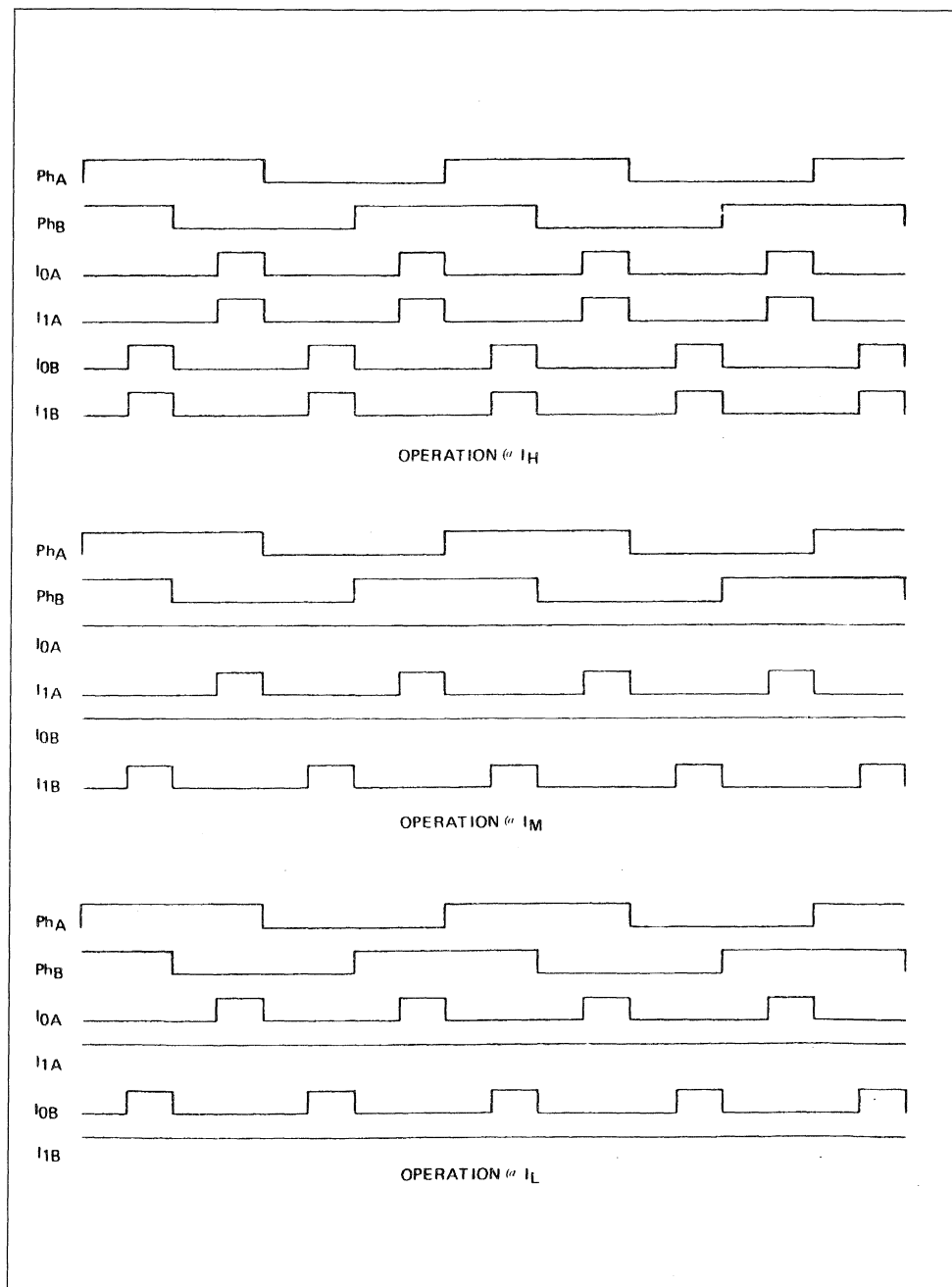
HALF-STEP OPERATION :

This mode allows to double the motor resolution and also to eliminate certain vibrations. Power is applied alternately to one winding and then to both. In half-step position, where only one winding is powered,

torque available on motor spindle is at its lowest value.

Same control signals as those used for full-step operation are applied to "phase" inputs, and I_0 , I_1 inputs are used to annul the current in one winding.

Figure 6 : Signals to Provide to Controller for Full-step Rotation.



MICRO-STEP OPERATION:

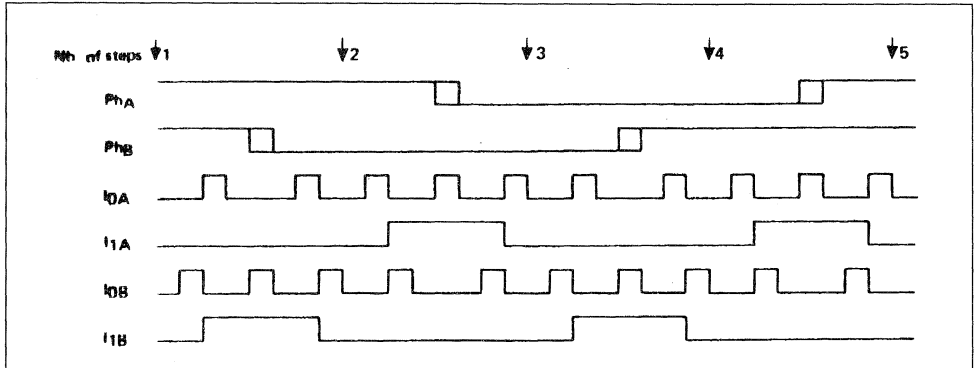
Micro-steps of up to 1/8 are obtained by implementing the flow of different supply current levels through both windings.

This type of operation may be envisaged if a good rotational regularity is required.

Some factors reduce the positioning precision of micro-steps :

- difference between theoretical value and available value for winding current,
 - comparator threshold levels dispersion,
 - motor winding characteristics dispersion.
- These factors don't affect full-step position

Figure 7 : Signals to Provide to Controller for Rotation in 1/8th of a Step.

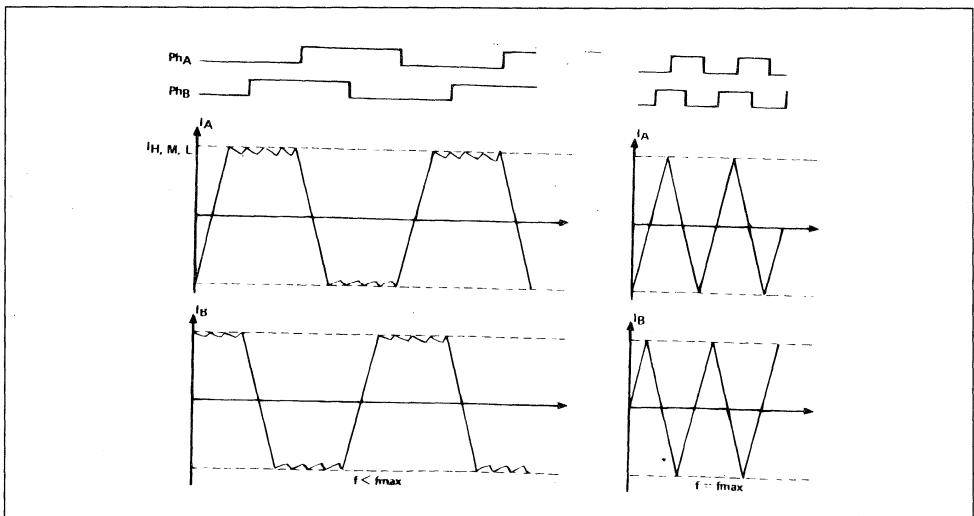
**CHOICE OF OPERATING FREQUENCY**

Motor's rotational speed is determined by the frequency of Ph_A and Ph_B signals.

This speed is limited by the mechanical characteristics and the time constant of L, r circuit formed by the winding.

The rate of current increase in the winding depends on V_{mm} . Thus, if operation at maximum speed is desired, it would be a good practice to work with high supply voltages.

Figure 8 : Phase Currents for two Differents Speeds.



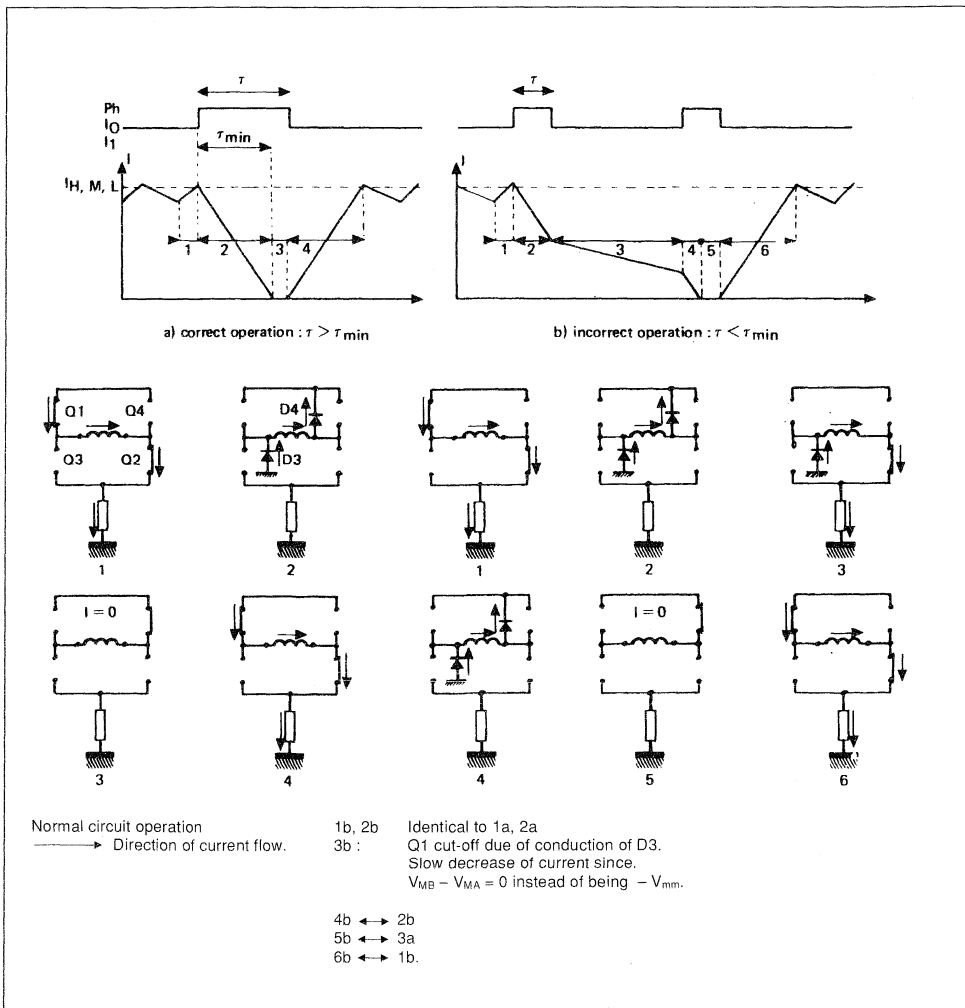
$I_1 = I_0 = \text{Ph}$ COMMAND

Simultaneous application of control signals to three inputs Ph, I_1 and I_0 (or to Ph and one of I inputs while the other is at high level), is used for half-step operation or unipolar mode.

It must be ensured that the time t during which $\text{Ph} = I_1 = I_0 = 1$ is higher than the time $t_{\min}$ required to annul the winding current.

If while the current is still positive, control signals $\text{Ph} : I_0 = I_1 = 1$ are applied to corresponding inputs, diode D2 or D3 will conduct and cause Q1 and Q4 to be turned-off, which prevents the current rise in the winding and disturbs the proper motor operation. Blocking of Q1 and Q4 is performed by a built-in protection unit and prevents the parasitics generated by the conduction of D2 and D3 to cause any short-circuit within the bridge.

Figure 9 : Operation with $\text{Ph} = I_1 = I_0$.



CHOICE OF T_{OFF} : SWITCHING TIME FOR CURRENT REGULATION

The value of t_{off} determines the quality of the current regulation in one phase.

The larger the t_{off} , the more important is the current ripple.

Value of t_{off} is found from the expression $t_{off} = 0.69 R_t C_t$ where $1k\Omega \leq R_t \leq 100k\Omega$

A suitable value of t_{off} for the majority of applications is $30\mu s$.

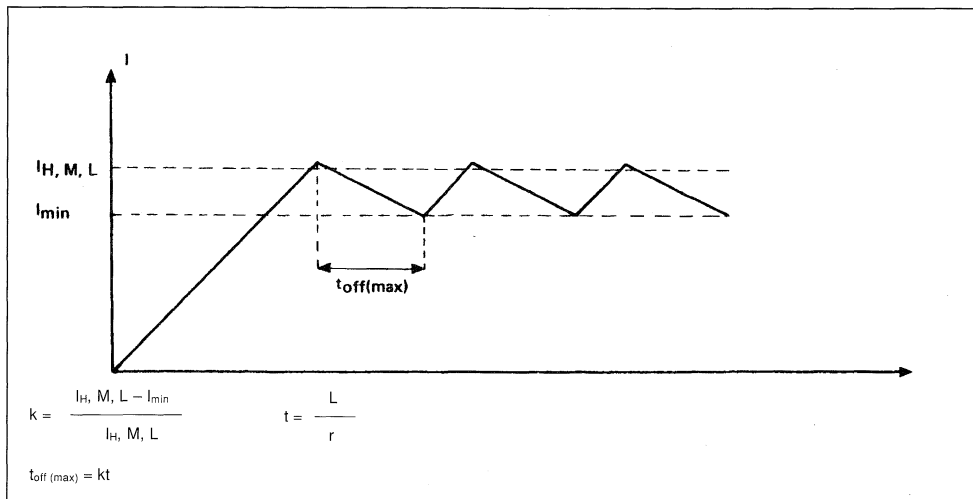
* $t_{off(max)}$

This is the t_{off} value over which the ripple value becomes excessive

Let's k be the desired ripple value and $t = L/r$ the time constant of motor winding, then :

$t_{off(max)}$ is given approximately by : $t_{off(max)} \approx kt$

Figure 10 : Winding Current @ off (max).



*** $t_{off(min)}$**

This is the limit under which the current regulation is not guaranteed.

Even if the current continually exceeds the threshold levels I_H , I_M or I_L , the device will ensure a minimum conduction time $t_{on(min)}$ which is combination of two periods :

- t_d : comparator trigger time and transistor desaturation time imposed by TEA3717

- t'_d : this is the time required by V_C to reach the comparator threshold level and is determined by low pass filter R_C , C_C .

Therefore, t_{off} must be selected to be long enough to allow the current to fall to a level below I_H , I_M or I_L .

Supply voltage V_{mm} and winding characteristics both determine the value of $t_{off(min)}$.

Figure 11 : Winding Current @ $T_{OFF(MIN)}$.

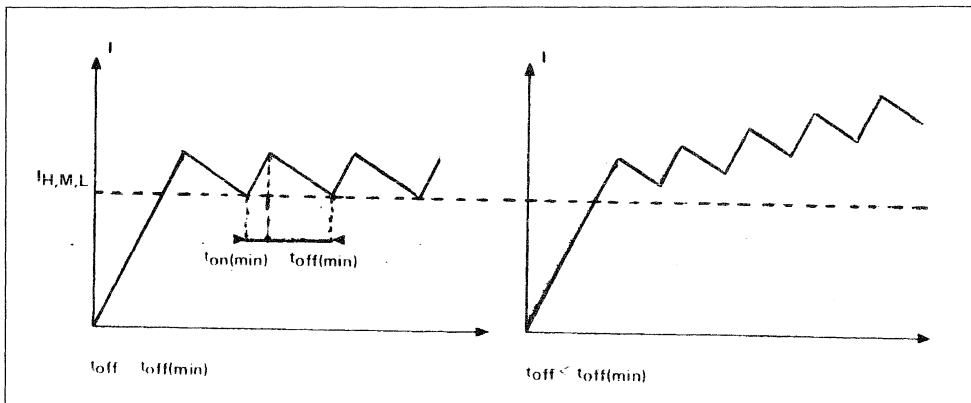
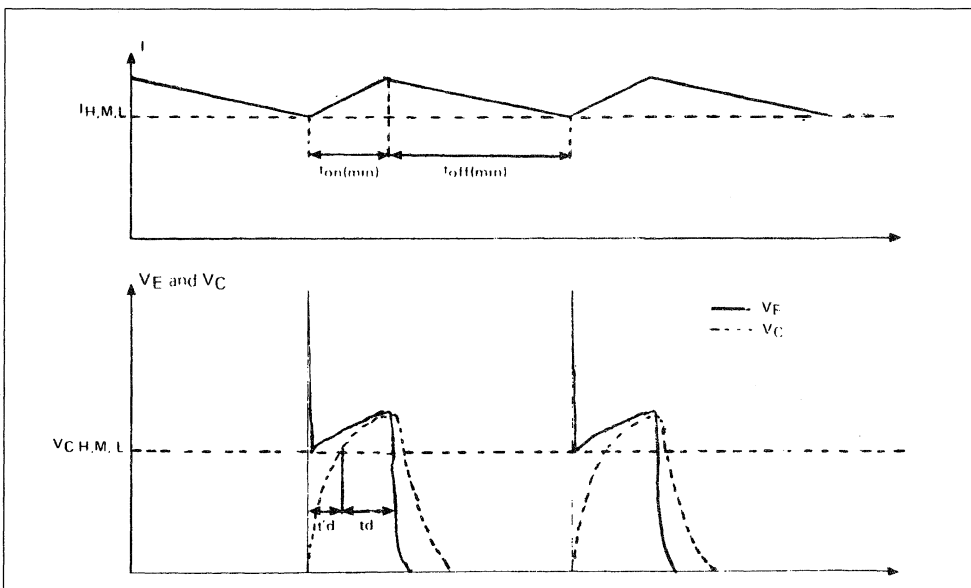


Figure 11 Bis : Winding Current, V_E and V_C Voltages @ $T_{OFF(MIN)}$.



SELECTION OF R_S VALUES

Three values of motor current I_H , I_M and I_L are determined by the choice of R_S and V_R values.

The value of R_S is calculated such that $V_{CH} = R_S \cdot I_H$
 where $V_{CH} = \frac{0.42}{5}$

V_R and I_H is the maximum motor supply current.

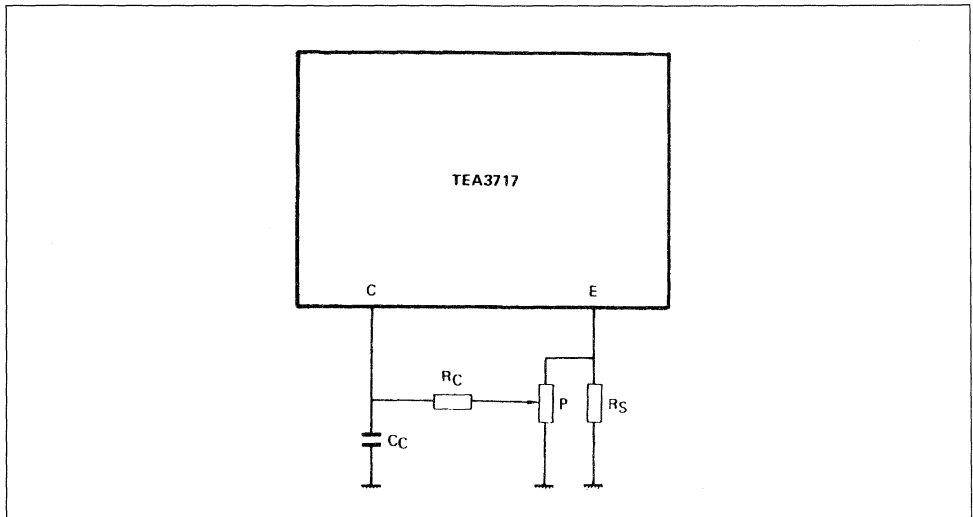
A choice of R_S value around 1Ω will guarantee a fast increase of the winding current and offers the possibility of operation with a voltage around 5 V for V_R , and thus is suitable for most applications.

It is also possible to vary the motor current in a continuous mode :

- by V_R adjustment
- by feeding back a portion of the voltage drop across R_S through a potentiometer whose wiper is connected to the comparator input.

In order to minimize the differential voltage $V_E - V_C$ due to comparator's input current, care must be taken to avoid the appearance of a large impedance between E and C terminals. Appropriate values of P and R_C would be : $P = 1\text{ k}\Omega$ and $R_C = 470\Omega$.

Figure 12 : Continuous Variation of Current Level.



CABLING

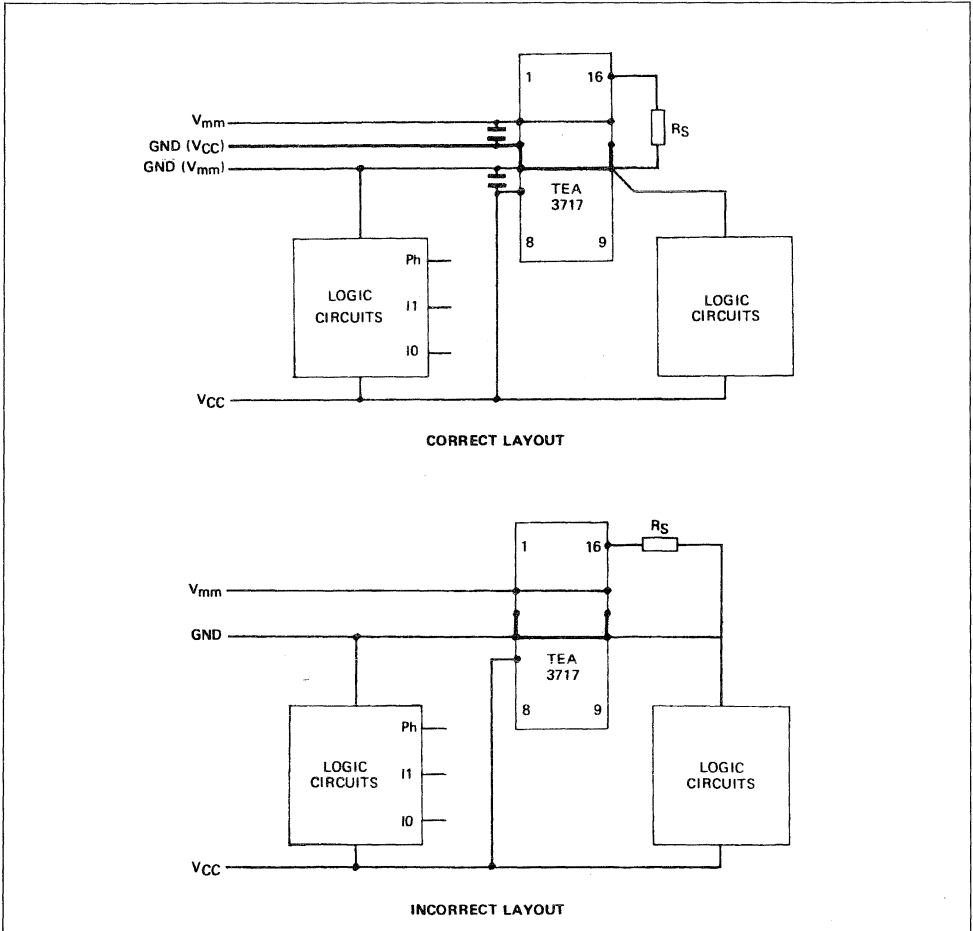
Since the TEA3717 operates in switch mode, it is essential to take particular cabling precautions so as to avoid the generation of interferences susceptible to disturb the correct operation of the control electronics.

Recommended precautions are :

- Separated ground connection for V_{mm} supply

- Connection link between RS and the TEA3717 must be kept as short as possible
- Decoupling of V_{mm} by a ceramic capacitor (15 to 150nF) directly connected to the TEA3717 and also by an electrolytic of higher value : 10 to 22 μ F.
- Decoupling of V_{CC} .

Figure 13 : TEA3717 PC Board Layout.



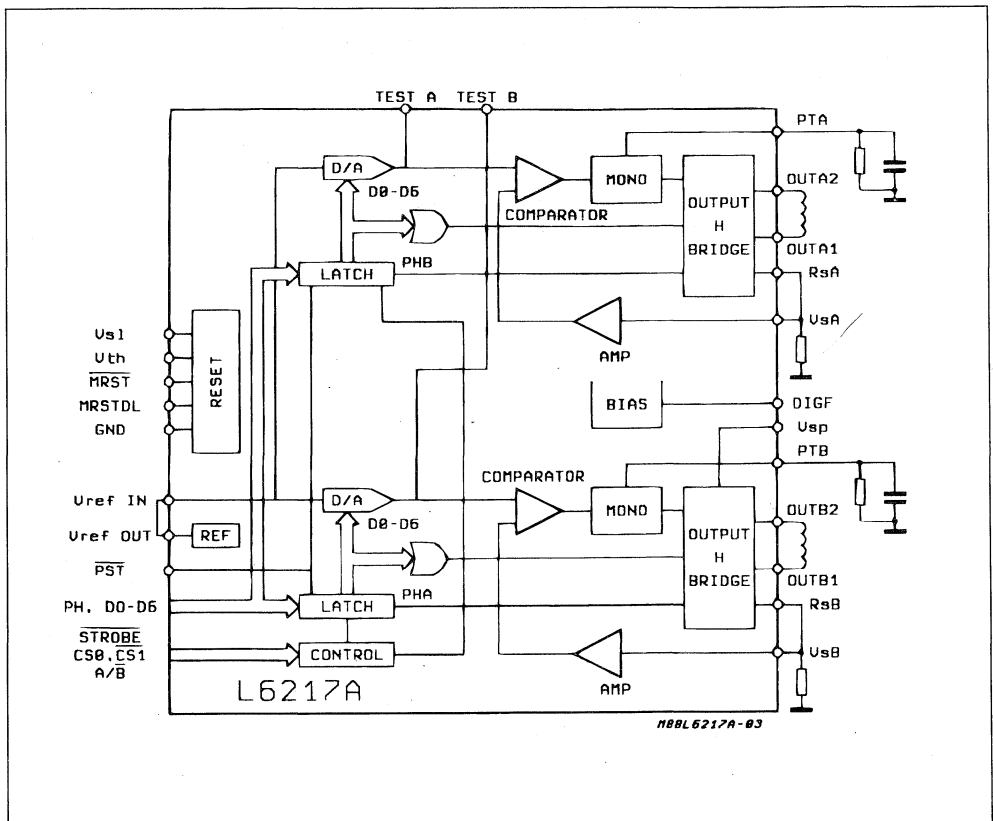
EFFICIENT MICROSTEPPING AT HIGH CURRENT

by T.L. Hopkins and A.O. Massimini

There is increasing demand for motor control systems which require precise current control for microstepping or for adjusting the current profile. These systems depend on a microprocessor proportionally controlling the current in each winding. This has been implemented in low current applications with the L6217A [1]. For high current applications the L6217A is used as a controller for an external power driver. This note will discuss the L6217A combined with the L6202 and the L6203, H-bridges in multipower BCD technology.

The L6217A is designed with all the blocks required for implementing a frequency modulated current drive for both coils of a bipolar stepper motor (figure 1). It can directly interface with a microprocessor. The output H-bridges are each capable of delivering 500mA. For higher current applications, the output H-bridges are driven off 5V logic and are used for switching signals to an external H-bridge. Using an H-bridge driver in Multipower BCD technology with power DMOS outputs, higher maximum current is possible: 1.5A with L6202 and 3.0A with L6203 [2].

Figure 1 : Block Diagram L6217A.

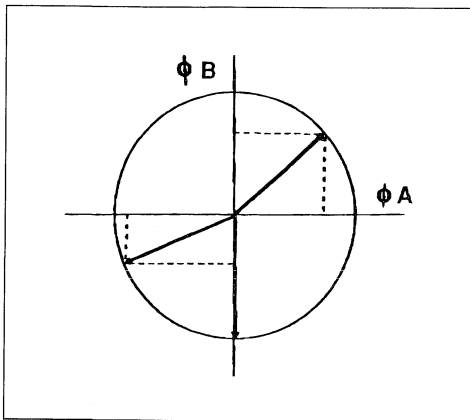


MICROSTEPPING

Basically, microstepping is achieving finer electrical resolution than is afforded by conventional full-step and half-step driving. The precision is dependent on the level of resolution of a digital to analog converter (D/A) and the number of current levels desired. Also, the mechanical characteristics of a motor in response to these current levels is a factor. Just because you might be able to achieve 256 current levels (microsteps) between two full step positions electrically, does not necessarily translate to 256 microsteps mechanically.

Microstepping can help smooth out the mechanical action of a stepper motor as well as improve the torque profile. Torque is proportional to the current in the motor windings which are proportional to the magnetic flux. One can imagine the windings aligned along the axis of an X-Y co-ordinate system. The resultant torque is the vector sum of the individual torques produced by phases A and B. The direction is determined by the direction of current flow (figure 2). The ideal situation would be for the resultant torque to fall on the unit circle for all positions. This would occur if the winding currents are orthogonal functions, such as sine and cosine.

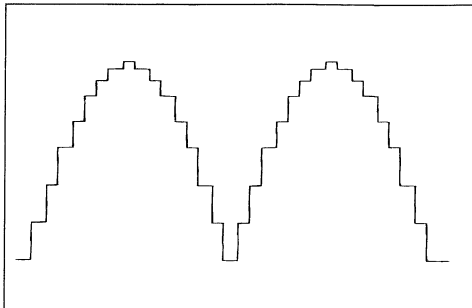
Figure 2 : Microstepping.



In a microprocessor controlled system these functions can be digitized and stored in a look-up-table (LUT). Usually the magnitude of the function is sufficient, software can take into account the direction. Figure 3 is a digitized rectified sine wave. Depending on software implementation, one could store in LUT only a portion

of a symmetrical waveform. The current waveforms can be modified to take into account motor resonances and damping [3] [4].

Figure 3 : Phase Current Magnitude.



DIGITAL INTERFACE

One important aspect of intelligent power devices is the ability to interface the devices to digital control circuits. The L6217A includes two data latches that can be easily interfaced to a microprocessor, either to an I/O port or directly on the data bus of the system [5]. Using these two latches the microprocessor can independently set both the level and direction of current flow in each winding of the stepper motor. Each of the two latches are loaded with a 7-bit value for the D/A converter (D0-D6) and one bit of phase information (PH) that controls the direction of current flow through the output bridge. This current value can be viewed as an 8-bit word with the MSB being PH as the sign bit. The latched information is then fed to the internal control circuitry which performs a closed loop current control.

D/A CONVERSION

Conversion of the digital information in the latch to an analog signal that sets the current level is performed by a pair of 7-bit D/A converters. Each D/A employs a current switching approach that switches binary weighted currents on and off of the output in response to the digital information. With this technique the D/A's have an output settling time of less than 2μs. The D/A output current is then converted to a voltage and applied to the current sense comparator input. To facilitate testing, the D/A output voltage is also available on external pins, TESTA and TESTB.

An additional function in the data conversion section is a circuit that disables the output bridge when the D/A input is 00 (Hexidecimal). With this circuit, the output is immediately tristated when the microprocessor commands zero current and the winding current decays with a fast di/dt. When the output bridge of the L6217A is used for switching signals to an external H-bridge this function is not directly available. Other methods for disabling the external H-bridge will be discussed below.

CURRENT CONTROL

The current control technique chosen for the L6217A employs Frequency Modulation switching control. This technique was chosen to minimize the power dissipation in the device and gain fast rise times that can be achieved only with switching techniques. Frequency Modulation was chosen over a fixed-frequency Pulse Width Modulation (PWM) technique which can exhibit some stability problems if the switching duty cycle exceeds 50%.

As implemented in the L6217A the current control section senses the current by monitoring the voltage across the two current sense resistors, Rsense1 and Rsense2. This voltage is then compared to the output of the D/A converter by the internal comparator. To minimize the voltage drop and power dissipation in the sense resistors, the sense voltage is amplified before it is compared to the D/A output. The peak current set by the device is given by equation 1.

$$I_{mp} = \frac{V_{ref}}{4.69 * R_{sense}} * \frac{D}{128} \quad (1)$$

Where = V_{ref} = Reference voltage
 R_{sense} = Sense resistance
 D = Digital data in (0-127)

When the bridge is energized the current in the motor winding will rise, limited by the L/R time constant of the motor winding, until it reaches the peak value set by the output of the D/A converter. When the peak current is reached, the comparator triggers an internal monostable that sets the off-time and causes the output to be switched into the recirculation mode. During recirculation only the upper transistor of the bridge is turned off while the lower transistor of the bridge remains on. In this way the current circulates in a loop that includes the sense resistor. This approach reduces the noise on the sense resistor since current is always present. At the end of the off-time, a new cycle is started, the H-bridge is enabled and the motor current starts to rise again.

An external parallel RC network to ground at the monostable defines the off time for that channel. This is determined by $T_{off} = 0.69 RC$.

To eliminate the need for external filtering in the current sense feedback required by many similar devices [5], the L6217A includes a digital filter circuit. This circuit consists of an internal monostable that inhibits the current sensing amplifier for a short time after the bridge is enabled. In this way the voltage spike that appears on the sense resistor is digitally masked, preventing a false trigger of the current control section. The default time of the digital filtering window is typically 2μs and can be modified with an external resistor if required. The digital filter pin (DIGF) is usually left open. The voltage at this pin is typically 0.7V. To increase the time of the digital filter current may be injected into the DIGF pin up to a maximum of 20μA. If the resistor is connected to logic voltage, 5V, the minimum value is 215Kohm. A resistor to ground will decrease the time.

In some applications a nonlinearity of the transfer function occurs at low current values. This nonlinearity is due to the minimum duty cycle achievable in the application. The minimum duty cycle is fixed by the minimum on time, which is the sum of the propagation delay from the current sense comparator to the output stage plus the digital filter time, and the off time set by the monostable. In some applications where there is a low back EMF, as will occur when trying to hold a position and the Vemf becomes zero, or high supply voltage, the minimum duty cycle can set a current level that is above the desired current level set by the D/A converter. For a given duty cycle the minimum current achievable in the motor is given by equation 2. This equation is applicable whether one uses either the L6217A H-bridge or an external H-bridge.

$$I_m = \frac{(DC) (V_{cc}) + (DC-1) (V_d) - (DC) (V_{su}) - V_{emf} - V_{sl}}{R_{motor} + R_{sense}} \quad (2)$$

Where : V_{cc} = Supply voltage
 V_d = Forward voltage drop of recirculation diode
 V_{sl} = Saturation voltage of lower output device
 V_{su} = Saturation voltage of upper output device
 V_{emf} = Average back EMF voltage of the motor
 DC = Output Duty Cycle, $T_{on}/(T_{on} + T_{off})$
 I_m = Average motor current

Two techniques may be used to minimize the effect of this behavior. First, the minimum duty cycle can be reduced by reducing the on time set by the digi-

power H-bridges like the L6202 or L6203, as shown in figure 4. In this application the outputs of the L6217A drive the logic inputs of the L6202 providing only control signals and not driving the motor directly. The application utilizes all of the control features of the L6217A. The L6202 is capable of delivering up to 1.5A RMS to each motor coil. If replaced with the L6203 each motor coil can be driven up to 3A RMS. By paralleling an L6203 with itself to form half an H-bridge and the same with another it is possible to achieve motor currents up to 6A RMS.

The internal block diagram of the L6202 and L6203 is shown in figure 5. The die is the same for each but is housed in different packages. The L6202 is housed in the Power-dip (12 + 3 + 3) and the L6203 is housed in the Multiwatt-15. The thermal characteristics of these packages determine the current capability of the driver [8] [9].

The L6202/3 is designed with Multipower BCD technology which allows the integration of Power DMOS elements, bipolar transistors, and C-MOS logic. Using this technology the L6202/3 is capable of ac-

cepting TTL or C-MOS compatible signals and is suitable for high efficiency, high frequency switching control of stepper motors. The maximum motor supply voltage is 48V.

The power stage of the L6202/3 consists of four DMOS N-channel transistors with $R_{DS(on)} = 0.3 \text{ Ohm}$. Each DMOS transistor has an intrinsic diode which can operate as a fast free-wheeling diode. Due to the very short turn-on and turn-off times characteristic of Power MOS devices a dead time of 40ns is provided to prevent a shoot-through current when switching direction of current flow from one side of the bridge to the other.

Like the L6217A the L6202/3 also has a thermal protection circuit which will disable the device if the junction temperature exceeds the set threshold.

The circuit shown in figure 4 can implement proportionally controlled or full step applications but cannot implement half step applications since the L6217A cannot provide the signal required to disable the L6202. As previously noted this signal is generated

Figure 5 : Block Diagram L6202/L6203.

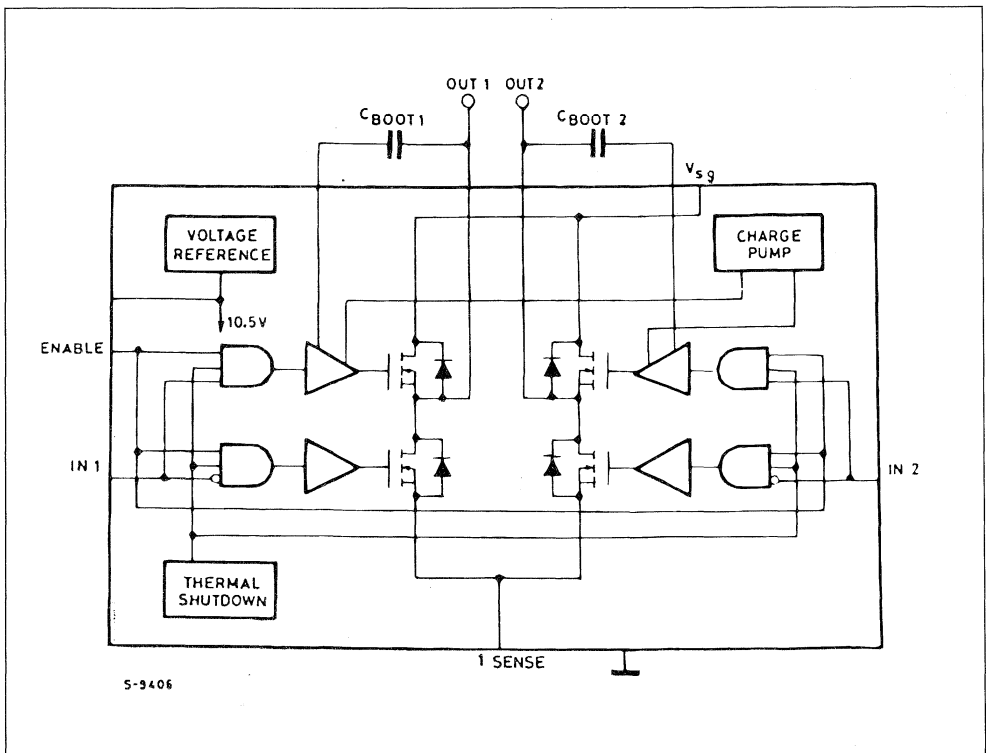
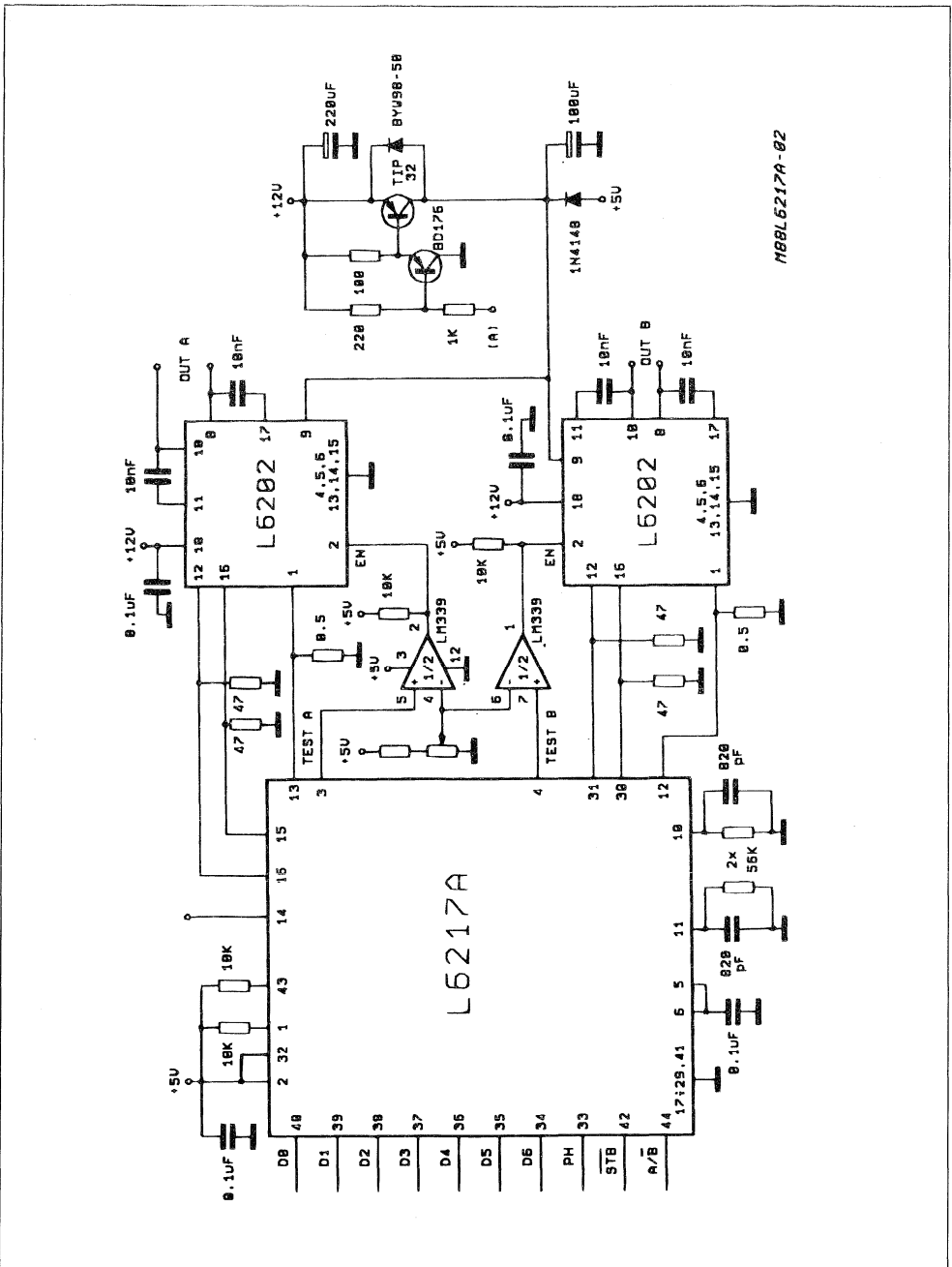


Figure 6 : Applications of L6217A Using Voltage Comparators.



within the L6217A for its internal H-bridge. For half step or applications requiring the output bridge to be disabled, the enable of the L6202 must be controlled. Two possible configurations can be used : 1) an additional signal may be brought from the microprocessor for each of the L6202 enable inputs, or 2) a sensing circuit may be added to sense when the output should be disabled. Figure 6 shows an application where a pair of comparators are connected to the test pins (D/A outputs) of the L6217A to sense when the output of the D/A converter is less than one LSB. These comparators then disable the L6202's when a current of 0 is set by the microprocessor.

The circuit in figure 6 also implements a dual level power supply for the output stage. In this circuit the power supply applied to the output bridge can be switched from the high voltage, when terminal (A) is pulled low, to the lower voltage by the control logic. This arrangement overcomes the problem of a minimum current level due to the fixed minimum duty cycle of the L6217A by lowering the supply voltage when low level currents are required.

In this application an external 12V is applied to the V_{ref} pin of the L6202. Usually only a small capacitor is required. The V_{ref} is internally generated from V_s and supplies the internal logic. If V_s is less than 12V the V_{ref} will be too low. For the dual power level application shown an external V_{ref} is supplied.

SUMMARY

For stepping motor drive applications requiring proportional current control, the L6217A can provide the complete interface between the microprocessor and motor in low power applications. For higher power applications the L6217A may be used as a controller IC for an external bridge like the L6202/3.

Using these devices proportional current control systems can be easily and compactly realized.

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SMART POWER DUAL BRIDGE MOTOR DRIVER

by Pierre PAYET-BURIN and Gilles TROUSSEL

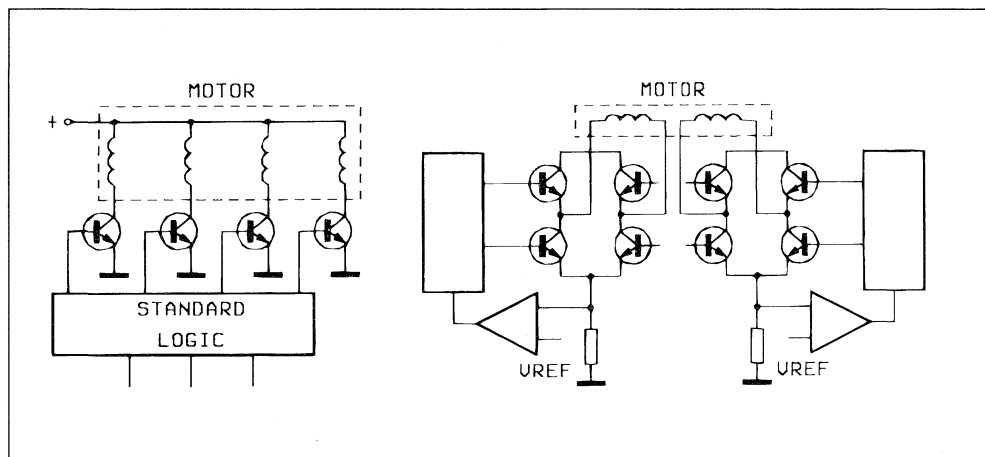
THREE GENERATIONS

During the past few years, the development of micro-processor based systems has enhanced the need for power drivers interfacing these systems to their load.

Especially in the stepper motor field, single chip integrated circuits now replace discrete component boards.

Discrete transistors were the first generation of power interfaces and a control system required many components (fig 1).

Figure 1.



Unipolar motor (the easiest to drive) was the first to be used whereas bipolar motors were limited to applications where the component cost was not critical.

Second generation of power interfaces were partly integrated solutions (fig 2).

Darlington arrays like L702 eased the design of unipolar motor controls but some specific problems, like the number of switches to be integrated and therefore the power to be dissipated slowed down the development of IC for bipolar stepper motor control applications.

For these motors, semiconductor manufacturers offered different answers :

- integrating a complete driving stage for half a motor (TEA3717) ;
- dedicating one chip to power and another to logic control ;
- fully integrated solution, but without switch mode control features.

Third generation IC : fully integrated solutions where a single chip offers all the control features originally developed for unipolar stepper motor, we now propose the UAB4718, a one-chip switch-mode control circuit for bipolar stepper motors (fig 3).

Figure 2.

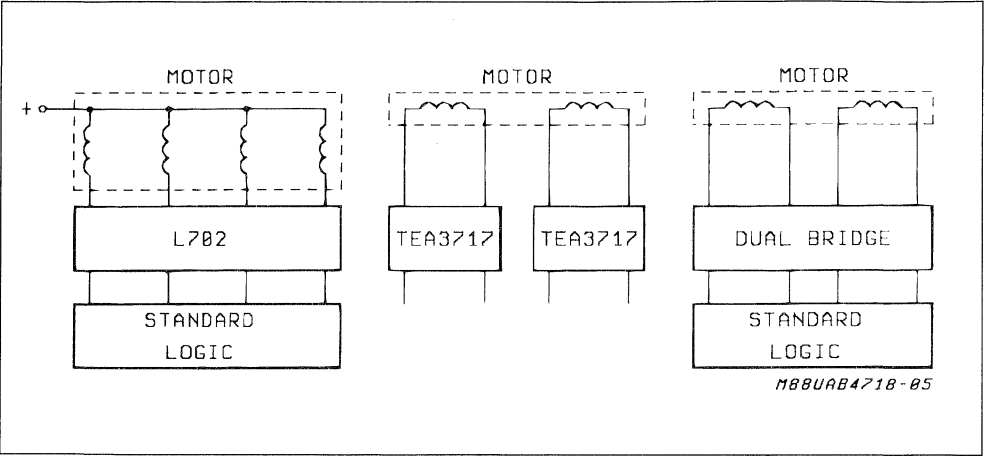
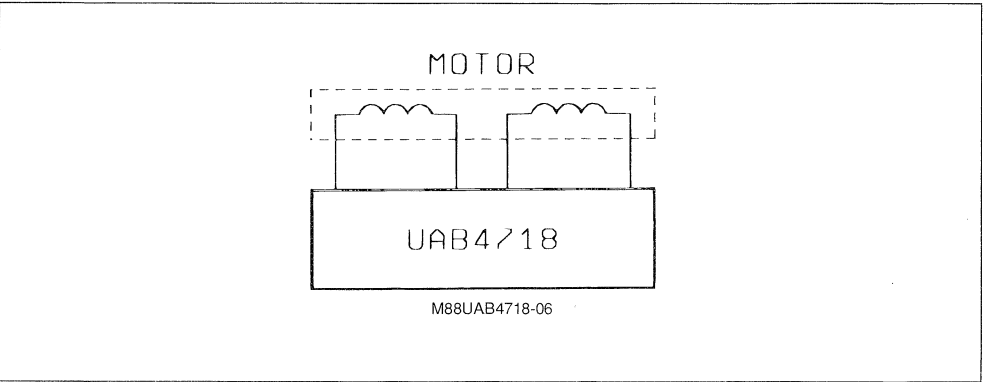


Figure 3.



CIRCUIT DESCRIPTION (fig 4)

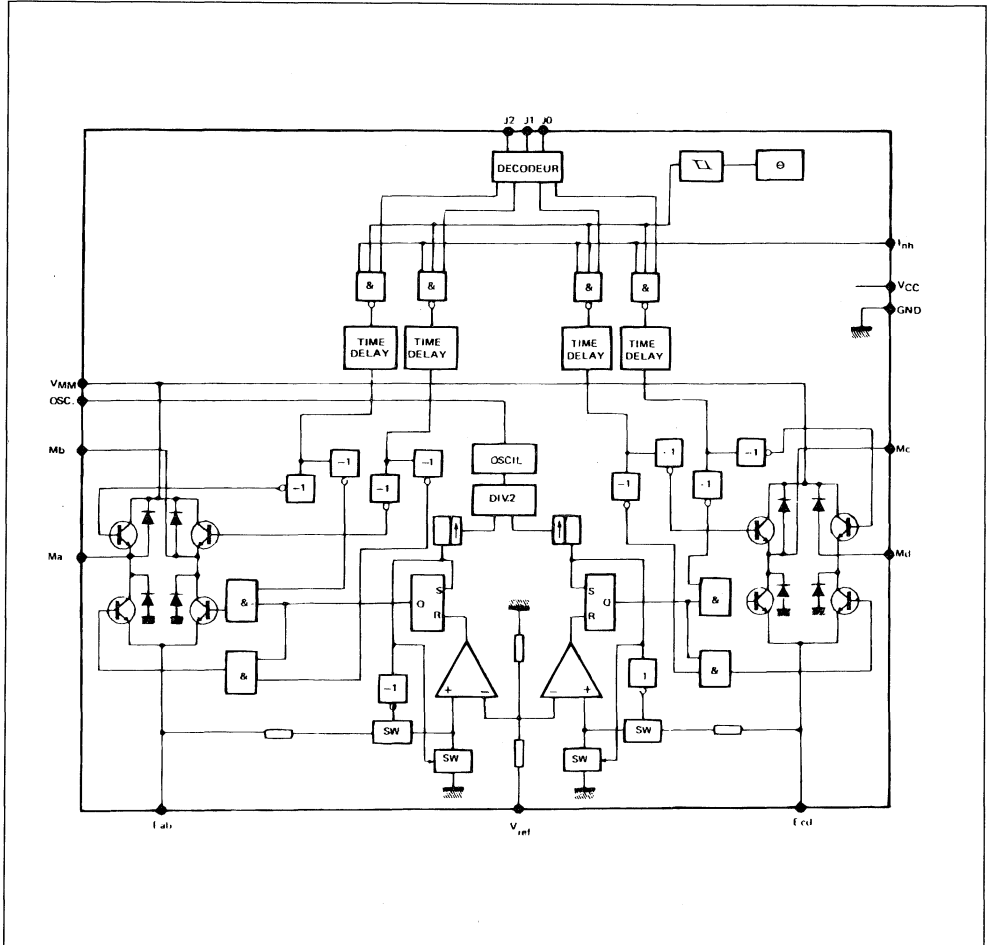
The new UAB4718 integrates two full H bridges with switch-mode control functions and offers the following features :

- Low power dissipation
- Good integration logic density and minimum number of logical inputs

- Fixed frequency switching
- Minimum number of external components
- Safety functions

To meet all these requirements, we used the newly developed Bimos technology and some original solutions.

Figure 4.

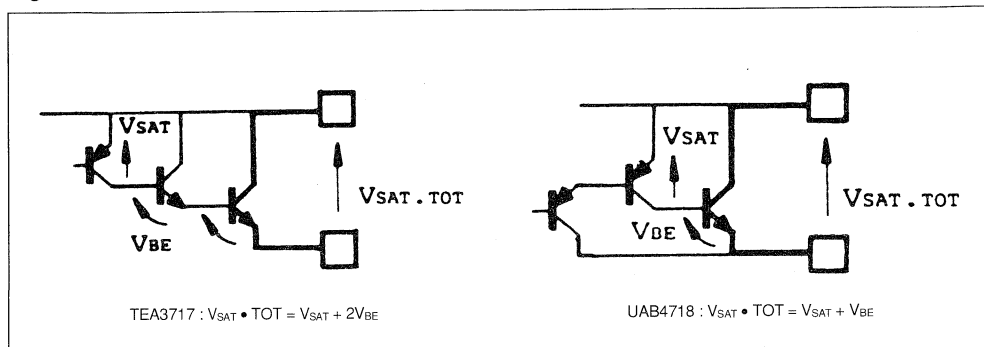


LOW POWER DISSIPATION

The power stages use the bipolar NPN transistors of the Bimos technology. They withstand 60V as V_{CE0} with a maximum leakage current of 100 μ A.

Versus the classical TEA3717, the H bridges have been redesigned to reduce the saturation voltage and, as a result, the dissipation.

Figure 5.



GOOD INTEGRATION LOGIC AND REDUCED NUMBER OF LOGICAL INPUTS

Because of the high density and the low consumption of the CMOS logic of the Bimos technology, it has been possible to integrate a complete control logic without increasing the power dissipation or the die area.

The two bridges are controlled by a decoder : three pins are sufficient to select the 8 combinations of currents in the motor windings needed for half or full step mode.

An inhibition signal (low active) and an integrated thermal protection can switch off the two output stages with a fast current decay in the windings.

Internal time delays avoid cross conducting when current is reversed.

All inputs are CMOS compatible with $5V \pm 10\%$ supply voltage.

FIXED FREQUENCY SWITCHING

Many solutions permit switch-mode current regulation :

- **PWM** : an image of the average current is fed to an error amplifier and modulates the conduction period. This method has fixed frequency, good precision but requires many components : it therefore cannot be used in our application.

For the source transistor, a PNP-NPN arrangement now replaces a NPN darlington and its PNP driver (fig 5). The later solution requires a larger area (about twice as large) because of the lower current density of the PNP transistors.

- **Fixed cut-off time** : the bridge is disabled for a fixed duration when the current exceeds a reference level. This system is simple but the switching frequency is not stable.
- **Fixed period** : the bridge is disabled when the current exceeds a reference level and it is switched on at a fixed frequency. This system has been chosen for UAB4718 because it is simple and the fixed frequency system solution can synchronise the two H-bridges.

DESCRIPTION

An external capacitor sets the oscillator frequency (up to 100kHz). This frequency is divided by two and generates pulses that alternately switch on each bridge to avoid high inrush currents.

The switching frequency can be calculated as follows :

$$f \text{ (KHz)} \approx 70/C(\text{nF})$$

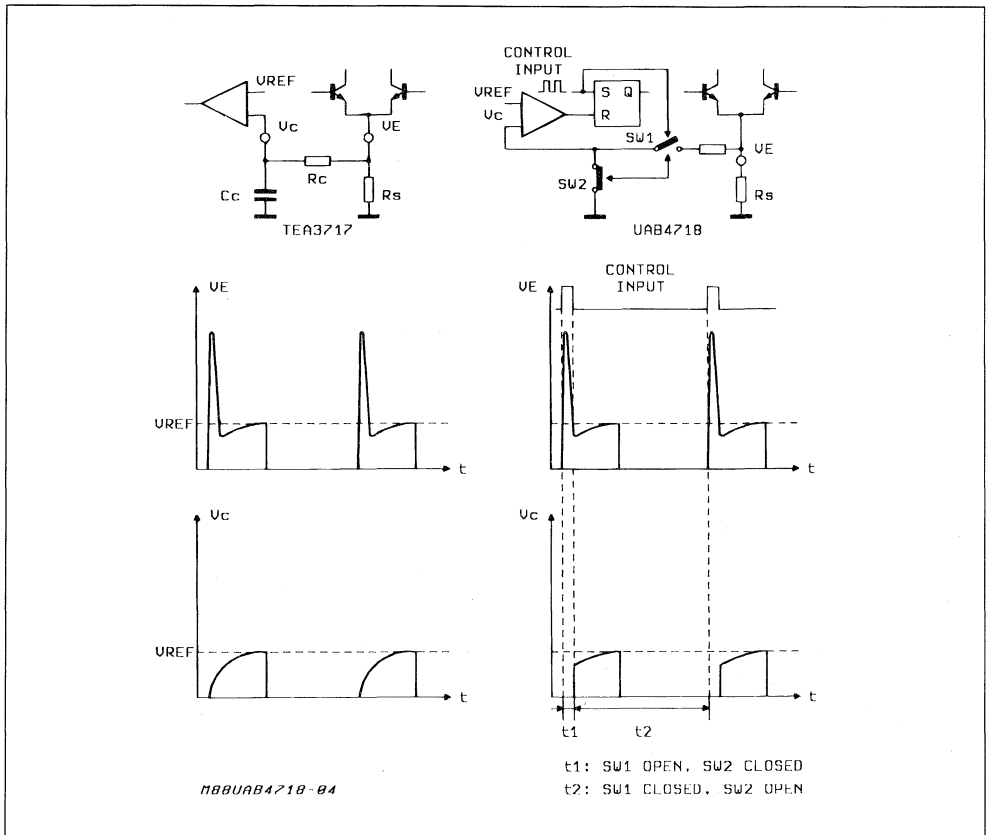
MINIMUM NUMBER OF EXTERNAL COMPONENTS

The number of external components has been reduced by the utilization of a single capacitor for the oscillator and by suppressing the classical RC filter between the sensing resistor and the comparator inputs.

A MOS switch prevents the current spikes at turn-on from triggering the comparator. At turn-on, its input is short-circuited to the ground during the spike (fig 6).

In addition, a small RC filter has been integrated to improve noise immunity. This was feasible because the comparators were designed with PMOS transistors which show very high impedance.

Figure 6.



SAFETY FUNCTION

It is important to preserve the power drivers in case of over-heating. An internal protection (low active) with a hysteresis switches off the two H bridges on detection of an over temperature in the chip. When the temperature decreases, the H bridges are switched on.

Table 1a : Full-step Rotation.

Step	J2	J1
0	0	0
1	0	1
2	1	0
3	1	1

JO = 0 : mode Two phase drive

JO = 1 : mode One phase drive

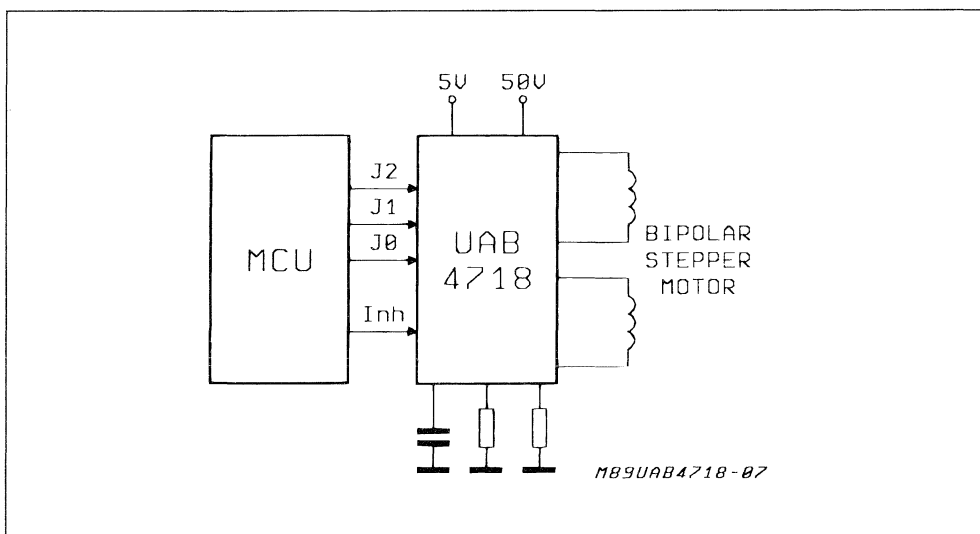
OPERATION

A complete application can be built with a single IC and 3 external components (fig 7).

Table 1b : Half-step Rotation.

Step	J2	J1	J0
0	0	0	0
.5	0	0	1
1	0	1	0
1.5	0	1	1
2	1	0	0
2.5	1	0	1
3	1	1	0
3.5	1	1	1

Figure 7.



The stepper motor drive circuit is driven according to the tables = 1a and 1b.

Fig 8 gives the general operation of the circuit : current direction in the windings is selected with J1, J2, J0 inputs while the oscillator generates the pulses for switch-mode current regulation.

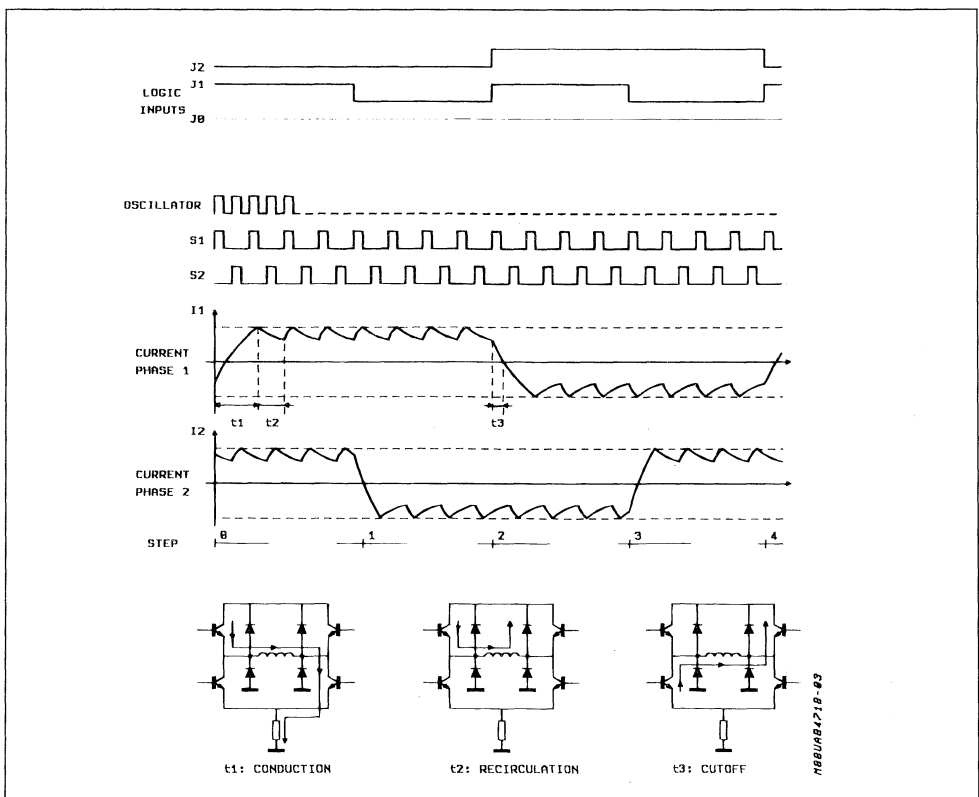
Versus the classical solution with two TEA3717, the number of components and the power dissipation have been considerably reduced due to the design of the chip.

Table 2.

Phase Current	Two Phases Driven	One Phase Driven
Without Heatsink	0.4A	0.7A
With Heatsink (10°C/W)	0.9A	1.5A

	Today Solution	UAB4718
I_{CS}	2	
Resistances	6	
Capacitors	4	
Diss. Power (2 x 400mA)	4W	2

Figure 8.



SHORT CIRCUIT PROTECTION ON L6203

By G. SCROCCHI and G. FUSAROLI

With devices like L6203 used as driver often interfacing the external world by means of wires, can be easy to have short circuits.

A short circuit can occur for many reasons : a short on the load, a mistake during the connection of the wires between the device and the load (i.e. L6203 driving a motor), an accidental short between the wires and so on.

The outputs of L6203 are not protected against the short circuit and if a short occurs, the big amount of current flowing through the outputs can destroy the device.

To avoid this risk can be useful to add a circuitry to protect the device : in this case, to have a total protection, we must consider three types of short circuit :

- 1 - output to output short circuit
- 2 - output to supply voltage short circuit
- 3 - output to ground short circuit

The first step is to sense the short circuit current.

In output to output (fig 1) or output to supply (fig 2) short circuit can be used the sensing resistor (R_{SL}) already used to set the current flowing in the load during the normal operation.

Figure 1.

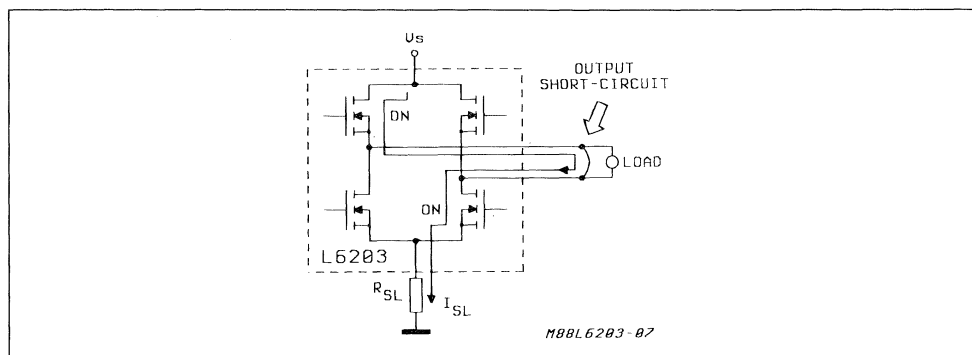
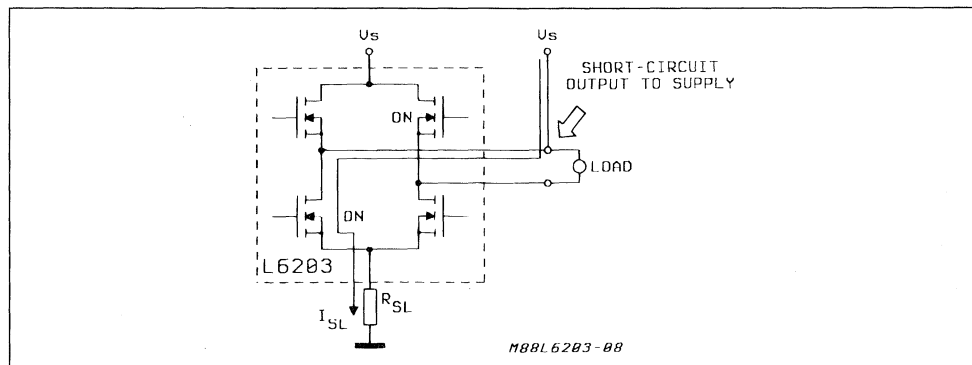
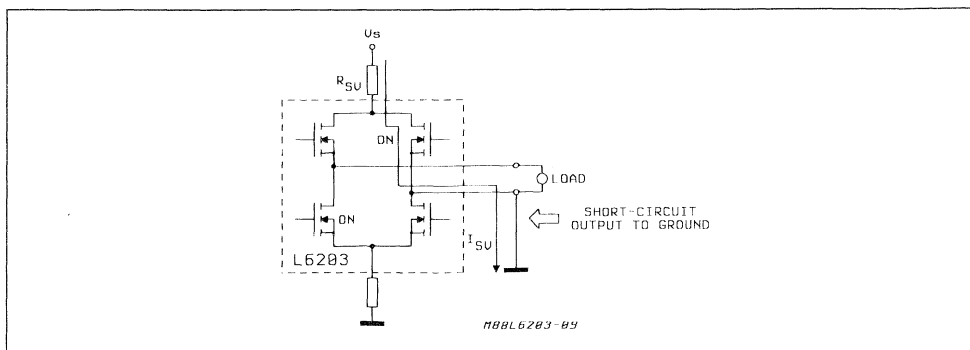


Figure 2.



To sense the output to ground short circuit (fig 3) another sensing resistor (R_{su}) must be added between the supply pin and the supply voltage.

Figure 3.

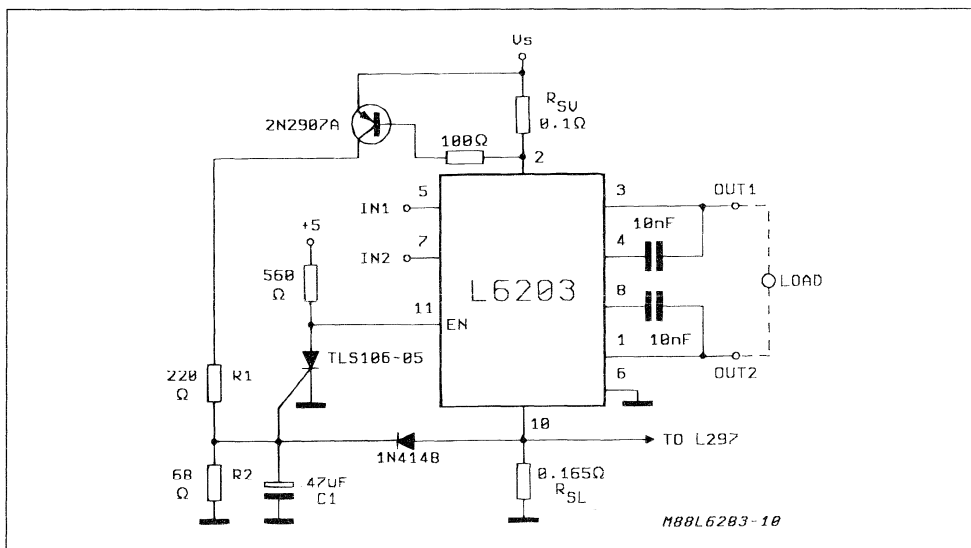


The second step is to create a threshold over which the value of the current must be considered as short circuit : for this way a transistor or a diode could be used.

The complete protection will be given by the ' or ' of

the signal coming from the upper and the lower sensing circuitry ; this signal can be used to act on the ENABLE pin of the L6203 disabling the output stages. A complete protection schematic diagram is shown in fig. 4.

Figure 4.



In normal operation the circuit works up to 3A/40V. When a short circuit occurs the SCR is triggered and L6203 disabled : due to the SCR memory L6203 is kept disabled until the power is switched off and then on, if the cause of short was removed.

The short circuit is detected when :

$$I_{SU} > \frac{V_{BE(T1)}}{R_{SU}} = \frac{0.6}{0.1} = 6A$$

$$I_{SL} > \frac{V_D + V_{THSCMT}}{R_{SC}} = \frac{0.6 + 0.7}{0.165} = 7.8A$$

The effective short circuit peak current is greater than I_{su} and I_{sl} : this is due to the high dI/dT during the short and to the delay between the short circuit detection and the **ENABLE** intervention :

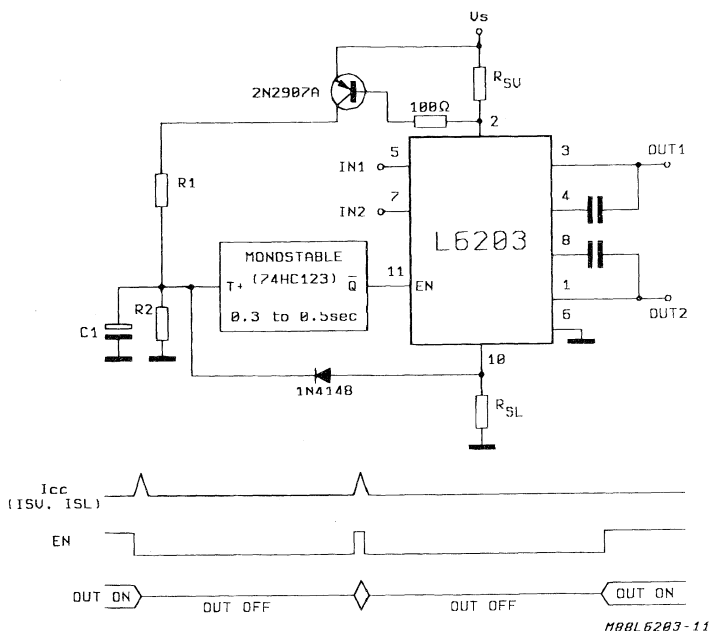
R_{su} and R_{sl} must be non inductive resistors.

R1 and R2 are used to scale the signal when the transistor goes on and in conjunction with C1 to filter the short circuit signals in order to avoid false trigger of the SCR : this filtering should not be too much heavy to avoid to introduce an excessive delay in the short circuit loop.

Isu and Isl must be calculated at the effective operating temperature being the Vbe and Vd temperature dependent.

Instead of the SCR, a monostable with a long time constant ($0.3 \div 0.5$ sec) can be used : in the case, every time a short circuit occurs, L6203 is disabled for the monostable time constant and then enabled, if the short is still present L6203 is disabled again, if the short was removed L6203 returns in normal operation (fig 5).

Figure 5.



$R_1, R_1, C_1, R_{SU}, R_{SL}$ are chosen depending on the application.

The intervention of the protection circuit is determined by

$$I_{SU} > \frac{V_{BE}}{R_{SU}}$$

$$V_D = V_{\text{DIODE}}$$

$$V_{IH} = \min V_{\text{Input High T+ Monostab}}$$

$$I_{SL} > \frac{V_{IH} + V_D}{R_{SL}}$$

CONTROLLING VOLTAGE TRANSIENTS IN FULL BRIDGE DRIVER APPLICATIONS

by Thomas L. Hopkins

In applications that involve fast switching of inductive loads, designers must consider the voltage transients that are generated in such applications. To insure a reliable design, the voltage transients must be limited to a level that is within the safe operating conditions of the switching device. This application note discusses the sources of voltage transients in full bridge applications and techniques that can be used to limit these over-voltage conditions to safe levels. Special attention will be given to applications using monolithic implementations of full bridge circuits like the SGS-THOMSON L6202 and L6203.

MAXIMUM RATINGS

The maximum voltage rating for the bridge driver can be derived from the maximum ratings of the devices used in the output stage and are generally the BV_{CE0} or BV_{DSS} of the power devices. In addition to the maximum allowable voltage across the output device, additional limits may be needed on the maximum output voltage above supply or below ground, depending on the implementation of the output stage.

As an example of a full bridge circuit, consider the SGS-THOMSON L6202 and L6203. These devices are full bridge drivers implemented with DMOS transistors on a monolithic structure. Using these devices full bridge drive circuits, like shown in figure 1, are easily implemented. The device has a maximum rating for the supply voltage of 60V, which implies a maximum BV_{DSS} for the output devices of 60V. In addition, due to the monolithic implementation, the voltage between the two output terminals must not

exceed 60V. Therefore, the maximum ratings that must be considered for the application are :

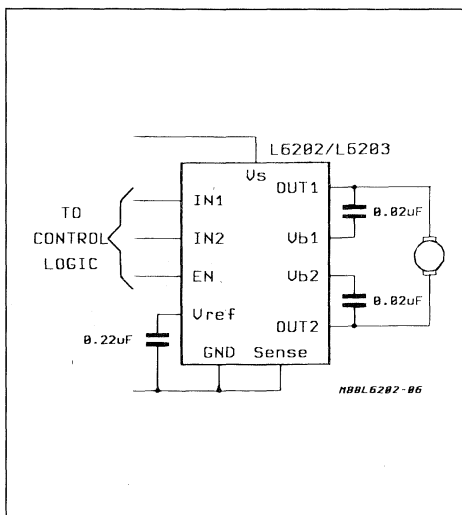
V_{supply} 60V

V_{ds} any output 60V

$V_{01} - V_{02}$: 60V

Similar maximum ratings will exist for any full bridge application, with the exception of the differential output voltage limit, which will not exist for discrete implementations.

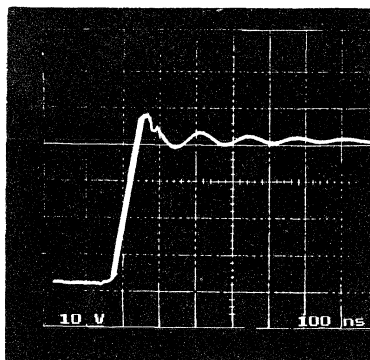
Figure 1 : DC Motor Drive Circuit using L6203.



SOURCES OF VOLTAGE TRANSIENTS

To protect against the over-voltage that may occur as a result of the inductive property of the load, voltage clamps are normally employed to limit the voltage across the output devices. In bridge applications these clamps are normally a diode bridge that clamps the voltage to one diode drop above supply and one diode drop below ground. However, if the diode switches slower than the transistor, there is a short time where neither the transistor nor the diode is conducting and the voltage rise is limited only by the capacitance on the node. The result is that a voltage overshoot occurs during the time before the diode turns on. When the bridge is built with DMOS power transistors, the intrinsic body diode is often used as the clamp. This is true for the L6202 and L6203. As can be seen in the figure 2, the turn-off time of the DMOS device in the L6203 is in the range of 25 to 50nS while the turn-on time of the intrinsic drain to source diode is in the range of 150nS. This difference in switching time is characteristic of many DMOS devices.

Figure 2 : Output Switching Waveform for L6203.

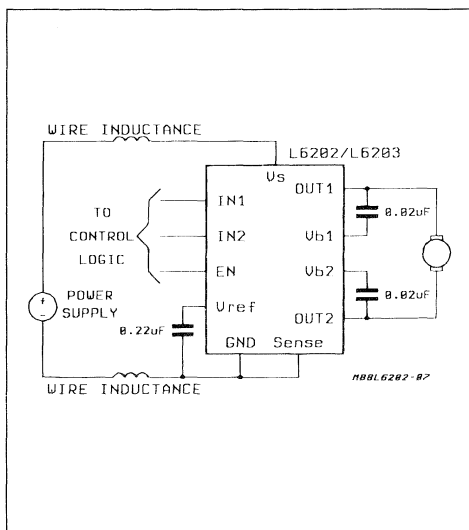


The second main factor contributing to the transients is the parasitic inductance in the wiring or printed circuit board layout. Figure 3 shows the parasitic inductances in the DC motor application. When

the current flowing in these parasitic inductances is rapidly switched, the inductive property of the wire causes a voltage transient. When large currents are rapidly switched, as with DMOS transistors, large voltage transients can be induced across even small parasitic inductances. For an inductive load driven by an H-Bridge the change of current in the power supply lead is equal to twice the load current when the bridge is switched off or the bridge is switched from one diagonal pair of transistors being on the other pair. Here switching the bridge results in a change of direction of current flow in the power leads. The time that it takes to switch the current is essentially the turn off time of the output device. In this case the resulting voltage across the inductance is given by the equation :

$$v = L \frac{di}{dt} = \frac{L_2 \times I_1}{T_{off}} \quad (1)$$

Figure 3 : Parasitic wiring Inductances in DC Motor Drive Circuit.



In fast switching applications, like the L6202, where the switching time is as short as 25nS, the induced voltage spike can become quite large. For example if the DC motor in figure 3 was driven with 4A and the bridge was switched off, a parasitic inductance of only 15nH would produce a 5V spike. Since the current is reversed in both the supply and ground leads the device would see a 10V spike between the power supply pin and chip ground, if the inductance of both wires were the same.

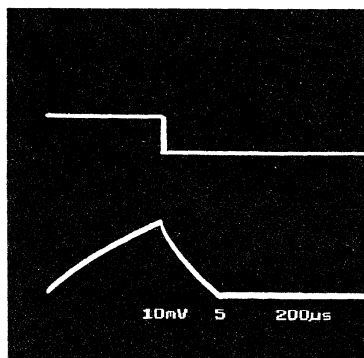
As a design example, consider a DC motor driver shown in figure 1 with the following system characteristics :

Supply Voltage Max 46V
 Min 38V

Peak Motor Current 5A

Chopping Frequency 50kHz

Figure 4 : Enable Input and Motor Current for Examples.



For evaluation, the motor will be driven with a peak current of 4A. Figure 4 shows the input signals for the L6202 and the motor current used in the evaluation.

Here the bridge is energized and the load current is allowed to build up to 4A. When the 4A peak is reached, the bridge is disabled and the current decays through the intrinsic diodes in the DMOS power stage. All figures in the remainder of this note are taken under these operating conditions.

POWER SUPPLY FILTERING

To reduce the effect of the wiring inductance a good high frequency capacitor can be placed on the board near the bridge circuit to absorb the small amount of inductive energy in the leads. It should be noted that this capacitor is usually required in addition to an electrolytic capacitor, which has poor performance at high frequencies.

Operating Voltages.

Figure 5a : Supply Voltage.

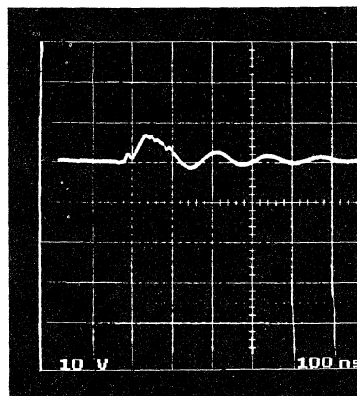
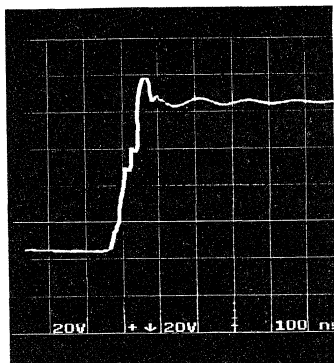


Figure 5a shows the spike on the power supply pin of the L6203 and the output pins when the bridge was disabled. These waveforms were present when the device was mounted on a printed circuit board where reasonable care was taken in the layout. When a 0.2 μ F polyester capacitor was connected between the supply and ground pin of the L6203 the voltage spike on the power supply was significantly reduced, as shown in figure 6a.

Figure 5b : V01 - V02.



Looking at the voltage waveform at the output terminals of the L6202, shown in figure 6b, a large spike is still present. The worst case spike is measured between the output terminals of the device ($V_{out1} - V_{out2}$) since the spikes above the supply and below ground are both present. After the voltage spike on the power supply was eliminated, the transients on the output must be related to the mismatch of switching times between the diodes and power transistors. To control these spikes two possible alternatives are present ; 1) use faster diodes, or 2) use an external circuit to slow the voltage rise time across the output when the transistors are turned off. Schottky diodes connected external to the L6203 would more closely match the switching time of the DMOS power transistors, but are expensive and require additional board space.

Operating Voltages with 0.2 μ F Bypass Capacitor on Supply Pin.

Figure 6a : Supply Voltage.

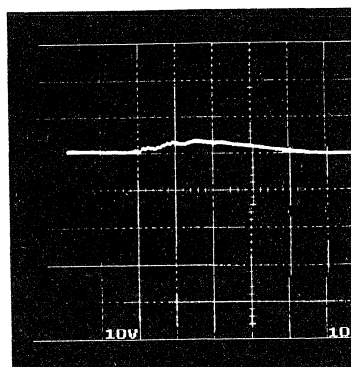
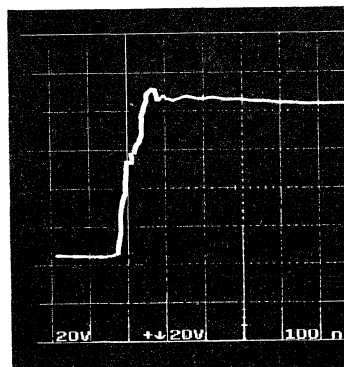


Figure 6b : V01 - V02.

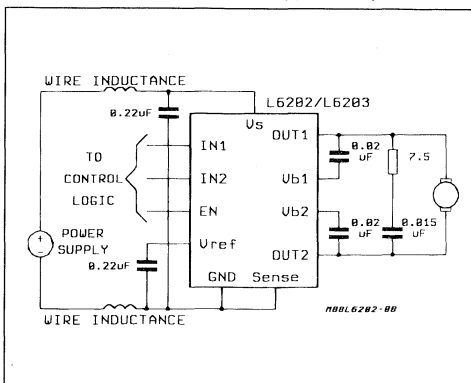


Slowing down the output voltage rise time can be accomplished by connecting a snubber network across the output terminals of the device. Figure 7 shows the connection for a RC snubbing circuit used with the L6203. With properly selected values the slope of the voltage waveform can be limited to where the diodes have sufficient time to turn on and clamp the remaining inductive energy.

SNUBBER DESIGN CONSIDERATIONS

The function of the snubber network is to limit the rate of change of the voltage across the motor (output terminals of the L6203) when one of the DMOS devices is turned off. Using the RC snubbing circuit shown in figure 7, the rate of change of the voltage on the output is dominated by the capacitor while the resistor is used primarily to limit the peak current flowing through the power transistor when it turns on.

Figure 7 : DC Motor Drive Applications with Snubber Network and Bypass Capacitor.



The time constant of the motor current is much longer than the switching time, due to the inductance of the motor. At the time of switching the DC motor can be assumed to be a constant current generator equal to the peak current at switching. If this

current is switched into the snubber, the voltage across the snubber network will jump to a value equal to the snubber resistance times the motor current. After the initial step, the rate of change is limited by the motor current charging the snubber capacitor.

To properly size the snubber network the resistor is selected such that the maximum motor current will produce a voltage less than the minimum power supply voltage. If the resistor is larger than this value, the snubber will be ineffective since the capacitor will not limit the voltage rise until the voltage has become greater than the power supply. For the design example, the maximum resistance for the snubber is given by the equation :

$$R_{max} = V_{smin}/I_{peak} = 38V/5A = 7.6 \text{ Ohm} \quad (2)$$

The snubber capacitor is calculated from the peak current and the target rise time. The capacitance is given by the equation :

$$C = I_{peak} dt/dv = 5A \cdot 150nS/50V = 0.015\mu F \quad (3)$$

When the snubber network is installed in the application the voltage transients on the terminals of the L6203 are greatly reduced, as shown in figure 8.

The drawback of a snubber network of this type is that a current spike will flow into the transistor when it is switched on as the capacitor is discharged. The theoretical peak value of this spike is given by the equation :

$$I = V_{smax}/R = 42V/7.5\text{Ohm} = 5.6A \quad (4)$$

Operating Voltages with Snubber Network and Bypass Capacitor.

Figure 8a : Sypply Voltage.

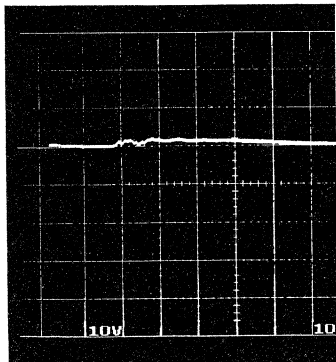
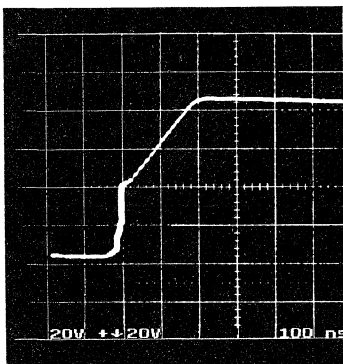


Figure 8b : V01 - V02.

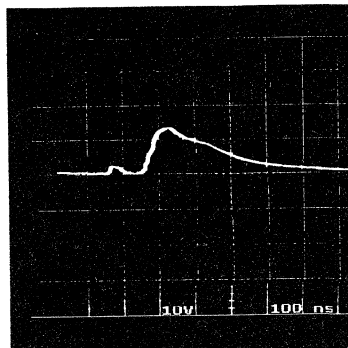


This peak current flowing in the snubber is added to the load current when the device is turned on and the total peak current in the transistor is the sum of

the snubber circuit current plus the load current. In practice the peak current measured is usually much less than the calculated peak, due to the capacitors internal resistance and inductance and the resistor inductance. Figure 9 shows the peak current in the snubber network in the design example.

Current in the Snubber Circuit.

Figure 9a : Turn on 2.0A/div.



The power dissipated in the snubber resistor is the sum of the dissipation during the turn-on and turn-off of the bridge. The resistor dissipation is :

$$P_d = (I_1^2 R DC) + (I_2^2 R DC) \quad (5)$$

where

I_1 = Current at turn-on

I_2 = Current at turn-off

R = Snubber resistor

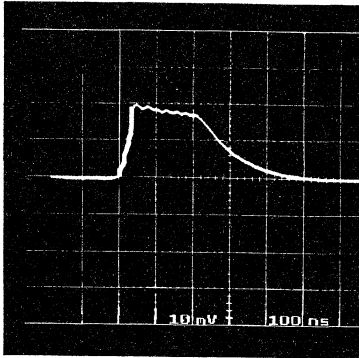
DC = Duty Cycle of current flow

For the design example the power dissipation, not considering the duty cycle is :

$$\begin{aligned} P_d &= ((2.5)^2 \cdot 7.5 \cdot 0.01) + ((5)^2 \cdot 7.5 \cdot 0.01) \\ &= 0.469 + 1.875 \\ &= 2.344 \text{ W} \quad (6) \end{aligned}$$

If the device is chopping for only a portion of the time the dissipation in the resistor will be reduced.

Figure 9b : Turn off 2.0A/div.



CONCLUSION

With the 0.2 μ F bypass capacitor and the snubber circuit in place the voltage transients measured in

the application have been limited to within safe values for the L6202. As shown in figure 8, the power supply voltage, the voltage across each of the DMOS transistors and the voltage across the output of the bridge (Vout1 - Vout2) are all within the maximum rating of the device with some margin.

SUMMARY

To insure reliable performance of a H-bridge drive circuit, the designer must insure that the device operates within the maximum ratings of the device(s) used in the circuit. One of the critical parameters to consider is the maximum voltage capability of the devices. To maintain the reliability, the voltage transients due to switching inductive loads must be maintained within the ratings of the device.

Two techniques used to control the voltage transients in fast switching applications are proper bypass filtering of the power supply and snubbing the outputs to control voltage rise times. Using these two techniques the voltage transients in a DMOS bridge application can be controlled to within safe levels.

A HIGH EFFICIENCY, MIXED-TECHNOLOGY MOTOR DRIVER

By C. CINI

A new mixed technology called *Multipower-BCD* allows the integration of bipolar linear circuits, CMOS logic and DMOS power transistors on the same chip. This note describes a H-bridge motor driver IC realized with this technology.

The miniaturization and integration of complex systems and subsystems has led in recent years to the implementation of monolithic circuits integrating logic functions and power sections.

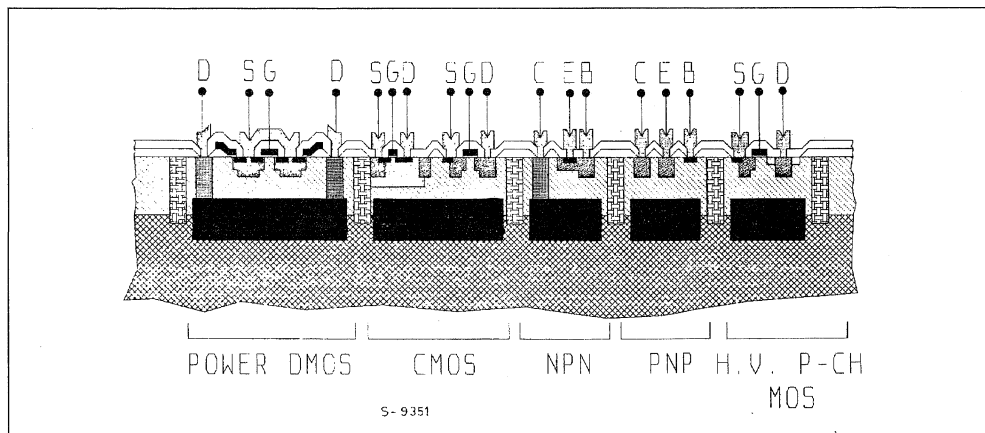
For these applications SGS-THOMSON Microelectronics has developed a new technology called *Multipower BCD* which allows the integration on the same chip of isolated Power DMOS elements, bipolar transistors and C-MOS logic.

Thanks to high efficiency, fast switching speed and the absence of secondary breakdown, this technology is particularly suitable for fast, high current sole-

noid drivers and high frequency switching motor control. The free-wheeling diode intrinsic to the DMOS structure (necessary if the device drives an inductive load) and the great flexibility available in the choice of the logic and driving section components allow the complete integration of power actuators without further expense in silicon area and a compact implementation of complex signal functions.

This technology has been applied to produce a switching power driver - the L6202/3 - capable of delivering 4A per phase, which is suitable for speed and position control in D.C. motor applications.

Figure 1 : A Schematic Cross Section of Bipolar, C-MOS, DMOS Structures (BCD).



MULTIPOWER BCD TECHNOLOGY

Multipower BCD technology combines the well known vertical DMOS silicon gate process, used for discrete POWER MOS devices, and the standard junction isolation, sinker and buried layer process. The architecture of the process is centred around the vertical DMOS silicon gate, a self aligned structure, which guarantees short channel length (1.5 μm) with consequent low $R_{DS(ON)}$ for the device.

In standard IC technologies the voltage capability is determined essentially by the thickness of the epitaxial layer and it is the same for signal and power components. But if the epi thickness is increased to allow the inclusion of high voltage transistors even the linear dimension of small signal transistors must be increased proportionally. In contrast MULTIPOWER BCD permits the realization of high voltage lateral DMOS structures in an epi-layer dimensioned for low voltage bipolar linear elements. Thus

it is possible to mix on the same die very dense CMOS logic, high precision bipolar linear circuits, very efficient DMOS power devices and high voltage lateral DMOS structures.

In this way the constraints which limit the complexity of signal processing circuits that can be integrated economically on a high chip are greatly reduced.

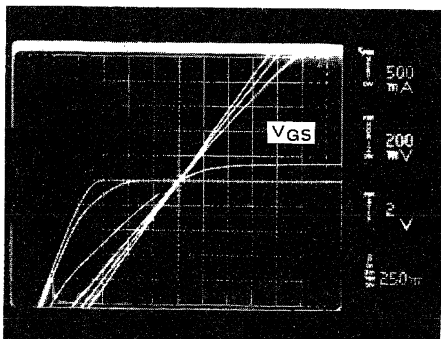
The active structures available in Multipower BCD technology are represented in fig. 1.

Within the vertical DMOS is indicated an intrinsic diode that can operate as a fast free-wheeling diode

Table 1 : Devices in Multipower BCD Technology.

• Vertical DMOS	$BV_{DSS} > 60 \text{ V}$	$V_{TH} \approx 3 \text{ V}$	$f_T > 1 \text{ GHz}$
• Lateral DMOS	$BV_{DSS} > 100 \text{ V}$	$V_{TH} \approx 3 \text{ V}$	$f_T > 800 \text{ MHz}$
• P-channel with Drain Extension	$BV_{DSS} > 85 \text{ V}$	$V_{TH} \approx 3 \text{ V}$	$f_T > 200 \text{ MHz}$
• Bipolar NPN	$LV_{CEO} > 20 \text{ V}$	$\beta = 35$	$f_T > 300 \text{ MHz}$
• Bipolar PNP	$LV_{CEO} > 20 \text{ V}$	$\beta = 20$	$f_T > 7 \text{ MHz}$
• C-MOS N and P-channel	$BV_{DSS} > 20 \text{ V}$	$V_{TH} \approx 3 \text{ V}$	

Figure 2 : I-V Characteristic of DMOS N-channel Power Device.



THE L6202 & L6203 H-BRIDGE DRIVERS

Using this technology a H-bridge IC has been realized which accepts TTL or C-MOS compatible signals and is suitable for high efficiency, high frequency switching control of DC and stepping motor. The power stage consists of four DMOS N-channel transistors with $R_{DS(ON)} \approx 0.3 \Omega$.

When this device is supplied with the maximum voltage of 60V it can deliver a DC current of 1.5A in a standard DIP.16 (L6202) and up to 5A in a MULTI-WATT package (L6203).

The device can also operate with a peak current of 8A for a time interval essentially determined by the time constant of heat propagation ($< 200\text{ms}$).

in switch mode applications. In fact DMOS, as a result of the way by which it is realized, is almost a symmetrical bidirectional device. That is, it can operate with the electrical I-V characteristic shown in the 3rd quadrant of fig. 2 ; that is, as a controlled resistor of value decreasing inversely with the gate source voltage applied to the power to which it is associated, up to a minimum equal to the $R_{DS(ON)}$ of the device itself, shunted by the body-drain diode intrinsic to the structure that limits the negative excursion of V_{DS} . Of the devices represented in fig. 1 the table 1 lists the electrical characteristics.

The system diagram representing the internal function blocks and external components (outside the dashed line) is shown in fig. 3.

The integrated circuit has 3 Inputs : Enable, Input 1, Input 2. When Enable is "low" all power devices are off ; when it is "high" their conduction state is controlled by the logic signals Input 1 and Input 2 that drive independently a single branch of the full bridge. When Input 1 (Input 2) is "high" DMOS 1 (DMOS 1') is "on" and DMOS 2 (DMOS 2') is "off", when is "low" DMOS 1 (DMOS 1') is "off" and DMOS 2 (DMOS 2') is "on".

A thermal protection circuit has been included that will disable the device if the junction temperature reaches 150°C . When the thermal protection is removed the device restarts under the control of the Input and Enable signals.

ON-OFF SYNCHRONIZATION CIRCUIT

ON-OFF synchronization of the power devices located on the same leg of the bridge must prevent simultaneous conduction, with obvious advantages in terms of power dissipation and of spurious signals on the ground and on sensing resistors.

Because of the very short turn-on, turn-off times characteristic of POWER MOS devices a dead time (time in which all power transistors are "off") of 40 ns is sufficient to prevent rail-to-rail shorts. The circuit that provides this time interval is shown in fig. 4 with the voltage waveforms that explain how it works. Let us suppose Enable = "high". Because of the delay times introduced by INV1 and INV2, V2 and V3 are two waveforms contained one in the

Figure 3 : L6202-6203 Block Diagram.

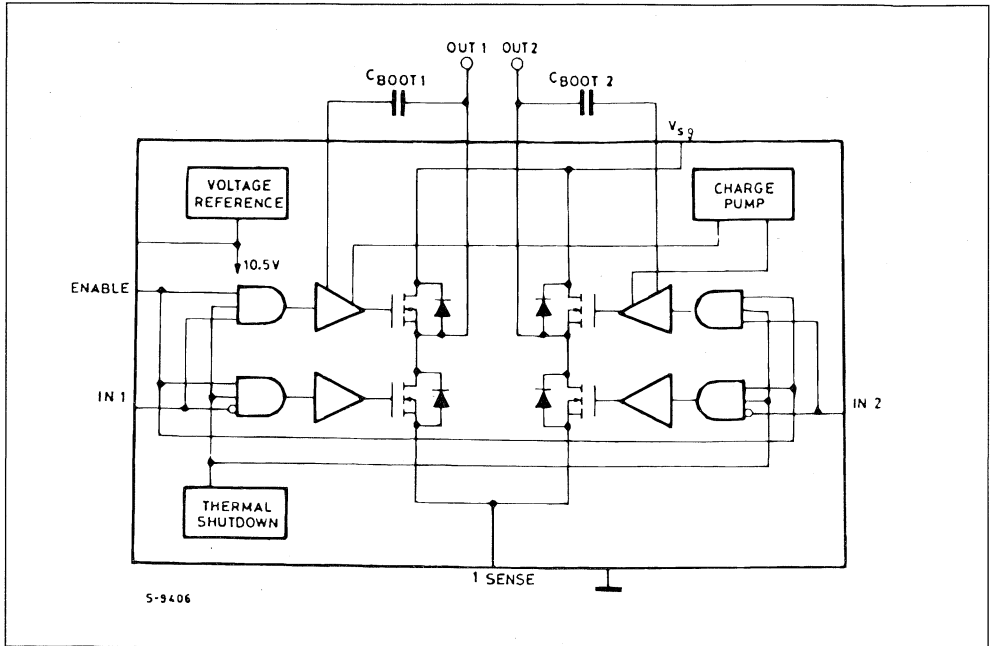
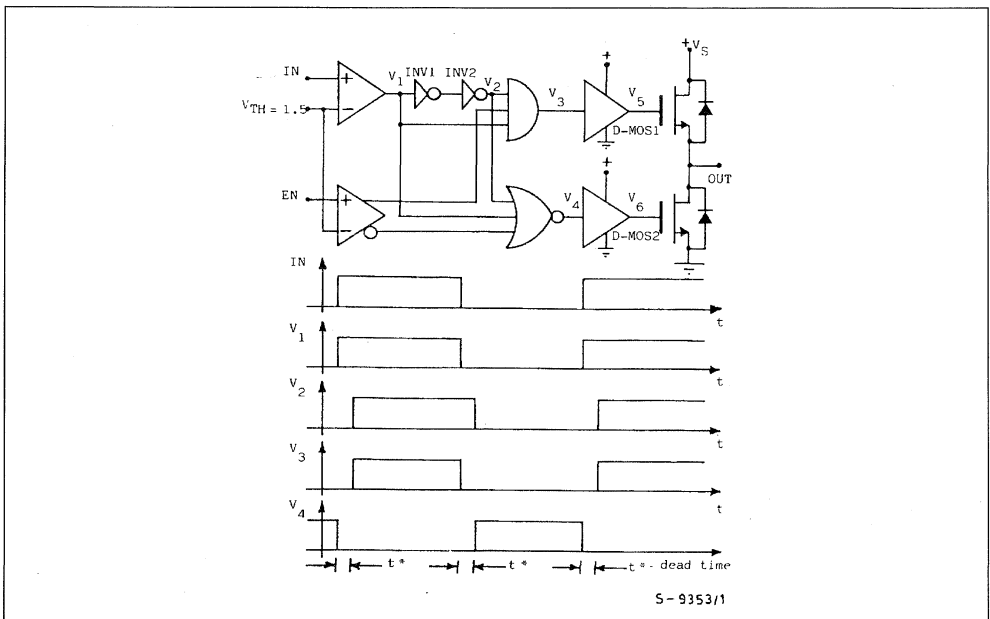


Figure 4 : A Schematic Representation of ON-OFF Synchronism Circuit.

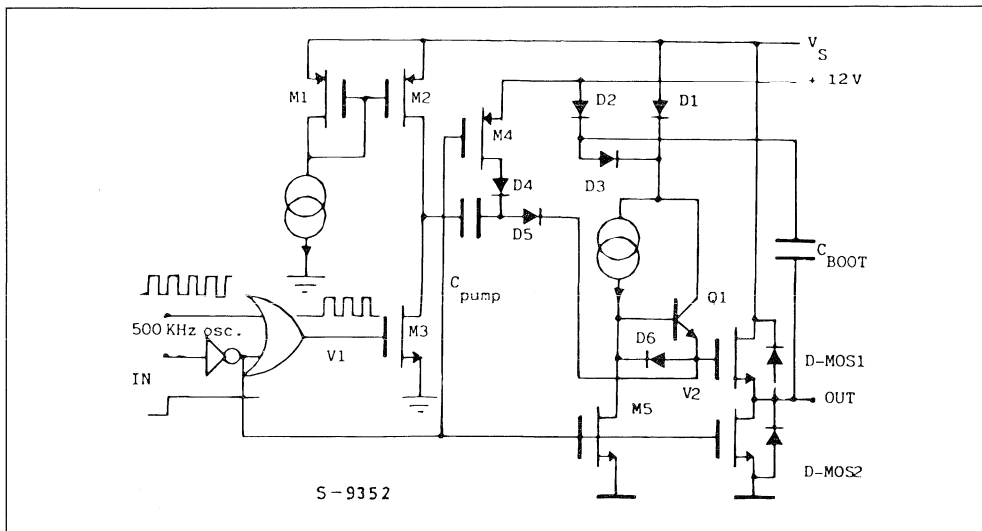


other and of polarity suitable to assure that the turn-on of a power transistor happens only after the turn-off of the other. The gate voltages V_5 and V_6 of DM1 and DM2 are represented in fig. 5. In fig. 3 we can see also the modality of operation of the Enable signal, charge pump and bootstrap circuits.

Concerning POWER MOS driving, it must be noted that it is necessary to assure to all DMOS N-channel a gate-source voltage of about 10V to guarantee full conduction of the POWER MOS itself. While there are no particular problems for driving the lower POWER MOS device (its terminals is referred to ground) for the upper one it is necessary to provide a gate voltage higher than the positive supply because it has the drain connected to the positive supply itself.

This is obtained using a system that combines a charge pump circuit, that assures DC operation, with a bootstrapping technique suitable to provide high switching frequencies. The circuit that satisfies to all these requirements is represented in the schematic diagram of fig. 6.

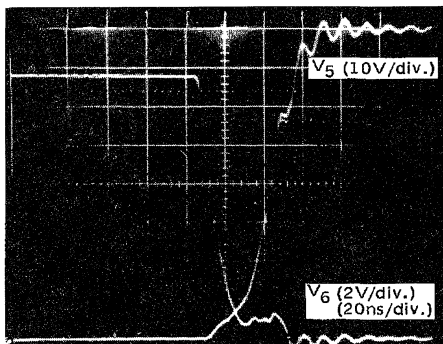
Figure 6 : Schematic Representation of Charge PUMP and BOOSTRAP Circuit used to Drive the Gate of the Upper DMOS Device.



In this condition, by means of D1, the circuit charges immediately the DMOS1 gate capacitance to V_S while the charge pump, activated by the signals $IN = \text{"low"}$, as it can be seen in fig. 7, must supply only a voltage of about 10V.

In the switching operation it will be C_{BOOT} that guar-

Figure 5 : POWER MOS Gate Voltage Waveforms.



In the description of this circuit we can assume that C_{BOOT} is absent and IN commutes from the "low" to the "high" level.

antees a faster turn-on of the upper POWER MOS and consequently high commutation frequencies.

In fact during the period in which DMOS2 is "on" C_{BOOT} is charged to a voltage of about 12V.

When V_{out} raises because DMOS2 is disactivated D2 and D1 became "off" while D3, that remains "on"

connects the gate circuit to C_{BOOT} that raises higher than V_S and makes DMOS1 full "on" in a very short time interval (20 ns).

It must be noted that the switch M4 in the fig. 6 circuit, driven by a complementary phase respect to M3 disconnects D4, D5 and D6 from 12 V when M5 goes "on" to assure the "turn-off" of DMOS1.

Figure 7 : Charge PUMP Abilitation Signal and Gate Voltage of DMOS Upper Device.

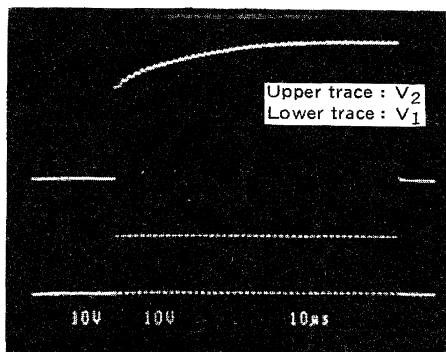
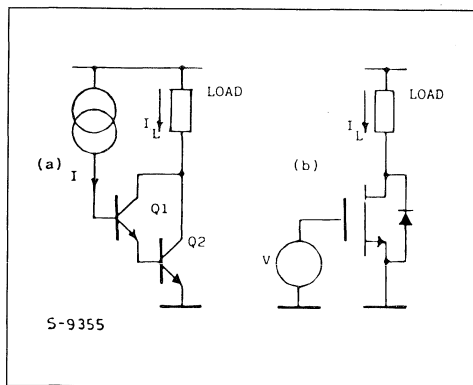


Figure 8 : Darlington Bipolar and DMOS Power Stages.



PERFORMANCE

One of the most important features is the very high efficiency achieved.

To appreciate the benefits of low power dissipation, and consequently of high efficiency, of a circuit realized in DMOS technology we must refer to the equivalent bipolar solution and also consider separate DC and AC operation.

Consider the typical Darlington power stage frequently used in integrated circuit and a DMOS power stages both represented in fig. 8. Neglecting the power dissipation in the driving section, in static conditions, the total dissipation of the two stages when they are "on" is in the case (a) :

$$P_{d(a)} = (V_{CESAT1} + V_{BE2}) \times I_L$$

and in the case (b) :

$$P_{d(b)} = R_{DS(ON)} \times I_L^2$$

where I_L is the load current.

Because the saturation loss of a power DMOS transistor can be reduced by increasing the silicon area it is possible to satisfy the condition

$$R_{DS-ON} \times I_L < (V_{CESAT1} + V_{BE2})$$

and then to obtain lower dissipation.

Concerning to the driving section, an other essential difference must be emphasised.

While in case (a) during the time in which the power is "ON" it is necessary to supply a current for maintaining Q1 saturated, in the case (b) power is dissipated only during the commutation of the gate voltage.

About AC operation, it must be noted that the greatest advantage, always in terms of power dissipation, is due to the inherently fast turn-on, turn-off times of power MOS devices. In fact, if we suppose that the load is of inductive type and that the current waveform is triangular on the voltage commutation of the output, the total power dissipation is :

$$P_d = V_S I_L T_{COM} \cdot f_{SWITCH}$$

where : V_S = Supply voltage, I_L = Peak load current,

$$T_{COM} = T_{TURN-ON} = T_{TURN-OFF},$$

$$f_{SWITCH} = \text{Chopper frequency.}$$

Because T_{COM} in DMOS case is $\leq$ than in bipolar case at a fixed frequency we have a lower dissipation or at fixed dissipation we can tolerate higher switching frequency.

Considering all these aspects, with a power device consisting of about 2200 cells we have realized DMOS power devices characterized by $R_{DS(ON)}$ 0.3 Ω and by switching times t_r , t_f of 50 ns. Other characteristics of the device when is configured as shown in fig. 9 are listed in table 2.

Fig. 10 shows the supply current with no load, vs. switching frequency.

Figure 9.

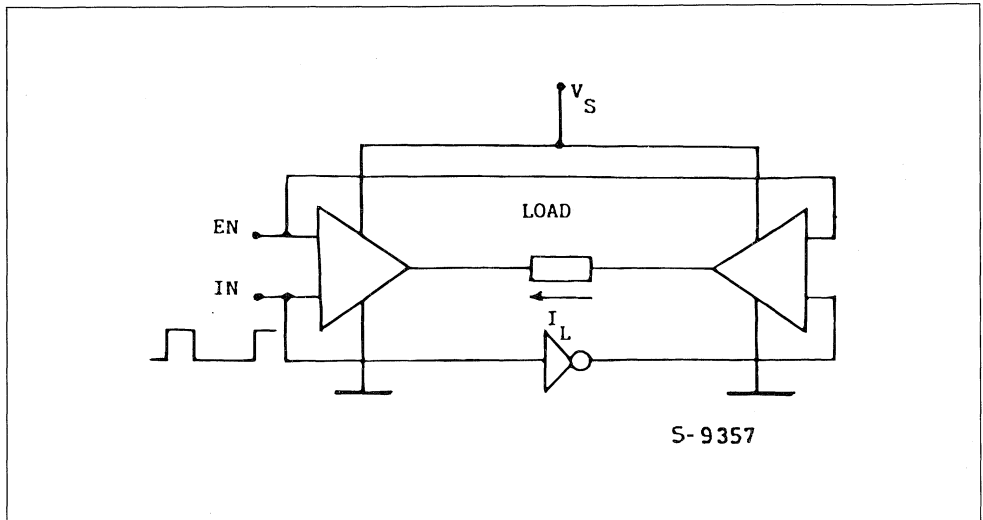
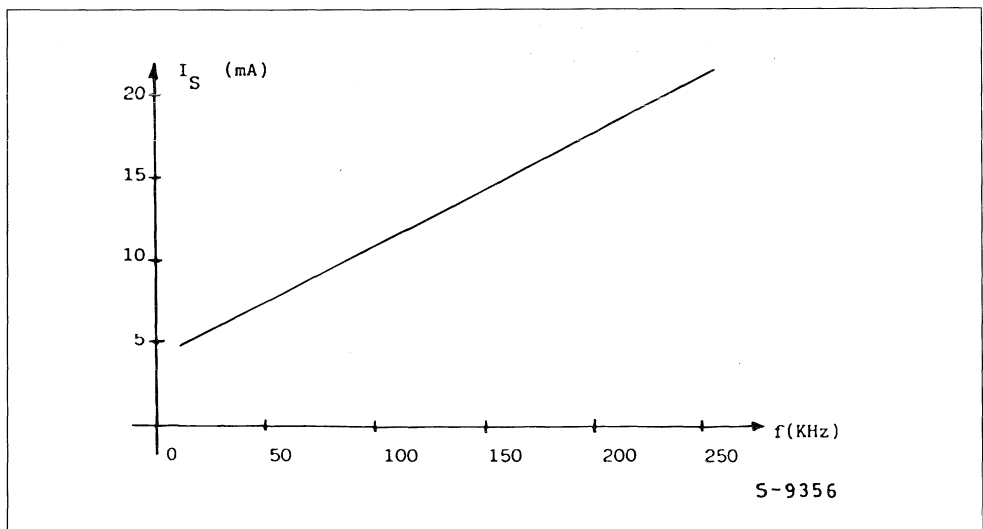


Table 2 : Main Features of L6202/6203.

• V_S (maximum supply voltage)	= 60 V
• I_L (maximum output current)	= 1.5 A DIP.16
	= 5 A MULTIWATT Package
• Efficiency	$\eta = 90\%$ $\left\{ \begin{array}{l} I_L = 1.5 \text{ A} \\ f_{\text{chopper}} = 50 \text{ KHz} \\ V_S = 54 \text{ V} \end{array} \right.$
• Power Dissipation	$P_d = 1.5 \text{ W}$
• t_d (turn-on, turn-off propagation delay)	= 100 ns

Figure 10.



STEPPER MOTOR DRIVING

By H. SAX

Dedicated integrated circuits have dramatically simplified stepper motor driving. To apply these ICs designers need little specific knowledge of motor driving techniques, but an understanding of the basics will help in finding the best solution. This note explains the basics of stepper motor driving and describes the drive techniques used today.

From a circuit designer's point of view stepper motors can be divided into two basic types : unipolar and bipolar.

A stepper motor moves one step when the direction of current flow in the field coil(s) changes, reversing the magnetic field of the stator poles. The difference between unipolar and bipolar motors lies in the way that this reversal is achieved (figure 1) :

Figure 1a : BIPOLAR - with One Field Coil and Two Chargeover Switches That are Switched in the Opposite Direction.

Figure 1b : UNIPOLAR - with Two Separate Field Coils and are Chargeover Switch.

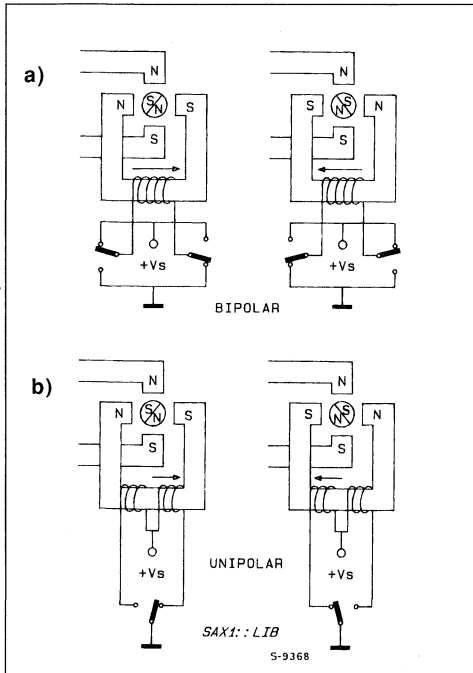
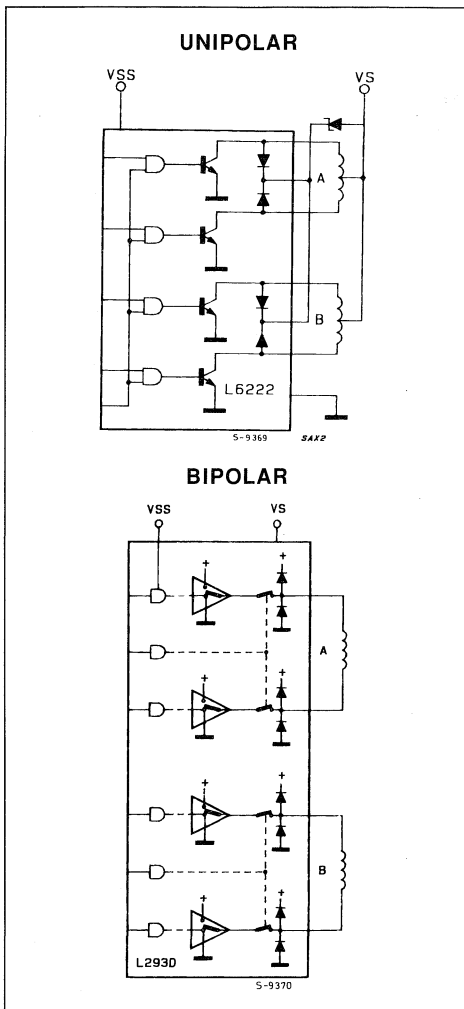


Figure 2 : ICs for Unipolar and Bipolar Driving.



The advantage of the bipolar circuit is that there is only one winding, with a good bulk factor (low winding resistance). The main disadvantages are the two changeover switches because in this case more semiconductors are needed.

The unipolar circuit needs only one changeover switch. Its enormous disadvantage is, however, that a double bifilar winding is required. This means that at a specific bulk factor the wire is thinner and the resistance is much higher. We will discuss later the problems involved.

Unipolar motors are still popular today because the drive circuit appears to be simpler when implemented with discrete devices. However with the integrated circuits available today bipolar motors can be driven with no more components than the unipolar motors. Figure 2 compares integrated unipolar and bipolar devices.

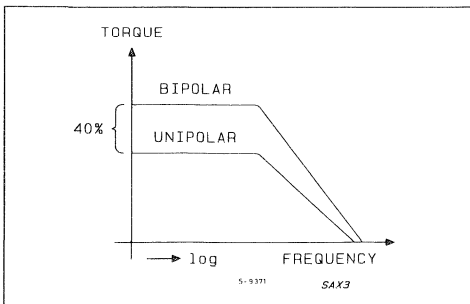
BIPOLAR PRODUCES MORE TORQUE

The torque of the stepper motor is proportional to the magnetic field intensity of the stator windings. It may be increased only by adding more windings or by increasing the current.

A natural limit against any current increase is the danger of saturating the iron core. Though this is of minimal importance. Much more important is the maximum temperature rise of the motor, due to the power loss in the stator windings. This shows one advantage of the bipolar circuit, which, compared to unipolar systems, has only half of the copper resistance because of the double cross section of the wire. The winding current may be increased by the factor $\sqrt{2}$ and this produces a direct proportional affect on the torque. At their power loss limit bipolar motors thus deliver about 40 % more torque (fig. 3) than unipolar motors built on the same frame.

If a higher torque is not required, one may either reduce the motor size or the power loss.

Figure 3 : Bipolar Motors Driver Deliver More Torque than Unipolars.



CONSTANT CURRENT DRIVING

In order to keep the motor's power loss within a reasonable limit, the current in the windings must be controlled.

A simple and popular solution is to give only as much voltage as needed, utilizing the resistance (R_L) of the winding to limit the current (fig. 4a). A more complicated but also more efficient and precise solution is the inclusion of a current generator (fig. 4b), to achieve independence from the winding resistance. The supply voltage in Fig. 4b has to be higher than the one in Fig. 4a. A comparison between both circuits in the dynamic load/working order shows visible differences.

Figure 4 : Resistance Current Limiter (a) and Current Generator Limiting.

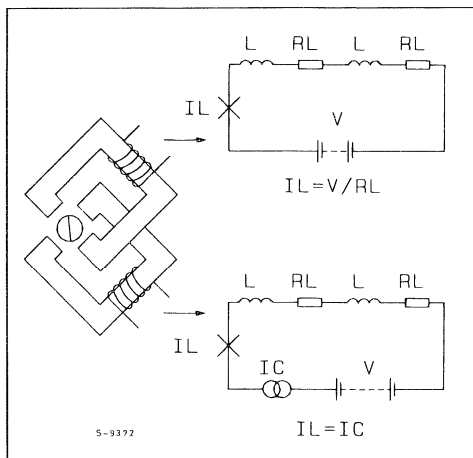
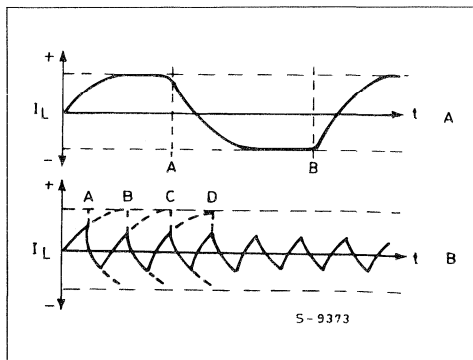


Figure 5 : At High Step Frequencies the Winding Current cannot Reach its Setting Value because of the Continuous Direction Change.



It has already been mentioned that this power of the motor is, among others, proportional to the winding current.

In the dynamic working order a stepper motor changes poles of the winding current in the same stator winding after two steps. The speed with which the current changes its direction in the form of an exponential function depends on the specified inductance, the coil resistance and on the voltage. Fig. 5a shows that at a low step rate the winding current I_L reaches its nominal value V_L/R_L before the direction is changed. However, if the poles of the stator windings are changed more often, which corresponds to a high step frequency, the current no longer reaches its saturating value because of the limited change time; the power and also the torque diminish clearly at increasing number of revolutions (fig. 5).

MORE TORQUE AT A HIGHER NUMBER OF REVOLUTIONS

Higher torque at faster speeds are possible if a current generator as shown in Fig. 4b is used. In this application the supply voltage is chosen as high possible to increase the current's rate of change. The current generator itself limits only the phase current and becomes active only the moment in which the coil current has reached its set nominal value. Up to this value the current generator is in saturation and the supply voltage is applied directly to the winding.

Fig. 6, shows that the rate of the current increase is now much higher than in Figure 5. Consequently at higher step rates the desired current can be maintained in the winding for a longer time. The torque decrease starts only at much higher speeds.

Fig. 7 shows the relation between torque and speed in the normal graphic scheme, typical for the stepper motor. It is obvious that the power increases in the upper torque range where it is normally needed, as the load to be driven draws most energy from the motor in this range.

EFFICIENCY - THE DECISIVE FACTOR

The current generator combined with the high supply voltage guarantees that the rate of change of the current in the coil is sufficiently high.

At the static condition or at low numbers of revolutions, however, this means that the power loss in the current generator dramatically increases, although the motor does not deliver any more energy in this range; the efficiency factor is extremely bad.

Help comes from a switched current regulation using the switch-transformer principle, as shown in

fig. 8. The phase winding is switched to the supply voltage until the current, detected across R_s , reaches the desired nominal value. At that moment the switch, formerly connected to $+V_s$, changes position and shorts out the winding. In this way the current is stored, but it decays slowly because of inner winding losses. The discharge time of the current is determined during this phase by a monostable or pulse oscillator. After this time one of the pole changing switches changes back to $+V_s$, starting an induction recharge and the clock-regulation-cycle starts again.

Figure 6 : With a Step Current Slew, it is not a Problem to Obtain, even at High Step frequencies Sufficient Current in Windings.

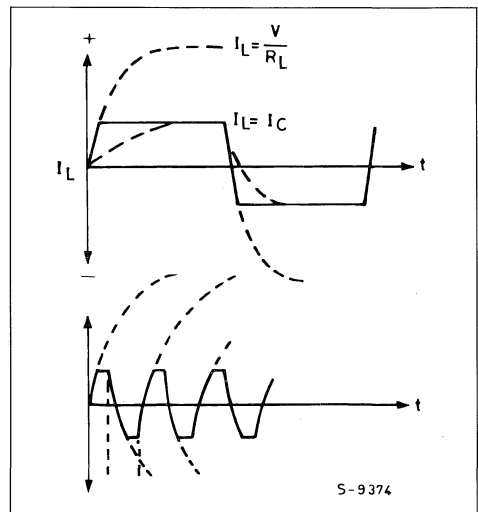
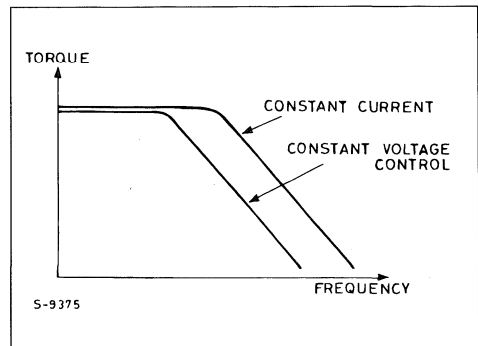


Figure 7 : Constant Current Control of the Stepper Motor Means more Torque at High Frequency.



Since the only losses in this technique are the saturation loss of the switch and that of the coil resistance, the total efficiency is very high.

The average current that flows from the power supply line is less than the winding current due to the concept of circuit inversion. In this way also the power unit is discharged. This kind of phase current control that has to be done separately for each motor phase leads to the best ratio between the supplied electrical and delivered mechanical energy.

POSSIBLE IMPROVEMENTS OF THE UNIPOLAR CIRCUIT

It would make no sense to apply the same principle to a stabilized current controlled unipolar circuit, as two more switches per phase would be necessary for the shortening out of the windings during the free phase and thus the number of components would be the same as for the bipolar circuit ; and more-

over, there would be the well known torque disadvantage.

From the economic point of view a reasonable and justifiable improvement is the "Bi-Level-Drive" (fig. 9). This circuit concept works with two supply voltages ; with every new step of the motor both windings are connected for a short time to a high supply voltage. This considerably increases the current rate of change and its behaviour corresponds more or less to the stabilized power principle. After a pre-determined time the switch opens, and a lower supply voltage is connected to the winding through a diode.

This kind of circuit by no means reaches the performance of the clocked stabilized power control as per fig. 8, as the factors : distribution voltage oscillation, B.e.m.f., thermal winding resistance, as well as the separate coil current regulation are not considered, but it is this circuit that makes the simple unipolar R/L-control suitable for many fields of application.

Figure 8 : With Switch Mode Current Regulation Efficiency is Increased.

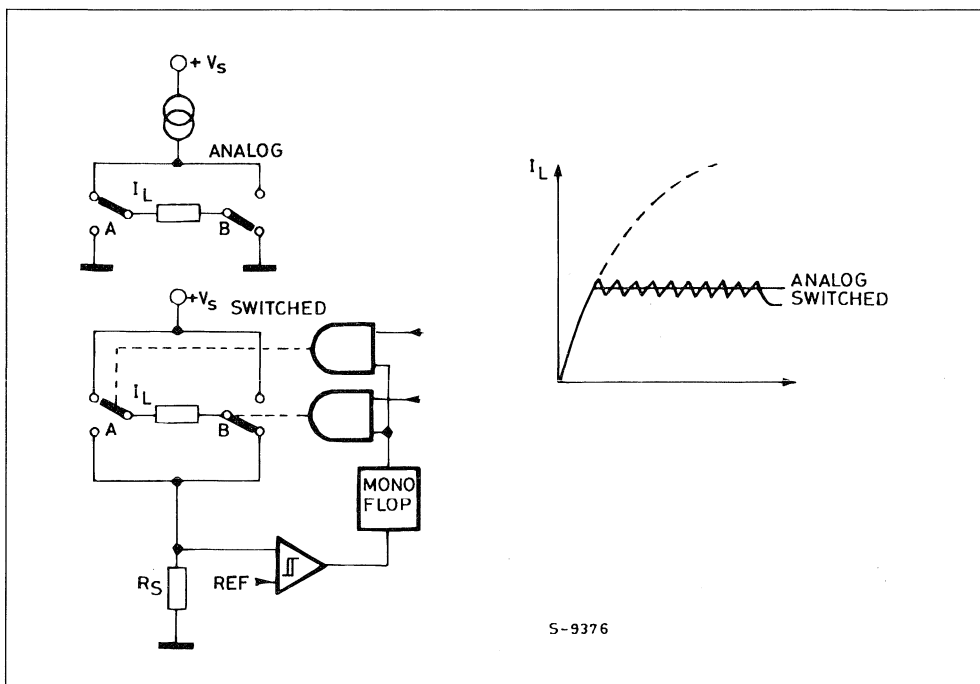
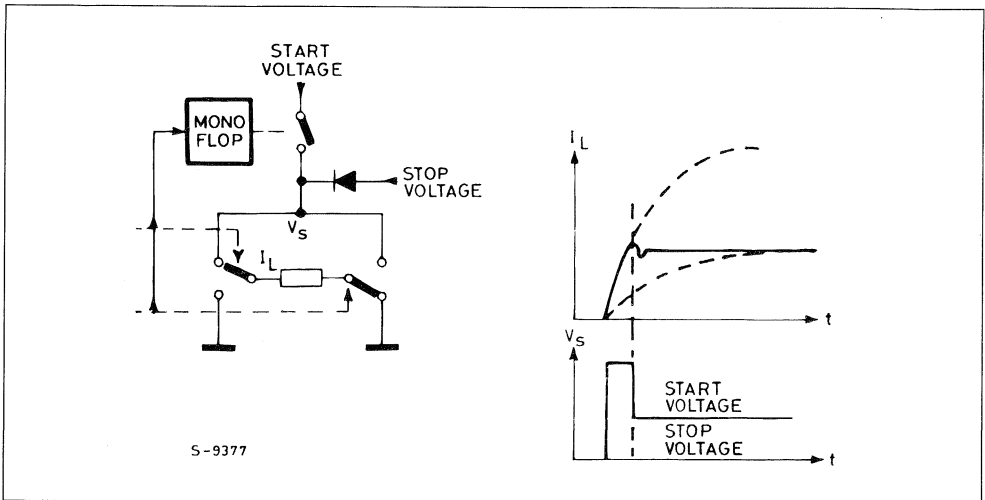


Figure 9 : At Every New Step of the Motor, it is Possible to Increase the Current Rate with a Bilevel Circuit.



ADVANTAGES AND DISADVANTAGES OF THE HALF-STEP

An essential advantage of a stepper motor operating at half-step conditions is its position resolution increased by the factor 2. From a 3.6 degree motor you achieve 1.8 degrees, which means 200 steps per revolution.

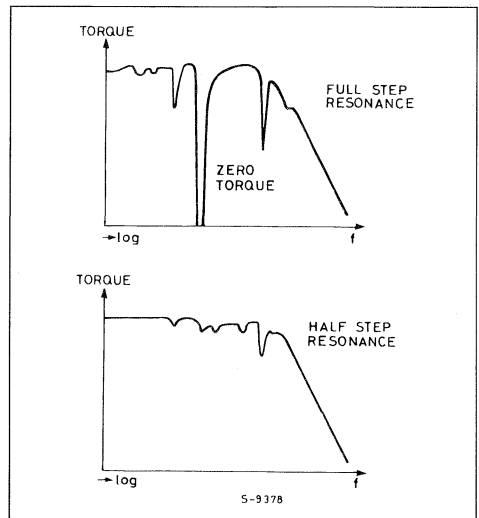
This is not always the only reason. Often you are forced to operate at half-step conditions in order to avoid that operations are disturbed by the motor resonance. These may be so strong that the motor has no more torque in certain step frequency ranges and loses completely its position (fig. 10). This is due to the fact that the rotor of the motor, and the changing magnetic field of the stator forms a spring-mass-system that may be stimulated to vibrate. In practice, the load might deaden this system, but only if there is sufficient frictional force.

In most cases half-step operation helps, as the course covered by the rotor is only half as long and the system is less stimulated.

The fact that the half-step operation is not the dominating or general solution, depends on certain disadvantages :

- the half-step system needs twice as many clock-pulses as the full-step system ; the clock-frequency is twice as high as with the full-step.
- in the half-step position the motor has only about half of the torque of the full-step.

Figure 10 : The Motor has no More Torque in Certain Step Frequency Ranges with Full Step Driving.



For this reason many systems use the half-step operation only if the clock-frequency of the motor is within the resonance risk area.

The dynamic loss is higher the nearer the load moment comes to the limit torque of the motor. This effect decreases at higher numbers of revolutions.

TORQUE LOSS COMPENSATION IN THE HALF-STEP OPERATION

It's clear that, especially in limit situations, the torque loss in half-step is a disadvantage. If one has to choose the next larger motor or one with a double resolution operating in full-step because of some insufficient torque percentages, it will greatly influence the costs of the whole system.

In this case, there is an alternative solution that does not increase the costs for the bipolar chopping stabilized current drive circuit.

The torque loss in the half-step position may be compensated for by increasing the winding current by the factor $\sqrt{2}$ in the phase winding that remains active. This is also permissible if, according to the motor data sheet, the current limit has been reached, because this limit refers always to the contemporary supply with current in both windings in the full-step position. The factor $\sqrt{2}$ increase in current doubles the stray power of the active phase. The total dissipated power is like that of the full-step because the non-active phase does not dissipate power.

The resulting torque in the half-step position amounts to about 90 % of that of the full-step, that means dynamically more than 95 % torque compared to the pure half-step ; a neglectable factor.

The only thing to avoid is stopping the motor at limit current conditions in a half-step position because it would be like a winding thermal phase overload concentrated in one.

The best switch-technique for the half-step phase current increase will be explained in detail later on Fig. 11 shows the phase current of a stepping motor in half-step control with and without phase current increase and the pertinent curves of step frequency and torque.

Figure 11 : Half Step Driving with Shaping Allows to Increase the Motor's Torque to about 95 % of that of the Full Step.

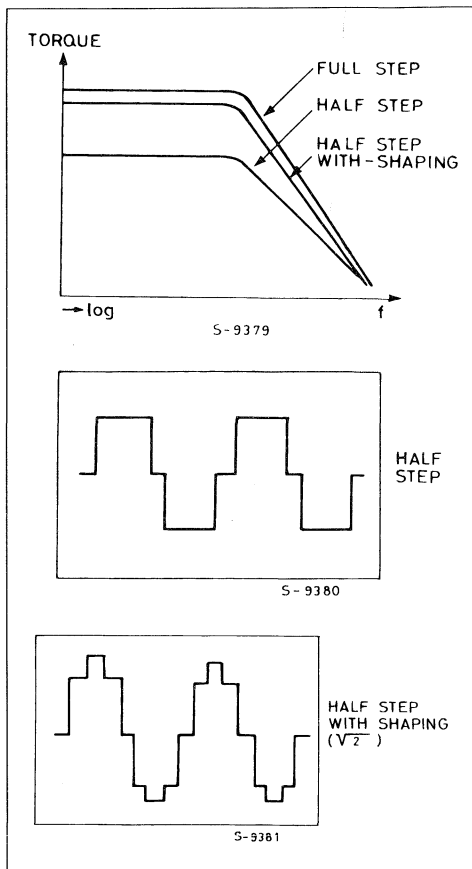
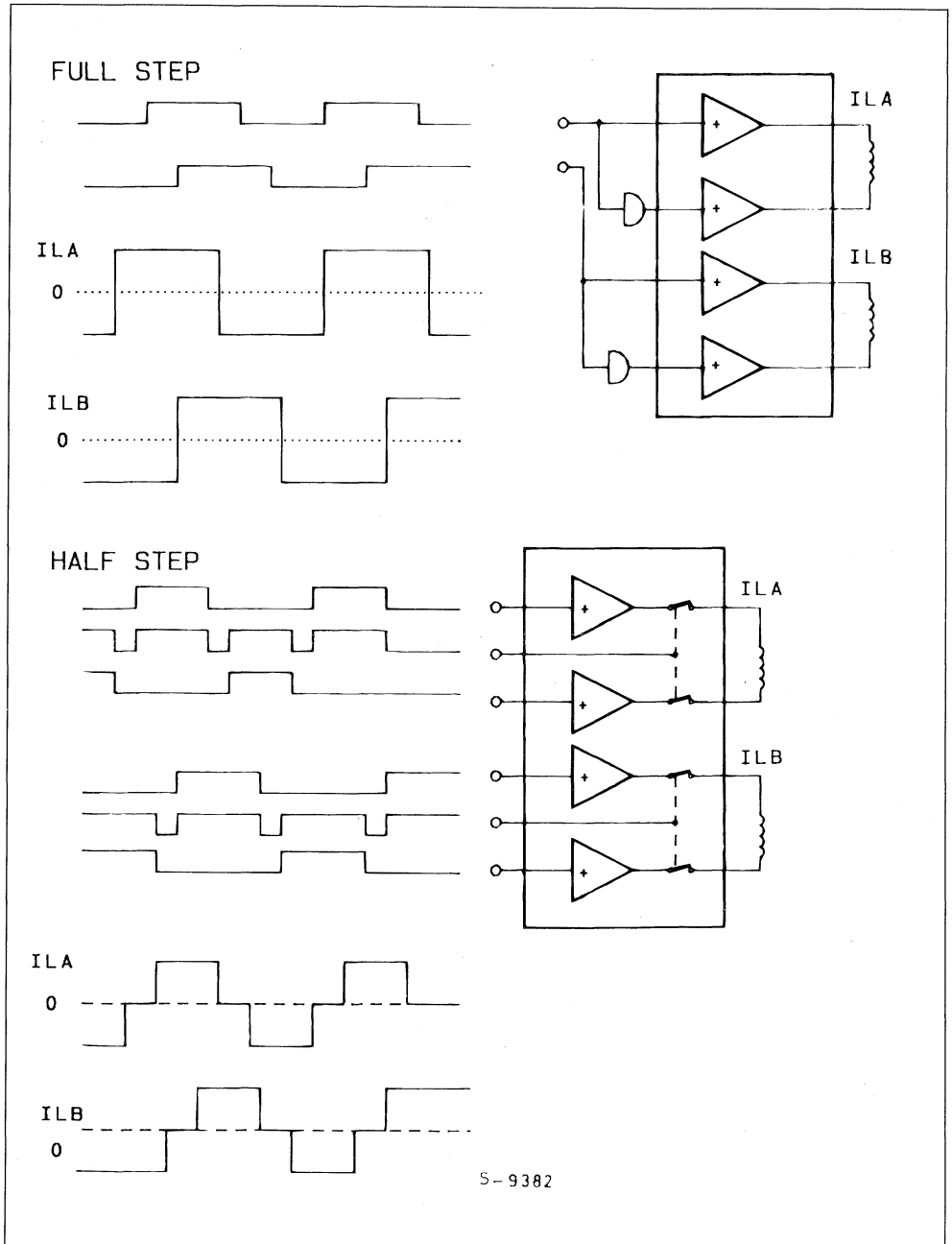


Figure 12 : Only Two Signals for Full Step Driving are Necessary while Four (six if three-state is needed on the output stages) for half Step.



DRIVE SIGNALS FOR THE MICRO ELECTRONIC

A direct current motor runs by itself if you supply it with voltage, whereas the stepping motor needs the commutation signal in for of several separated but linkable commands. In 95 % of the applications today, the origin of these digital commands is a microprocessor system.

In its simplest form, a full-step control needs only two rectangular signals in quadrature. According to which phase is leading, the motor axis rotates clockwise or counter-clockwise, whereby the rotation speed is proportional to the clock frequency.

In the half-step system the situation becomes more complicated. The minimal two control signals become four control signals. In some conditions as many as six signals are needed. If the Tri-state-command for the phase ranges without current, necessary for high motor speeds, may not be obtained from the 4 control signals. Fig. 12 shows the relationship between the phase current diagram and the control signal for full and half-step.

Since all signals in each mode are in defined relations with each other, it is possible to generate them using standard logic. However, if the possibility to

choose full and half-step is desired, a good logic implementation becomes quite expensive and an application specific integrated circuit would be better. Such an application specific integrated circuit could reduce the number of outputs required from a microprocessor from the 6 required to 3 static and dynamic control line.

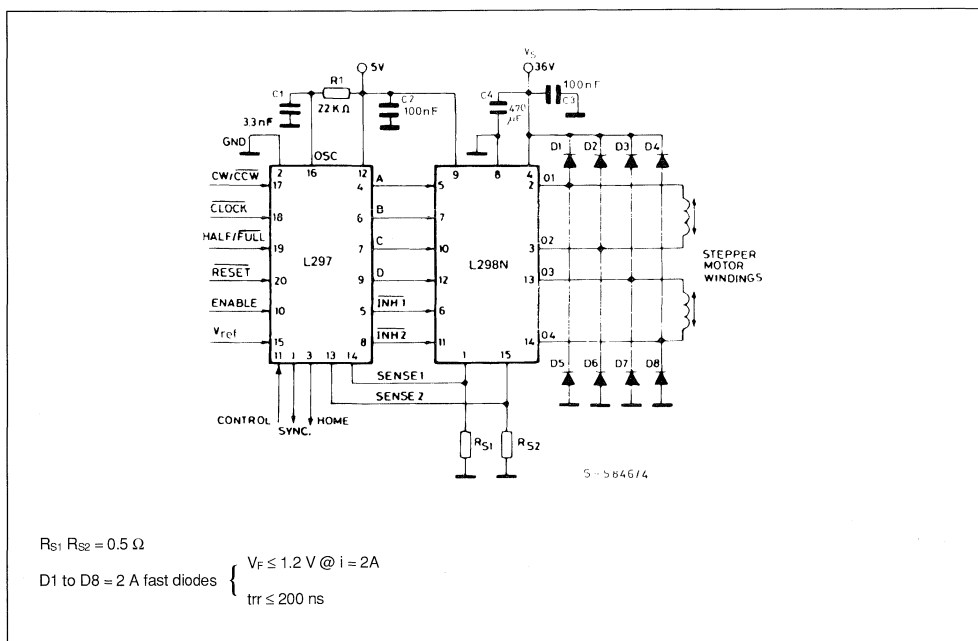
A typical control circuit that meets all these requirements is the L297 unit (fig. 13).

Four signals control the motor in all operations :

1. CLOCK : The clock signal, giving the stepping command
2. RESET : Puts the final level signals in a defined start position
3. DIRECTION : Determines the sense of rotation of the motor axis.
4. HALF/FULL : Desides whether to operate in full or in half-step.

Another inhibit input allows the device to switch the motor output into the Tri-state-mode in order to prevent undesired movements during undefined operating conditions, such as those that could occur during.

Figure 13 : The L297 avoids the Use of Complicated Standard Logic to Generate Both Full and Half-step Driving Signals Together with Chopper Current Control.



SWITCH-MODE CURRENT REGULATION

The primary function of the current regulation circuit is to supply enough current to the phase windings of the motor, even at high step rates.

The functional blocks required for a switchmode current control are the same blocks required in switching power supplies ; flip-flops, comparators ; and an oscillator are required. These blocks can easily be included in the same IC that generates the phase control signals. Let us consider the implementation of chopper current control in the L297.

The oscillator on pin 16 of the L297 resets the two flip-flops at the start of each oscillator period. The flip-flop outputs are then combined with the outputs of the translator circuit to form the 6 control signals supplied to the power bridge (L298).

When activated, by the oscillator, the current in the winding will raise, following the L/R time constant curve, until the voltage across the sense resistor (pin 1, 15 of L298) is equal to the reference voltage input (pin 15, L297) the comparator then sets the flip-flop, causing the output of the L297 to change to an equi-phase condition, thus effectively putting a short circuit across the phase winding. The bridge is activated into a diagonally conductive state when the oscillator resets the flip-flop at the start of the next cycle.

Using a common oscillator to control both current regulators maintains the same chopping frequency for both, thus avoiding interference between the two.

The functional block diagram of the L297 and the power stage (L298) are shown in Figure 14 along with the operating wave forms.

An important characteristics of this circuit implementation is that, during the reset time, the flip-flops are kept reset. The reset time can be selected by selecting the impedance of the R/C network on pin 16. In

this way, the current spike and noise across the sense resistors that may occur during switching will not cause a premature setting of the flip-flop. Thus the recovery current spike of the protection diodes can be ignored and a filter in the sense line is avoided.

THE RIGHT PHASE CURRENT FOR EVERY OPERATING CONDITION

The Chopper principle of the controller unit reveals that the phase current in the motor windings is controlled by two data : the reference voltage at pin 15 of the controller and the value of the sense resistance at pins 1 and 15 of the L298, that is $I_L = V_{REF}/R_S$. By changing V_{REF} it is very easy to vary the current within large limits. The only question is for which purpose and at which conditions.

More phase current means more motor torque, but also higher energy consumption.

An analysis of the torque consumption for different periods and load position changes shows that there is no need for different energies.

There is a high energy need during the acceleration or break phases, whereas during continuous operation or neutral or stop position less energy has to be supplied. A motor with its phase current continuously oriented at the load moment limit, even with the load moment lacking, consumes needlessly energy, that is completely transformed into heat.

Therefore it is useful to resolve the phase current in at least two levels controllable from the processor. Fig. 18 shows a minimal configuration with two resistance and one small signal transistor as change-over switch for the reference input. With another resistance and transistor it is possible to resolve 2 Bits and consequently 4 levels. That is sufficient for all imaginable causes.

Fig. 16 shows a optimal phase current diagram during a positioning operation.

Figure 14 : Two ICs and very Few External Components Provide Complete Microprocessor to Bipolar Step-
per Motor Interface.

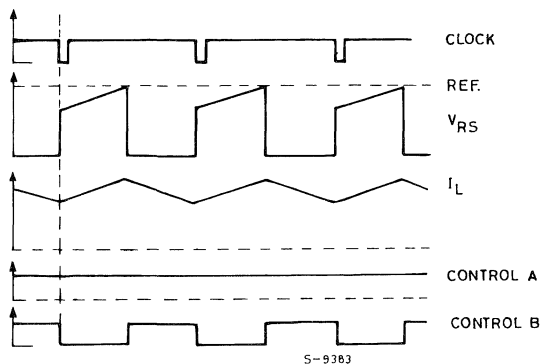
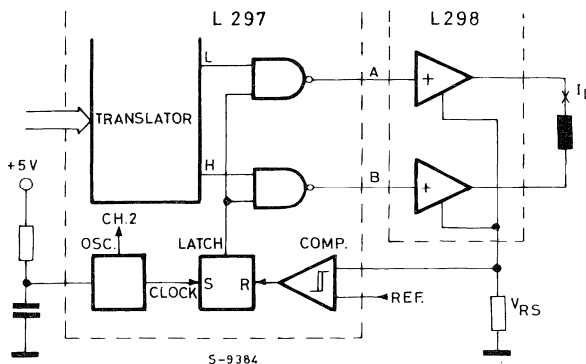


Figure 15 : Because of the Set-dominant Latch Inside the L297 it is Possible to Hide Current Spikes and Noise Across the Sense Resistors thus Avoiding External Filters.

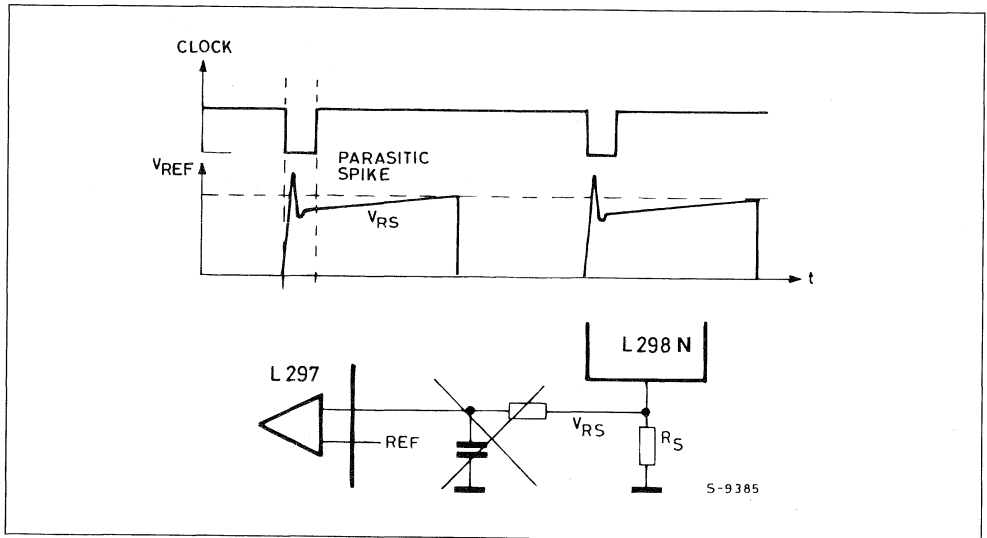
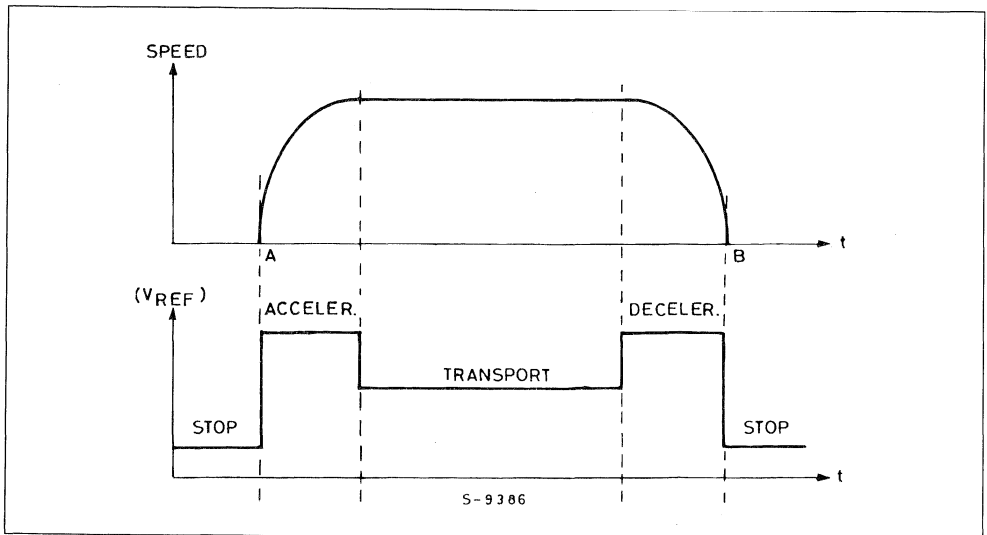


Figure 16 : More Energy is needed During The Acceleration and break Phases Compared the Continuous Operation, Neutral or Stop Position.



HIGH MOTOR CLOCK RESETS IN THE HALF-STEP SYSTEM

In the half-step position one of the motor phases has to be without current. If the motor moves from a full-step position into a half-step position, this means that one motor winding has to be completely discharged. From the logic diagram this means for the high level bridge an equivalent status of the input signals A/B, for example in the HIGH-status. For the coil this means short circuit (fig. 17 up) and consequently a low reduction of the current. In case of high half-step speeds the short circuit discharge time constant of the phase winding is not sufficient to discharge the current during the short half-step

phases. The current diagram is not neat, the half step is not carried out correctly (fig. 17 center).

For this reason the L297 controller-unit generates an inhibit-command for each phase bridge, that switches the specific bridge output in the half-step position into Tri-state. In this way the coil can start swinging freely over the external recovery diodes and discharge quickly. The current decrease rate of change corresponds more or less to the increase rate of change (fig. 17 below).

In case of full-step operation both inhibit-outputs of the controller (pin 5 and 8) remain in the HIGH-status.

Figure 17 : The Inhibit Signal Turns Off Immediately the Output Stages Allowing thus a Faster Current Decay (mandatory with half-step operation).

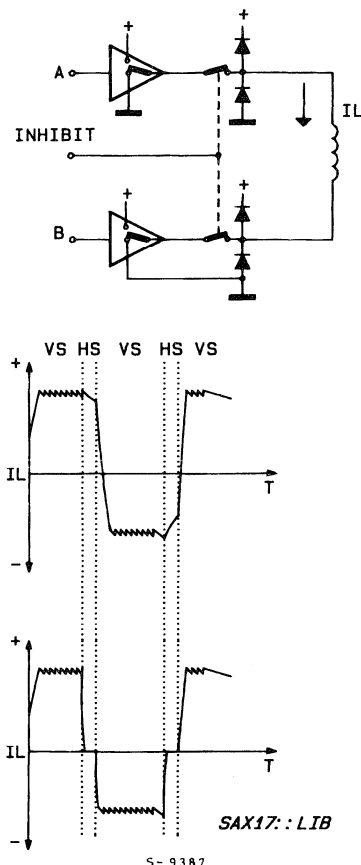
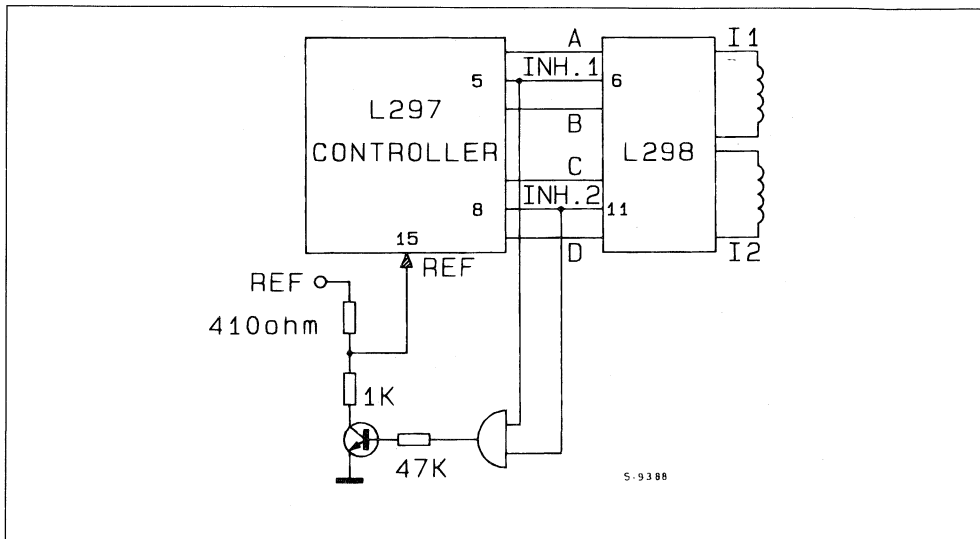


Figure 18 : With This Configuration it is Possible to Obtain Half-step with Shaping Operation and Therefore More Torque.



MORE TORQUE IN THE HALF-STEP POSITION

A topic that has already been discussed in detail. So we will limit our considerations on how it is carried out, in fact quite simply because of the reference voltage controlled phase current regulation.

With the help of the inhibit-signals at outputs 5 and 8 of the controller, which are alternatively active only when the half-step control is programmed, the reference voltage is increased by the factor 1.41 with a very simple additional wiring (fig. 18), as soon as one of the two inhibit-signals switches LOW. This increases the current in the active motorphase proportionally to the reference voltage and compensates the torque loss in this position. Fig. 19 shows clearly that the diagram of the phase current is almost sinusoidal, in principle the ideal form of the current graph.

To sum up we may say that this half-step version offers most advantages. The motor works with poor resonance and a double position resolution at a torque, that is almost the same as that of the full-step.

BETTER GLIDING THAN STEPPING

If a stepper motor is supposed to work almost gliding and not step by step, the form of the phase current diagram has to be sinusoidal.

The advantages are very important :

- no more phenomena of resonance
- drastic noise reduction
- connected gearings and loads are treated with care
- the position resolution may be increased further.

However, the use of the L297 controller-unit described until now is no longer possible of the more semplified form of the phase current diagram the Controller may become simpler in its functions.

Fig. 20 shows us an example with the L6505 unit. This IC contains nothing more than the clocked phase current regulation which works according to the same principle as L297. The four control signals emitting continuously a full-step program are now generated directly by the microprocessor. In order to obtain a sinusoidal phase current course the reference voltage inputs of the Controller are modulated with sinusoidal half-waves.

The microprocessor that controls the direction of the current phase with the control signals also generates the two analog signals.

For many applications a microprocessor with dedicated digital to analog converters can be chosen. Eliminating the need for separate D/A circuits.

About 5 bit have proved to be the most suitable subdivision of the current within one full-step. A higher

resolution brings no measurable advantages. On the contrary, the converter clock frequency is already very high in case of low motor revolutions and very difficult to process by the processor-software. It is recommended to reduce the D/A resolution at high step frequencies.

In case of higher motor revolutions it is more convenient to operate only in full-step, since harmonic control is no longer an advantage as the current has only a triangular waveform in the motor winding.

PRECISION OF THE MICRO STEP

Any desired increase of the position resolution between the full step position has its physical limits. Those who think it is possible to resolve a 7.2° - stepper motor to 1.8° with the same precision as a

1.8° - motor in full-step will be received, as there are several limits :

The rise rate of the torque diagram corresponding to the twisting angle of the rotor for the 7.2° - motor is flatter by a factor of 4 then for the original 1.8° - motor. Consequently with friction or load moment, the position error is larger (fig. 21).

For most of the commercial motors there isn't a sufficiently precise, linear relationship between a sinusoidal-current-diagram and an exact micro step angle. The reason is a dishomogeneous magnetic field between the rotor and the two stator fields.

Above all, problems have to be expected with motors with high pole feeling. However, there are special stepper motors in which an optimized micro step operation has already been considered during the construction phase.

Figure 19 : The Half-step with Shaping Positioning is Achieved by Simply Changing Reference Voltages.

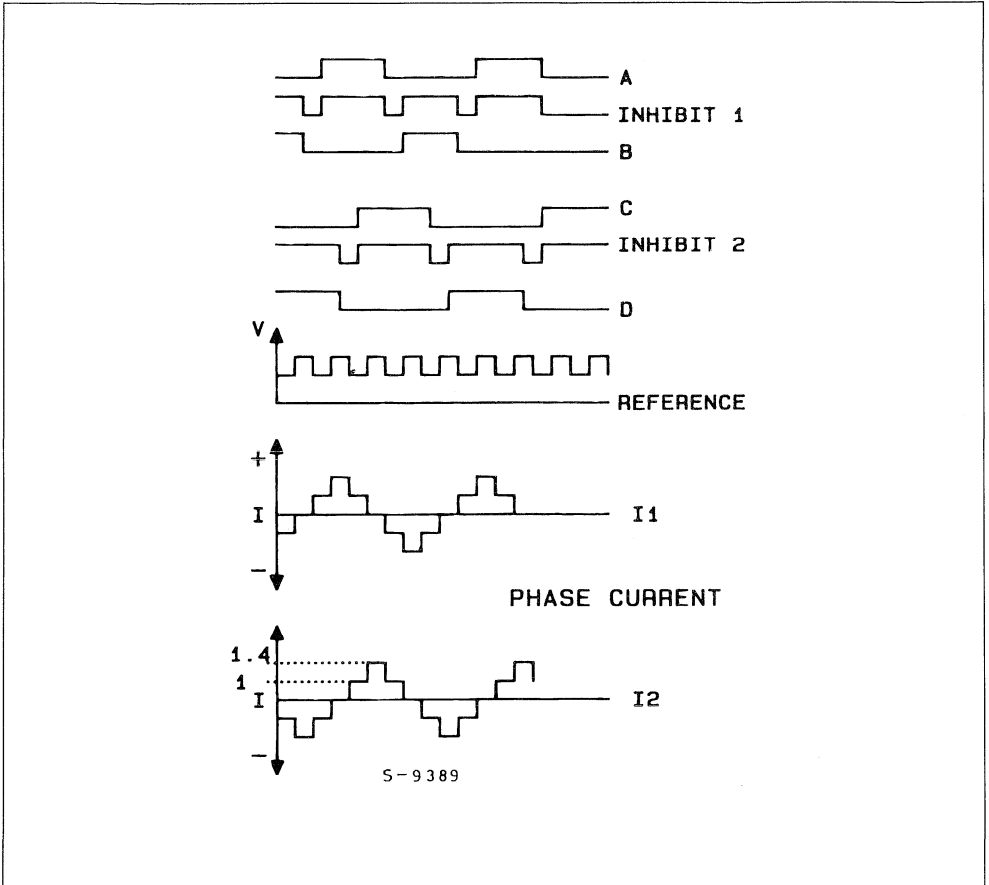
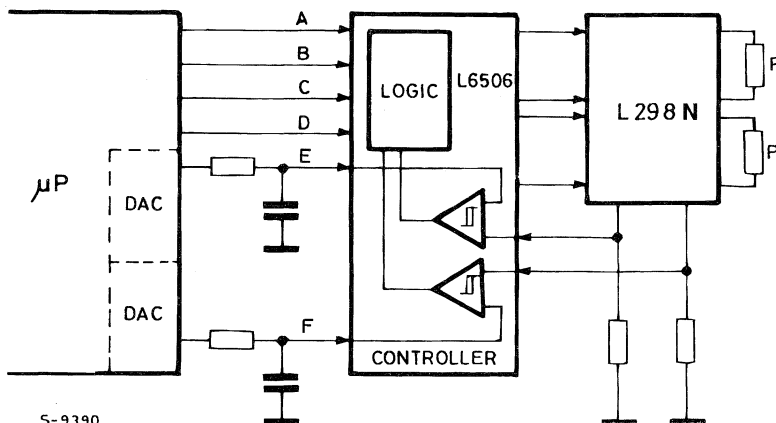
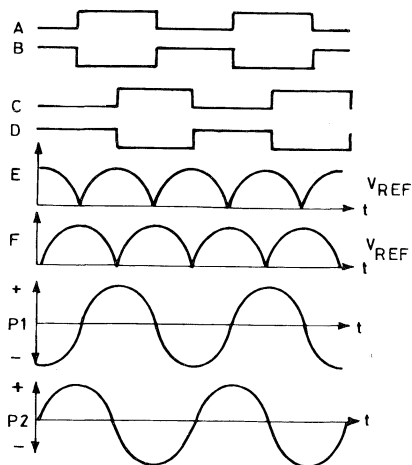


Figure 20 : L6506 Unit Gives The Possibility to Modulate Separately the Two Reference Voltage Inputs in Order to obtain a Sinusoidal Phase Current.

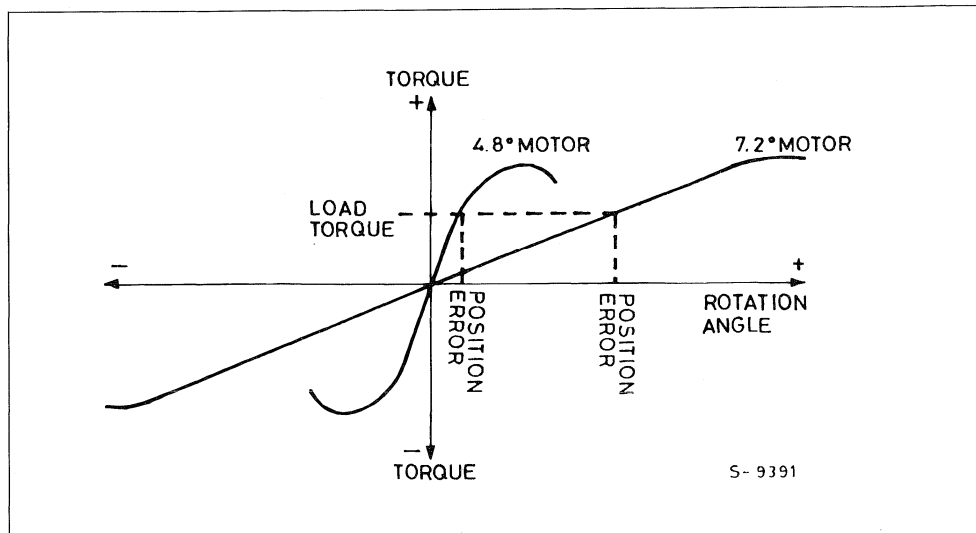


S-9390



S-9423

Figure 21 : Better Resolution is achieved with Low Degree Motor but More torque is delivered with high Degree Motor.



CONCLUSIONS

The above described application examples of modern integrated circuits show that output and efficiency of stepper motors may be remarkably increased without any excessive expense increase like before.

Working in limit areas, where improved electronics with optimized drive sequences allow the use of less expensive motors, it is even possible to obtain a cost reduction.

CONSTANT-CURRENT CHOPPER DRIVE UPS STEPPER-MOTOR PERFORMANCE

PULSE WIDTH-MODULATED DRIVE IMPROVES MOTOR TORQUE AND SPEED YET ADDS NO COMPLEXITY TO CIRCUIT

Designers opting to use a fractional-horsepower stepper motor in applications such as computer printers can improve the motor's efficiency and its torque and speed characteristics by using a constant-current pulse-width-modulated (PWM) chopper-drive circuit. What's more, for high-power drives, dedicated control chips and a constant-current chopper drive can be as simple to use as direct drive.

A basic problem for a directly driven stepper is that the motor winding's time constant (L/R) causes the current to increase slowly in the winding during each pulsed input. It may, therefore, never reach full-rated value, especially at high speed, or high pulsing rates, unless the voltage (V_s) across the terminals

is high. In the simplest stepper drive (see fig. 1a), transistor or Darlington switches sequentially activate the windings to drive the motor (see box, "Stepper motor basics").

This type of drive performs poorly because the supply voltage must be low so that the steady-state current is not excessive. As a result, the average winding current – and hence the torque – is very low at high drive motor speed.

Often, this problem is overcome by introducing a series resistance, thereby increasing the overall value by a factor of four - giving an $L/4R$ ratio - and also by increasing the supply voltage (see fig. 1b). This arrangement reduces the motor's time constant, which improves torque at high step rates. However such an approach is inefficient, because the series resistor constitutes a substantial waste of power.

Figure 1 : Common Unipolar Stepping Drives (a) Produce Insufficient Torque Output because Their Supply Voltage must be kept Low to Limit Current. Adding Series Resistance to an $L/4R$ Ratio (b) and raising the Supply Voltage Proportionately improves Torque Output, Especially at High Step Rates.

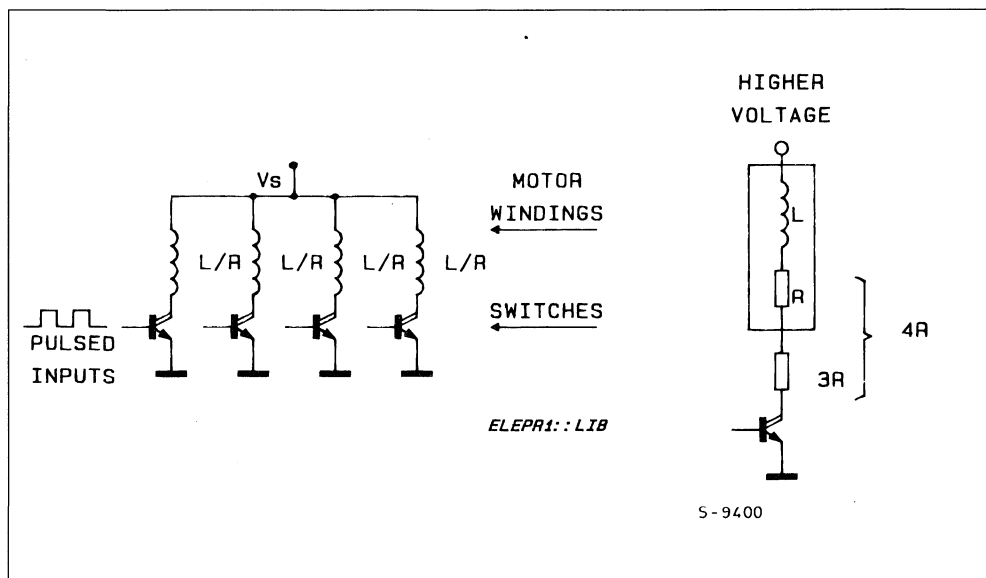
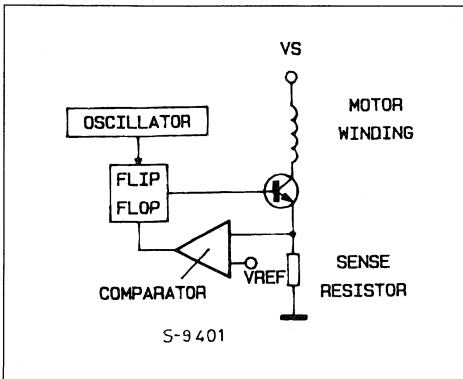


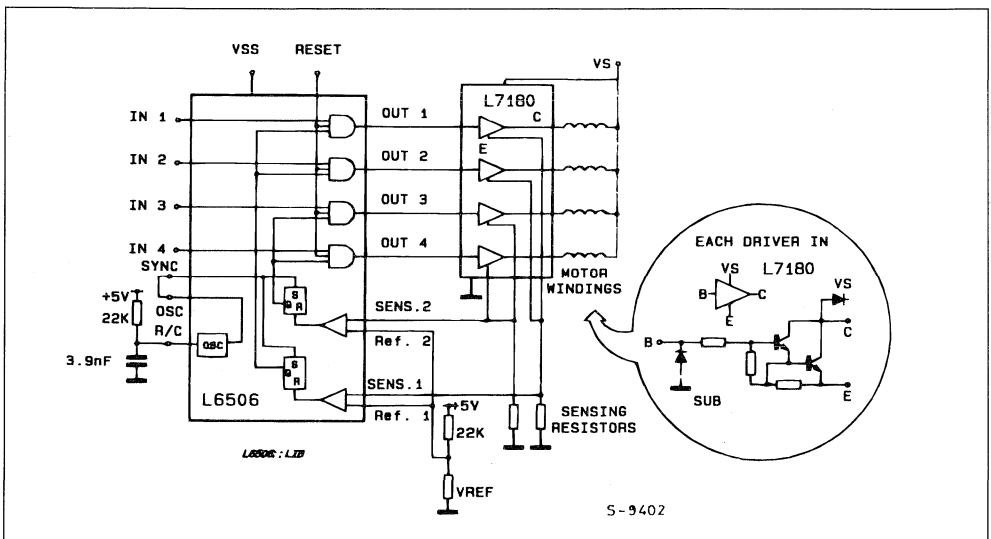
Figure 2 : A Pulse-width-modulated, or Chopper, Drive Overcomes most of the Problems of the Simpler Direct Drive or even Linear Constant-current Drives.



CONSTANT CURRENT IS BEST

Introducing a feedback loop to control the winding current is a better solution. Linear constant-current control is possible but is rarely used because of high power losses in the power stage. However, a pulse-width-modulation scheme – a chopper circuit – not only solves the L/R time-constant problem but cuts power dissipation too (see fig. 2).

Figure 3 : A simple Chopper Drive for a Unipolar Stepping Motor, can be assembled with Just Two Chips : a Quad Darlington Output Driver IC and Constant-current Feedback Controller IC.



A four-phase bifilar/hybrid unipolar stepper motor could use a quad Darlington like the L7180 as a chopper driver and a chip like the L6506 as a current controller (see fig. 3). The quad Darlington can drive motors at up to 1.4 A/phase - which is suitable for a carriage motor in a medium-size printer.

The L6506, which contains all the chopper circuitry, is simple to use. An external RC network sets the oscillator frequency, and a voltage divider (or trimmer) sets the reference voltages, and hence the phase currents. Normally an oscillator frequency of over 20 KHz is chosen to avoid motor noise. The maximum usable frequency depends on the L/R time constant of the motor.

Control signals for the four-phase inputs can be provided by a micro-computer chip or a simple repetitive sequence from a logic circuit. Note that the L6506 contains just two independent chopper-control loops - sufficient for a four-phase unipolar stepping motor because opposing windings never energize together.

DRIVING BIPOLAR MOTORS

Bipolar stepper motors, preferred for their better torque/weight ratio, however, are normally driven by H-bridge output stages. They enable a single-polarity supply to drive each motor winding end sequentially to achieve a polarity-reversal effect on the windings.

STEPPER-MOTOR BASICS

In computer-peripheral office-equipment applications, the most popular stepper motors are permanent-magnet types with two-phase bipolar windings or bifilar-wound unipolar windings. Stripped to the essentials, both types consist of a permanent-magnet rotor surrounded by stator poles carrying the windings.

A two-pole motor would have a step angle of 90° . However, most motors have multiple poles to reduce the step angle to a few degrees.

A bipolar permanent-magnet stepper motor has a single winding for each phase – and the current must be reversed to reverse the stator field. Bifilar/hybrid unipolar motors, however, have two windings wound in opposite directions for each phase, so that the field can be reversed with a single-polarity drive. Unipolar motors were once popular because the drive was simpler. But with today's dual bridge (H-bridge) ICs, it is just as easy to drive a bipolar motor.

In the most popular drive technique – two-phase-on – both phases are always energized, and the rotor poles are aligned with stator poles between steps. In another method – called the wave drive – one phase is energized at a time.

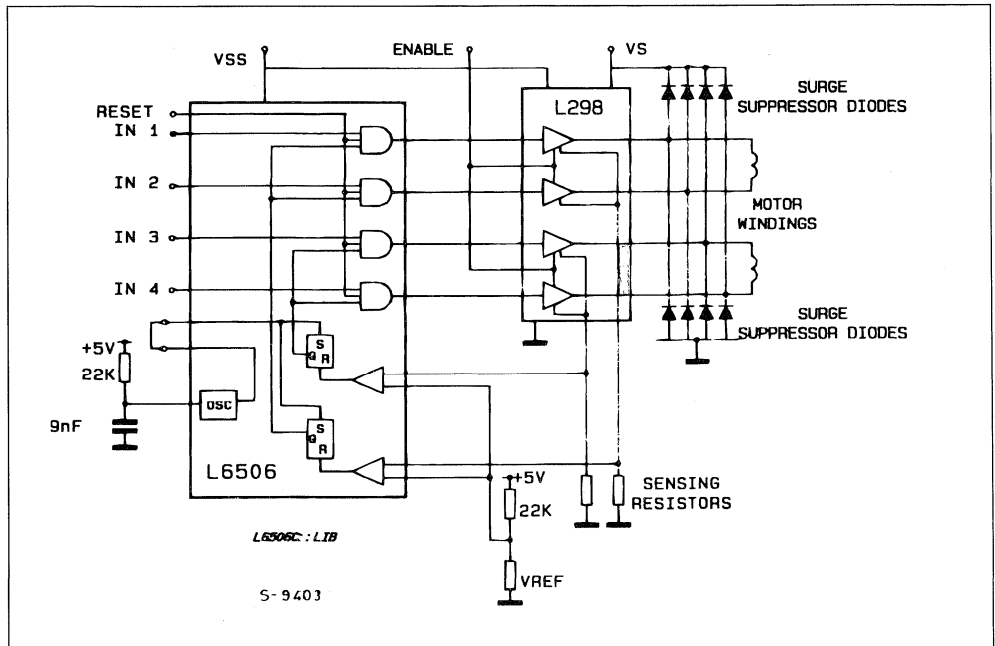
A third technique combines the two sequences and drives the motor one half-step at a time. Half-stepping is very useful because motor mechanically designed for very small step angles are much more complex – and costly – to build. It is more economical to use a 100-step motor in half steps rather than a 200-step motor in full step.

Recently designers have started microstepping, or driving the motor at one-quarter stepping rather or less. This type of operation can obtain fine step control without using mechanically complex motors with small step angles.

A two-phase bipolar motor needing up to 1A/phase can be driven by a single IC – the L298 dual bridge (see fig. 4). It contains two H-bridges with all the necessary level shifters and gates to directly interface low-level input logic signals.

As before, a complete chopper drive can be built by adding a current-controller chip and the necessary protective diodes, an RC network to define the oscillator frequency and a reference-voltage divider to set the current level. Four-phase signals to the controller are provided by a controlling microcomputer or by another dedicated controller chip – the L297 stepper-motor controller.

Figure 4 : A Dual-bridge IC Provides a Simple Power-stage Design Solution for a Bipolar Stepper Motor.



Containing an internal translator circuit controlled by step-and-direction inputs, the L297 motor controller (see fig. 5) allows operation in three modes : two-phase-on, half-step and wave-drive.

The normal two-phase-on mode is selected by a low level on the half/full input when the device has been reset to start.

Half-step drive is selected by a high level on the half/full step input. To initialize the wave-drive mode, the user disables the output stage (brings enable low), resets the device, steps the translator one step, brings half/full low, and then reenables the outputs.

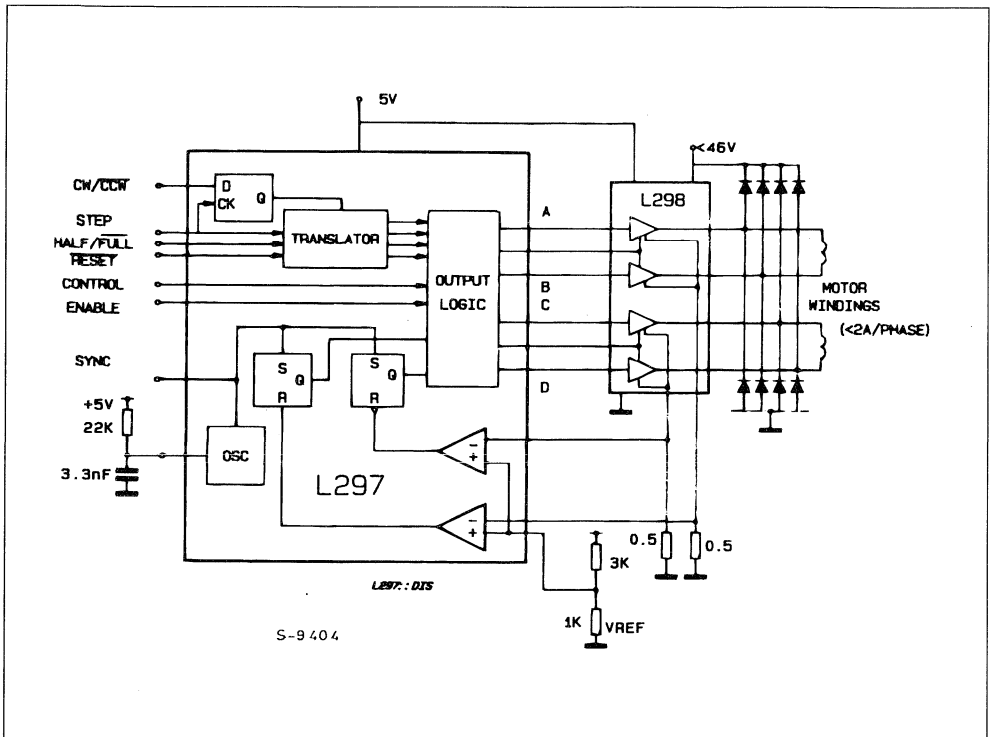
The L297 also lets the designer select either phase or inhibit chopping. Phase chopping provides lower

ripple and is suitable for unipolar motor, whereas inhibit chopping returns energy to the supply and is better for bipolar motors.

In applications such as printer-paper feed, the motor is often at rest. Since the full torque is not usually necessary to hold the motor in position, designers can save power by switching the current to a lower level between runs. With an L297 or L6506 control chip, this task can be done by simply switching the reference input between two levels.

Where several chopper drives are used in the same system, they should be synchronized to prevent inter-modulation effects. This is done by connecting the sync pins to one another and omitting the oscillator RC network on all but one device.

Figure 5 : Controlled by Step, Direction, and Mode Inputs, the L297 Stepper-motor Controller Chip Performs some of the Functions of a Controlling Microcomputer.



HANDLING HIGH CURRENT

For current drives greater than 2A/phase, the two bridges in an L298 IC can be paralleled by connecting inputs to the corresponding outputs. However, for a more equal distribution of the load and chip heating, driver 1 should be paralleled with driver 4, and driver 2 with driver 3. Additionally, total current should be derated by 0.5 A to allow for the maximum possible imbalance between the current in each bridge. Thus two L298s can drive motors rated at 3.5 A/phase.

A different configuration for microstepping stepper motors is employed in the PBL3717A control circuit. It contains all of the control and power circuitry for

one phase of a motor. An H-bridge output stage can drive motors rated at up to 1A/phase. Two of these devices are needed to drive a two-phase bipolar motor.

The output current level from the PBL3717A is set both by an analog-reference input and two logic inputs (I_1 and I_0), which select one of three preset current levels (the fourth combination disables the outputs stage). This feature implements the microstepping, in which several current levels are used to obtain very small step angles for even more precise control (but at the expense of a less regular torque). Unlike the L297 and L6506, the PBL3717A has a constant off-time chopper driver which is ideal for microstepping.

USING THE L6506 FOR CURRENT CONTROL OF STEPPING MOTORS

The L6506 is a linear integrated circuit designed to sense and control the current in stepping motors and other similar devices. When used in conjunction with power stages like the L293, L298N, or L7180 the chip set forms a constant current drive for inductive loads and performs all the interface functions from the control logic through the power stage.

The L6506 may be used with either two phase bipolar or four phase unipolar motor configurations. The circuit in figure 1 shows the L6506 used in conjunction with the L298N in a 2 phase bipolar stepper motor application. The circuit in figure 2 implements a similar 4 phase unipolar application.

CURRENT CONTROL LOGIC

In these two circuits, the L6506 is used to sense and control the current in each of the load windings. The

current is sensed by monitoring the voltage across a sense resistor (R_{sense}) and using a Pulse Width Modulated control to maintain the current at the desired value.

An on-chip oscillator drives the dual chopper and sets the operating frequency. An RC network on pin 1 sets the operating frequency, which is given by the equation :

$$f \approx \frac{1}{0.69 R_1 C_1} \quad (1)$$

The oscillator provides pulses to set the two flip-flops, which in turn cause the outputs to activate the power actuator. Once the outputs have been activated the current in the load starts to increase, limited by the inductive characteristic of the load.

Figure 1 : Application Circuit for Bipolar 2 Phase Stepper Motor.

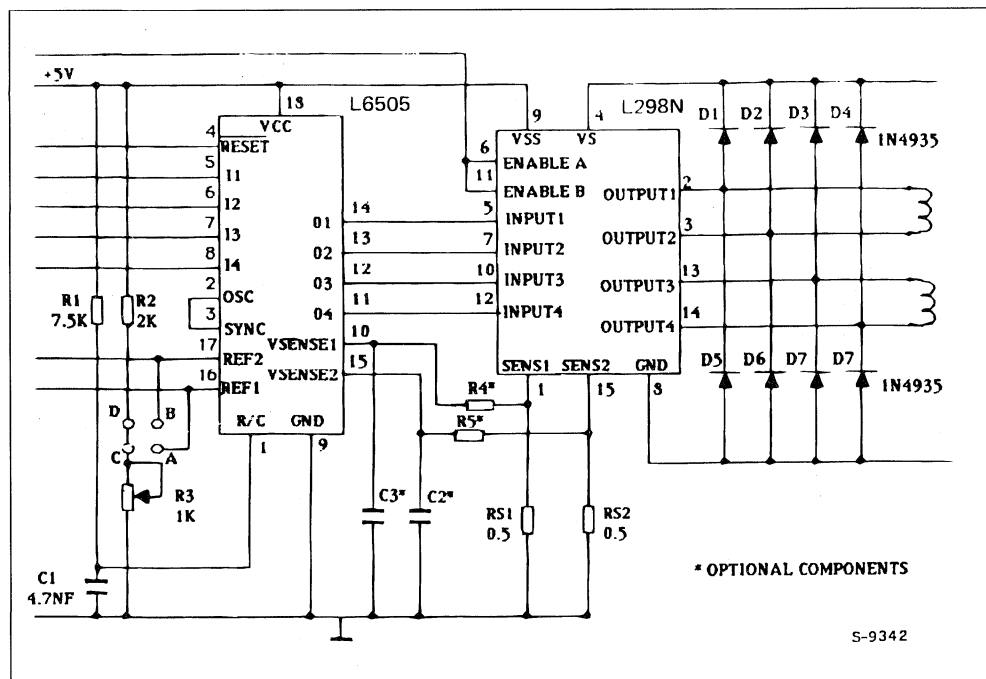
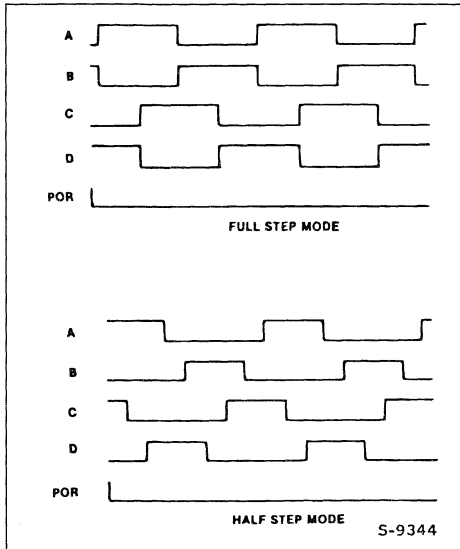
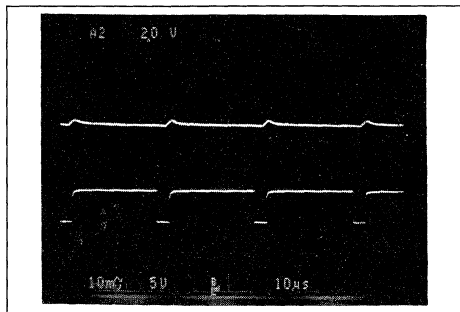


Figure 3 : Input Signal for Stepper Motor Drive.

When implementing a half step drive, both outputs of the L6506 will be low during the half step of one phase. This means a very long time is required for the current in the "off" winding to decay when driving bipolar motors.

Alternately, the power stage (L298) may be inhibited to put the output in the state and achieve a faster current decay.

Since separate V_{ref} inputs are provided for each channel, each of the loads may be programmed independently allowing the device to be used to implement microstepping or applications with different peak and hold currents. In this type of application, changing the reference voltage (V_{ref}) will change the load current, effectively implementing a transconductance amplifier.

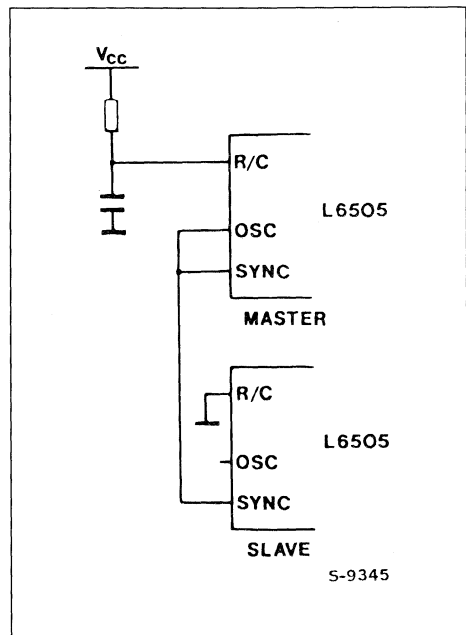
Figure 4 : Ripple Current in Bipolar Motors.

SYNCHRONIZING MULTIPLE DEVICES

Ground noise problems in multiple configurations can be avoided by synchronizing the oscillators. This may be done by connecting the sync pins of each of the devices with the oscillator output of the master device and connecting the R/C pin of the unused oscillators to ground as shown in figure 5. The devices may be synchronized to external circuits by applying synchronizing pulses to the sync pins. It should be noted, however, that the input pulse sets the minimum on time of the outputs and will therefore set a minimum output average current.

SELECTING THE OSCILLATOR COMPONENTS

When selecting the values for the external components for the oscillator one of the primary considerations is the operating frequency. In addition there is another important consideration for these components.

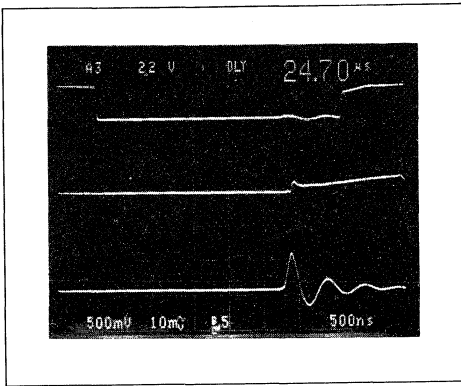
Figure 5 : Synchronizing Multiple Devices.

In many applications the reverse recovery current of the free wheeling diodes and of parasitic elements in the power stage will flow through the sensing resistor in addition to the load current. Also there is sometimes noise generated in the system when the power stage is switched on.

These two sources of error can fool the current limiting stage and make it appear to operate at a subharmonic of the desired frequency. With the proper selection of the oscillator components this behavior can be avoided.

The design of the L6506 is such that the flip-flops used in the device are set dominant so that whenever the sync input is low the Q output of the flip-flop will be high even if the reset is applied by the comparator at the same time. This characteristic of the flip-flops can be used to make the current sensing immune to the recovery currents and noise spikes that occur when the power devices switch. If the sync pulse is longer than the turn on delay time of the power stage, as shown in figure 6, these two sources of errors will be ignored.

Figure 6 : Load Current and Sync Pulse.



To select the proper values for the oscillator components a more detailed equation for the operating frequency and duty cycle of the oscillator is required. The required equations can be derived from the equivalent circuit for the oscillator section shown in figure 7.

As can be seen from figure 7, the full equation for the operating frequency includes not only the external resistance and capacitance but the internal discharge resistor as well. The full equation for the operating frequency is :

$$f = \frac{1}{0.69 C \left(R1 + \left(\frac{R1 Ri}{R1 + Ri} \right) \right)} \quad (3)$$

The equations for the active time of the sync pulse (T2), the inactive time of the sync signal (T1) and the duty cycle can also be found by looking at the figure 7 and are :

$$T2 = 0.69 C1 \frac{R1 Ri}{R1 + Ri} \quad (4)$$

$$T1 = 0.69 R1 C1 \quad (5)$$

$$DC = \frac{T2}{T1 + T2} \quad (6)$$

By substituting equations 4 and 5 into equation 6 and solving for the value of R1 the following equations for the external components can be derived :

$$R1 = \left(\frac{1}{DC} - 2 \right) Ri \quad (7)$$

$$C1 = \frac{T1}{0.69 R1} \quad (8)$$

Looking at equation 4 it can easily be seen that the minimum pulse width of T2 will occur when the value of Ri is at its minimum and the value of R1 at its maximum. Therefore, when evaluating equation 7 the minimum value for Ri of 700Ω (1 KΩ 30 %) should be used to guarantee the required pulse width.

For a typical application using the L298, which has a maximum turn on delay of 2.5 μs, with the L6506 consider the following operating points :

$$f = 25 \text{ KHz}$$

$$T1 + T2 = 40 \mu s$$

$$T2 \text{ min} = 3 \mu s$$

From equation 6 :

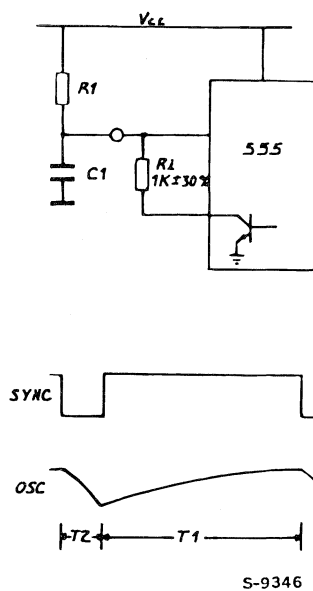
$$DC = \frac{3 \mu s}{40 \mu s} = 0.075$$

From equation 7 :

$$R1 = \left(\frac{1}{0.075} - 2 \right) 700 = 7.9 \text{ K}\Omega$$

From equation 8 :

$$C1 = \frac{37 \mu s}{(0.69) (7.9 \text{ K})} = 6.7 \text{ nF}$$

Figure 7 : Oscillator Circuit and Waveforms.

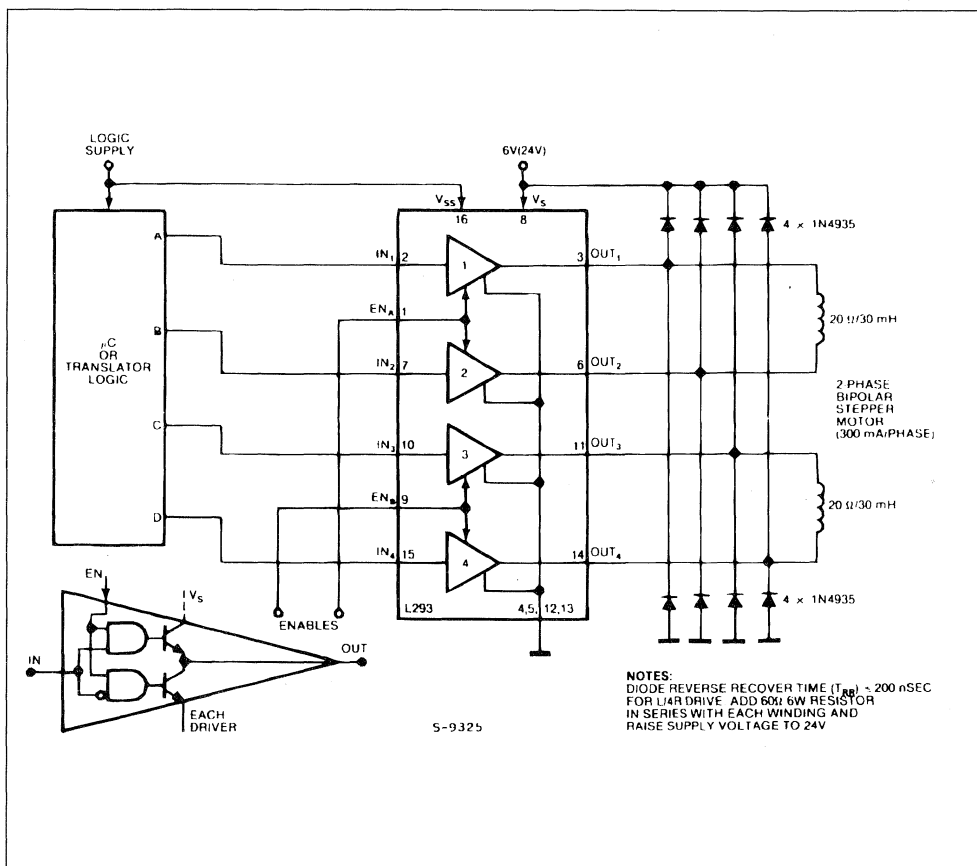
HIGH-POWER, DUAL-BRIDGE ICs EASE STEPPER-MOTOR-DRIVE DESIGN

In addition to simplifying design problems, a family of dedicated chips improves stepper-motor drive-circuit reliability by significantly reducing the component count.

The L293, L293E and L298N dual-bridge ICs (see box, "inside the dual-bridge ICs") significantly reduce the problems encountered in the design of stepper-motor drive circuitry. They can, for example, simplify the design and increase the efficiency of

constant-current choppers. And with a single chip replacing the transistors and predriver stages, circuit performance improves. Best of all, the devices have applications in complex as well as basic driver networks.

Figure 1 : The Simplest Stepper-motor Drive Technique is the Basic L/R Configuration. Adding Series Resistors and Raising the Supply to Make an L/4R Drive Improves Torque at High Steps rates but Reduces Efficiency.



SIMPLEST DESIGN IS AN L/R DRIVE

The simplest motor-drive configuration (fig. 1) consists of a μC that performs the translator function in software (see **box**, "Generating switching sequences") and drives the motor through a L293 dual bridge. Only eight external components are required ; these are diodes that protect the device's output transistors against inductive spikes generated when a winding de-energizes.

The L293 handles 1A continuous (for higher current

use and L298N). However, if you plan to run the motor continuously with two phases on, dissipation will be the limiting factor.

You can improve the performance of this basic L/R drive by increasing the series resistance and raising the supply voltage to restore the original phase current. At high speeds, torque improves, but efficiency decreases. Normally, you increase each winding's resistance by a factor of four through the addition of a 3R series resistance, resulting in the L/4R drive.

INSIDE THE DUAL-BRIDGE ICs

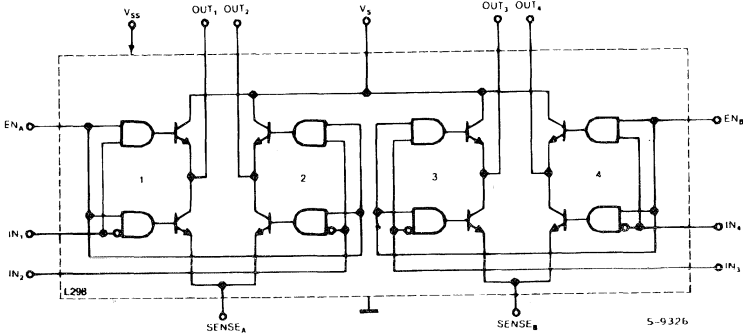
The L293, L293E and L298N (figure) contain two power-transistor bridges, predriver stages, control logic and protection circuitry. There's a control input for each bridge and an enable input for each half bridge ; inputs connect directly to μCs , CMOS or TTL. The ICs integrate level shifters with a separate logic-supply pin. For current sensing, the L293E and L298N have external emitter connections.

A single package drives a 2-phase bipolar stepper motor, challenging the assumption held by many that unipolar motors are easier to drive.

You can use a bipolar motor - simpler and less expensive than a unipolar motor - without building complex power stages. Furthermore, you don't have to worry about simultaneous conduction of a half bridge's source and sink transistors - a basic problem with discrete-component bridge circuits. Chip design makes it impossible for both transistors to be on at the same time.

Designers should also discard the mistaken idea that constant-current chopper drivers are complicated and expensive. You can build one with two bridge ICs and a few passive components.

Dual-bridge driver ICs reduce the parts count of bipolar stepper motors and simplify design. The schematic of the L298N is functionally similar to those of the L293 and L293E.



Type	I_o	$I_{o(PEAK)}$	V_s	Package	Sensing Connections
L293	1 A	1.5 A	36 V	16 DIP	
L293E	1 A	1.5 A	36 V	20 DIP	One Per Half Bridge
L298N	2 A	2.5 A	46 V	Multiwatt 15	One Per Bridge

MULTIPLE SUPPLIES BOOST PERFORMANCE

A dual-level supply also improves the performance of a basic L/R circuit. A high supply voltage yields good torque characteristics when the motor is running. A lower-than-rated voltage provides some holding torque when the motor is at rest, thereby saving power when the motor is idle.

Fig. 2 shows a suitable voltage-switch circuit. R_x sets the holding current, which can be low because a permanent magnet or hybrid stepper motor provides some holding torque at zero current. However, make certain the L293's motor-supply input never goes below the logic-supply voltage. While there's no danger of damaging the device, it's impossible to drive the output transistors correctly under such conditions.

The dual bridge's enable inputs offer a means of extending the chip's flexibility. For example, you can connect them directly to the logic supply - no resistors are needed - to enable the chip permanently. As an alternative, use the enable inputs to disable the motor during the power-on reset sequence.

In wave-drive and half-step modes, use the enable inputs to increase torque at high speeds. When a winding de-energizes, flux collapse is a function of the current-decay rate. During this decay, the de-energized winding opposes the efforts of the next winding in sequence, partially cancelling the torque.

You can minimize this effect by disabling a bridge only when the winding it drives is turned off ; because the $\Delta i/\Delta t$ of an inductor equals E/L , disabling the bridge accelerates the current decay. This action discharges the winding's stored energy through its supply and maintains the terminal voltage E at V_s plus two diode drops. If you were to leave the bridge enabled, the current would flow to ground through one diode and one transistor, and it would lower the terminal voltage. This scheme doesn't apply with drives with two phases on because no winding ever de-energizes.

Figure 2 : Switching the Supply to a Lower Voltage when the Motor is Idle Saves Current without Compromising Driving Power.

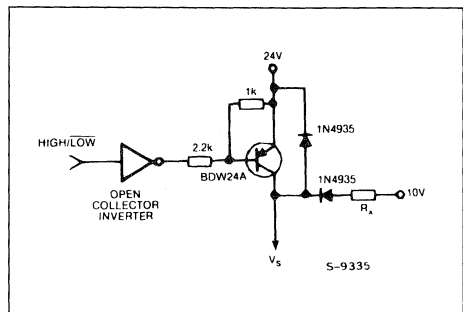
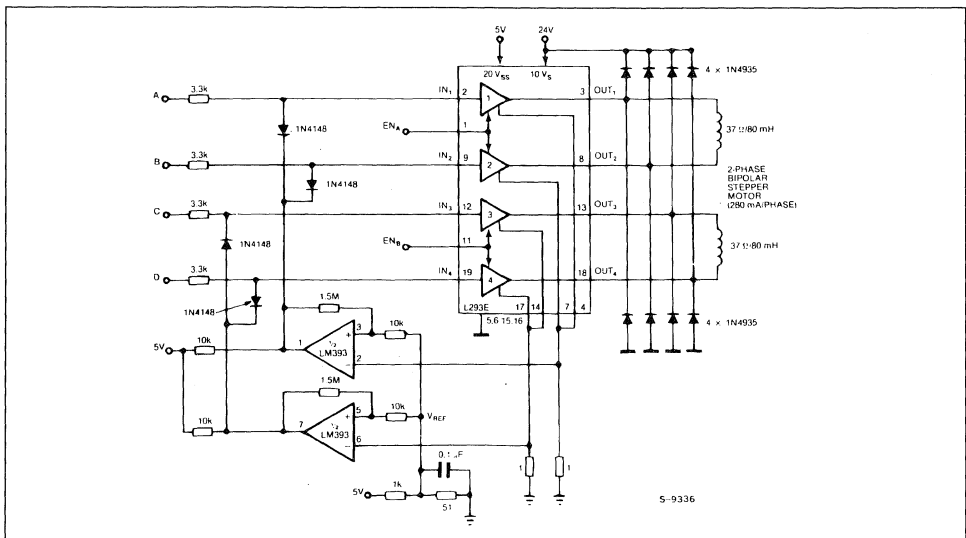


Figure 3 : Maintaining a Constant-average Phase Current this Fixed-ripple Chopper Provides Improved Performance and Efficiency V_{REF} Controls the Phase Current.

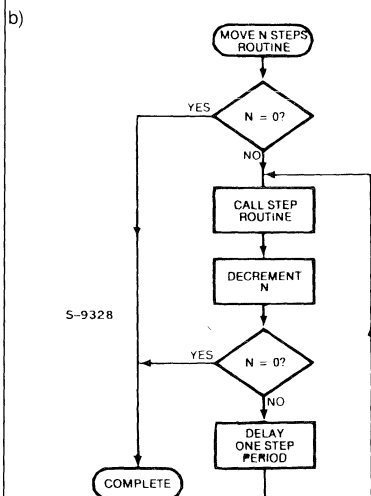
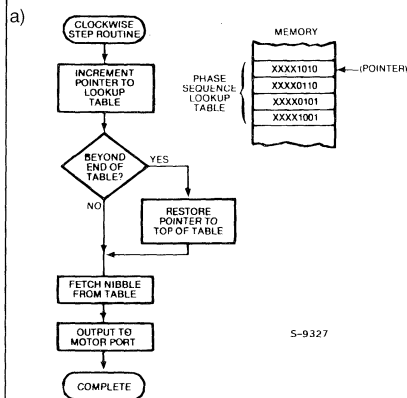


GENERATING SWITCHING SEQUENCES

In addition to selecting a motor and determining power-stage design, you must also decide how to generate the switching sequences that step the motor. Programming a μC or using a special piece of hardware called a transistor accomplishes this task.

Software translation is more economical, and it is the first choice for large-volume products. Fig. A shows a basic step procedure (a) that you can integrate into a routine (b); the routine executes a clockwise rotation of N steps at a fixed rate. The step rate is defined by a software loop, but you can also use programmed timer interrupts.

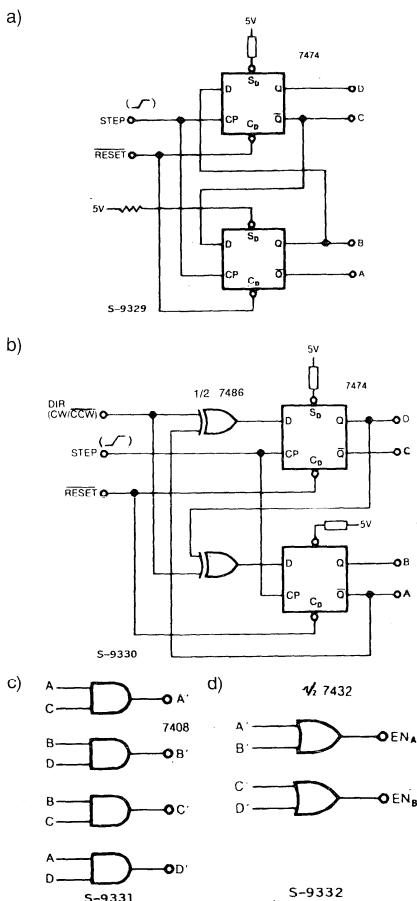
Fig. A : A μC can generate the phase sequence (a) for a stepper motor. A routine (b) expands a single-step routine into one that executes a move of N steps.



A simpler approach uses the software equivalent of a shift register. For example, you can load a 99 (hex) into a register and take the phases from bits 0 to 3. A Rotate Left instruction yields a clockwise step; a Rotate Right instruction causes a counterclockwise move.

When software translation ties up your μC , lighten the load by adding a hardware translator. In applications involving unidirectional motors, this logic circuit (fig. B) requires only one pulse for each step; you'll also need a direction signal (b) if your motor rotates in both directions. By adding a 7408 to a 2-phase translator, you can satisfy a wave-drive application (c), while the addition of two OR gates provides fast turn-off in wave-drive mode.

Fig. B : Built a simple 2-phase hardware translator using a dual flip-flop, for single (a) or bidirectional (b) rotation. Add some extra ICs for wave-drive signals (c) and to provide fast turn-off (d).



Often a μ C controls the translator, setting the direction line and providing a pulse for each step. Software is thus simplified, and if you use a programmed interrupt scheme, the μ C is free to handle other tasks. Fig. C describes an absolute-positioning routine for a step with a direction-control translator; Fig. D outlines how programmed timer interrupts are used to relieve the burden on the C.

Figure C : For use with a Hardware Translator this a Absolute-positioning Routine Sets the Direction Line and Sends the Appropriate Number of Step Pulses.

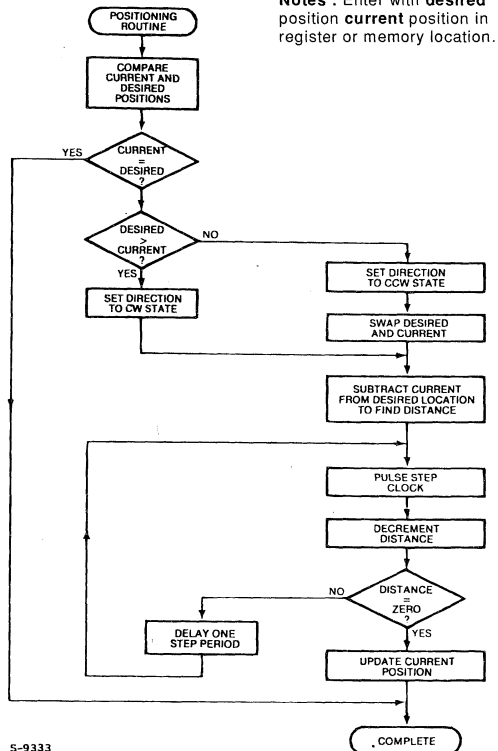
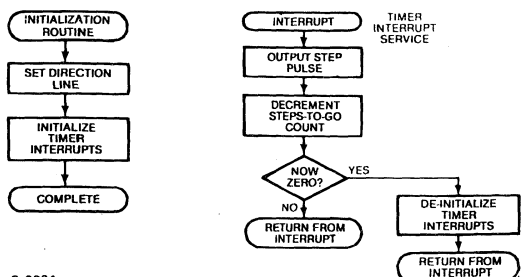


Figure D : To Set a motor Step Rate, used Programmed Timer Interrupts in Place of Software Timing Loops.



CHOPPER CIRCUIT OFFERS MORE ENHANCEMENTS

Adding a chopper circuit to maintain a constant-average phase current improves performance and efficiency. Fig. 3 shows a simple constant-current drive that employs a dual bridge, dual comparator and a few passive components. This circuit requires an L293E, because this dual-bridge IC offers access to the lower emitter connections, thus letting you insert current-sensing resistors.

Operation of this fixed-ripple chopper drive is straightforward. When the μC or translator activates a bridge, the increasing load current raises the voltage across the sensing resistor until it equals the comparator's reference voltage. The comparator then switches, clamping the translator signals through the diodes to deactivate the bridge. As the current decays, the voltage across the sensing resistor decreases until it equals the comparator's lower threshold. The comparator switches again, allowing the μC or translator to activate a bridge and restart the cycle. As long as the translator drives the bridge, this sequence repeats to provide a constant-average phase current with fixed ripple.

V_{ref} adjusts the lower current limit, while the comparator's hysteresis sets the ripple, and hence the peak current. Although a divider establishes the value of V_{ref} in this case, you can employ the dual-supply design approach and switch V_{ref} to a lower value when the motor is idle. In addition, use of a D/A converter establishes V_{ref} for micro-stepping applications. This drive circuit, with its fixed-ripple current characteristics, is well suited for such service.

FIXED-FREQUENCY CHOPPER IS MOTOR INDEPENDENT

Fig. 3's drive has some disadvantages. First, the chopper frequency depends on motor characteristics, and these parameters vary from unit to unit. In addition, it's impossible to synchronize the choppers, and this shortcoming can cause trouble on the ground plane.

Using a flip flop/comparator arrangement (fig. 4) to develop a fixed-frequency chopper overcomes these problems. In this circuit, the NE555 timer generates negative pulses that reset the flip flops to enable the phase-control signals from the transla-

Figure 4 : This Fixed-frequency Constant-current Chopper Driver Enables the Synchronization of Several Drives, thus Minimizing Potential Ground-plane Problems.

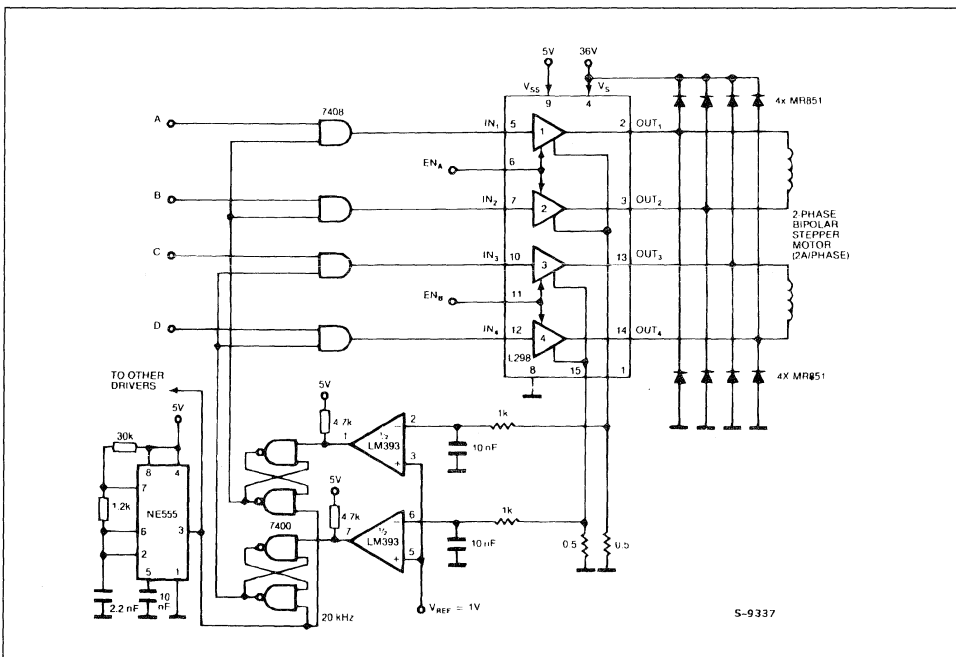
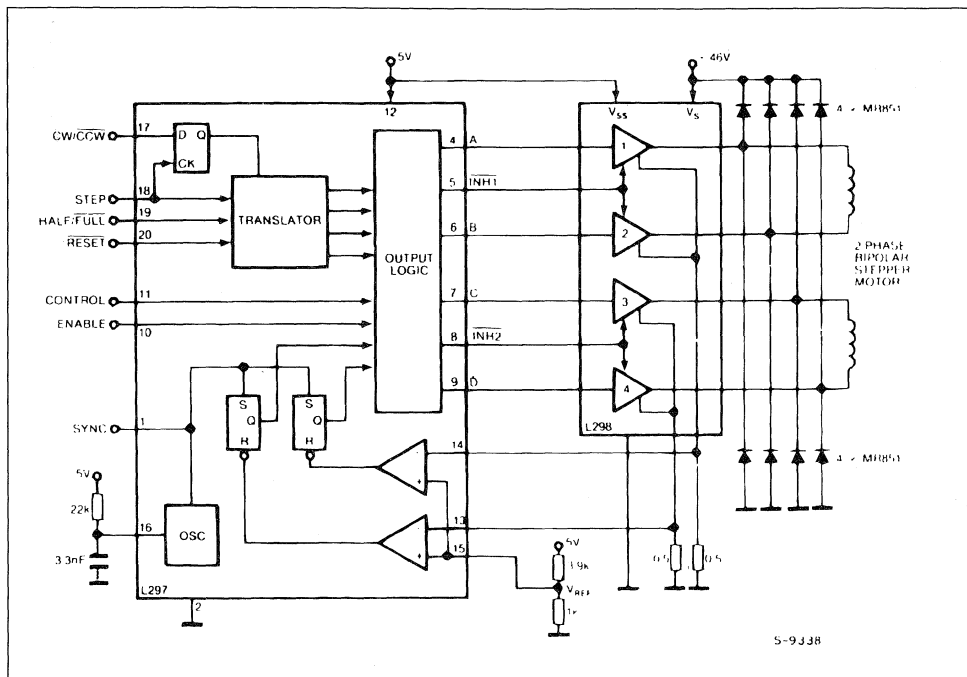


Figure 5 : A Special Translator-chopper Control Circuit cuts the Drivers Components Count to the Minimum.



tor. If these signals are set to energize a winding, the current in that winding rises until the voltage across the sensing resistor switches the comparator, thus setting the flip flop. This disables the phase signals and deactivates the bridge. Current in the winding falls until the next clock pulse resets the flip flop, and the sequence repeats to maintain a constant current.

CONTROLLER IC REDUCES COMPONENT COUNT

If you're using a hardware translation and constant-current choppers, you can further reduce the component count by using a controller chip such as the L297 – a 20-pin DIP that houses a translator and a

dual fixed-frequency chopper circuit. Under the control of step and direction inputs, the L297 generates normal, wave-drive and half-step sequences.

As shown in fig. 5, the controller connects directly to a dual bridge. External component requirements are minimal : and RC network to set the chopper frequency and a resistive divider to establish the comparator reference voltage (V_{ref}).

To accommodate motors with a phase current as great as 3.5 A, replace the single dual-bridge IC with two devices configured in parallel (input to input, enable to enable, etc) to form a single bridge. It's extremely important that you pair the half bridges – 1 with 4 and 2 with 3 – to ensure optimum current sharing.

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THE L297 STEPPER MOTOR CONTROLLER

The L297 integrates all the control circuitry required to control bipolar and unipolar stepper motors. Used with a dual bridge driver such as the L298N forms a complete microprocessor-to-bipolar stepper motor interface. Unipolar stepper motor can be driven with an L297 plus a quad darlington array. This note describes the operation of the circuit and shows how it is used.

The L297 Stepper Motor Controller is primarily intended for use with an L298N or L293E bridge driver in stepper motor driving applications.

It receives control signals from the system's controller, usually a microcomputer chip, and provides all the necessary drive signals for the power stage. Additionally, it includes two PWM chopper circuits to regulate the current in the motor windings.

With a suitable power actuator the L297 drives two phase bipolar permanent magnet motors, four phase unipolar permanent magnet motors and four phase variable reluctance motors. Moreover, it handles normal, wave drive and half step drive modes. (This is all explained in the section "Stepper Motor Basics").

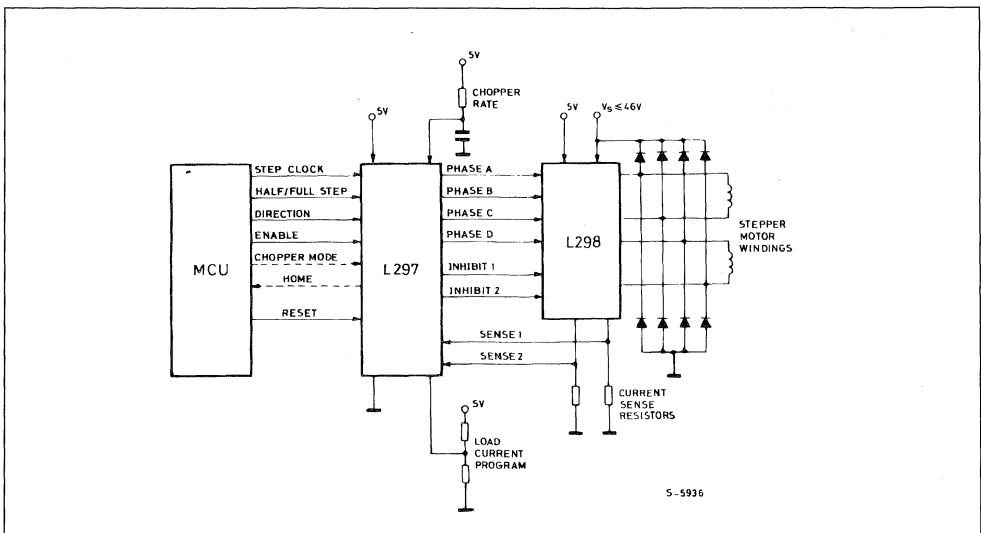
Two versions of the device are available : the regular

L297 and a special version called L297A. The L297A incorporates a step pulse doubler and is designed specifically for floppy-disk head positioning applications.

ADVANTAGES

The L297 + driver combination has many advantages : very few components are required (so assembly costs are low, reliability high and little space required), software development is simplified and the burden on the micro is reduced. Further, the choice of a two-chip approach gives a high degree of flexibility-the L298N can be used on its own for DC motors and the L297 can be used with any power stage, including discrete power devices (it provides 20mA drive for this purpose).

Figure 1 : In this typical configuration an L297 stepper motor controller and L298 dual bridge driver combine to form a complete microprocessor to bipolar stepper motor interface.



For bipolar motors with winding currents up to 2.5A the L297 should be used with the L298N ; for winding currents up to 1A the L293E is recommended (the L293 will also be useful if the chopper isn't needed). Higher currents are obtained with power transistors or darlingtontons and for unipolar motors a darlington array such as the L7180 is suggested. The block diagram, figure 1, shows a typical system.

Applications of the L297 can be found almost everywhere ... printers (carriage position, daisy position, paper feed, ribbon feed), typewriters, plotters, numerically controlled machines, robots, floppy disk drives, electronic sewing machines, cash registers, photocopiers, telex machines, electronic carburetors, telecopiers, photographic equipment, paper tape readers, optical character recognisers, electric valves and so on.

The L297 is made with SGS' analog/digital compatible I^2L technology (like Zodiac) and is assembled in a 20-pin plastic DIP. A 5V supply is used and all signal lines are TTL/CMOS compatible or open collector transistors. High density is one of the key features of the technology so the L297 die is very compact.

THE L298N AND L293E

Since the L297 is normally used with an L298 or L293E bridge driver a brief review of these devices will make the rest of this note easier to follow.

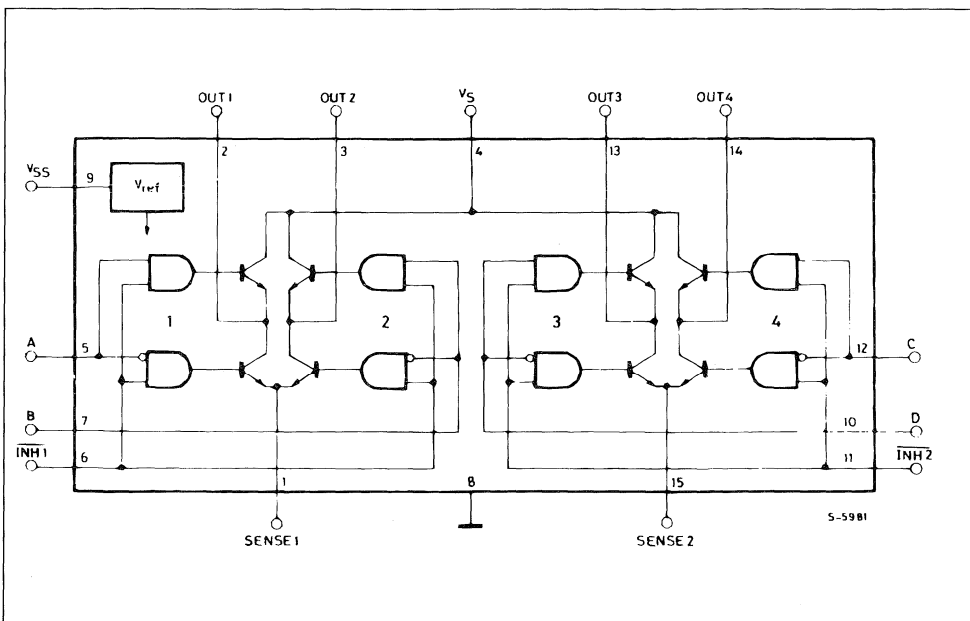
The L298N and L293E contain two bridge driver stages, each controlled by two TTL-level logic inputs and a TTL-level enable input. In addition, the emitter connections of the lower transistors are brought out to external terminals to allow the connection of current sensing resistors (figure 2).

For the L298N SGS' innovative ion-implanted high voltage/high current technology is used, allowing it to handle effective powers up to 200W (46V supply, 2.5A per bridge). A separate 5V logic supply input is provided to reduce dissipation and to allow direct connection to the L297 or other control logic.

In this note the pins of the L298N are labelled with the pin names of the corresponding L297 terminals to avoid unnecessary confusion.

The L298N is supplied in a 15-lead Multiwatt plastic power package. Its smaller brother, the functionally identical L293E, is packaged in a Powerdip - a copper frame DIP that uses the four center pins to conduct heat to the circuit board copper.

Figure 2 : The L298N contains two bridge drivers (four push pull stages) each controlled by two logic inputs and an enable input. External emitter connections are provided for current sense resistors. The L293E has external connections for all four emitters.



STEPPER MOTOR BASICS

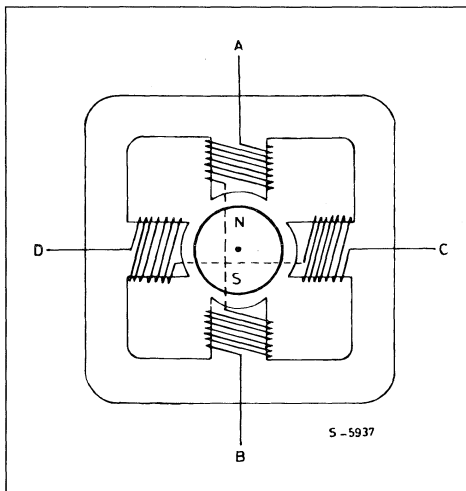
There are two basic types of stepper motor in common use : permanent magnet and variable reluctance. Permanent magnet motors are divided into bipolar and unipolar types.

BIPOLAR MOTORS

Simplified to the bare essentials, a bipolar permanent magnet motor consists of a rotating permanent magnet surrounded by stator poles carrying the windings (figure 3). Bidirectional drive current is used and the motor is stepped by switching the windings in sequence.

For a motor of this type there are three possible drive sequences.

Figure 3 : Greatly simplified, a bipolar permanent magnet stepper motor consist of a rotating magnet surrounded by stator poles as shown.



The first is to energize the windings in the sequence AB/CD/BA/DC (BA means that the winding AB is energized but in the opposite sense). This sequence is known as "one phase on" full step or wave drive

mode. Only one phase is energized at any given moment (figure 4a).

The second possibility is to energize both phases together, so that the rotor always aligns itself between two pole positions. Called "two-phase-on" full step, this mode is the normal drive sequence for a bipolar motor and gives the highest torque (figure 4b).

The third option is to energize one phase, then two, then one, etc., so that the motor moves in half step increments. This sequence, known as half step mode, halves the effective step angle of the motor but gives a less regular torque (figure 4c).

For rotation in the opposite direction (counter-clockwise) the same three sequences are used, except of course that the order is reserved.

As shown in these diagrams the motor would have a step angle of 90°. Real motors have multiple poles to reduce the step angle to a few degrees but the number of windings and the drive sequences are unchanged. A typical bipolar stepper motor is shown in figure 5.

UNIPOLAR MOTORS

A unipolar permanent magnet motor is identical to the bipolar machine described above except that bifilar windings are used to reverse the stator flux, rather than bidirectional drive (figure 6).

This motor is driven in exactly the same way as a bipolar motor except that the bridge drivers are replaced by simple unipolar stages - four darlington or a quad darlington array. Clearly, unipolar motors are more expensive because they have twice as many windings. Moreover, unipolar motors give less torque for a given motor size because the windings are made with thinner wire. In the past unipolar motors were attractive to designers because they simplify the driver stage. Now that monolithic push pull drivers like the L298 are available bipolar motors are becoming more popular.

All permanent magnet motors suffer from the counter EMF generated by the rotor, which limits the rotation speed. When very high slewing speeds are necessary a variable reluctance motor is used.

Figure 4 : The three drive sequences for a two phase bipolar stepper motor. Clockwise rotation is shown.

Figure 4a : Wave drive (one phase on).

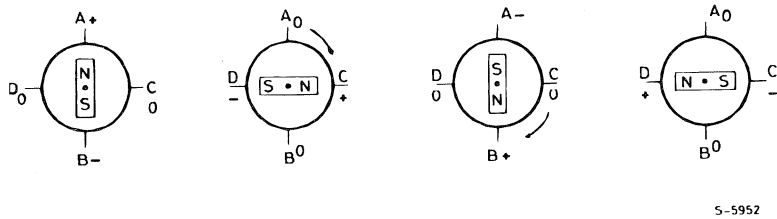


Figure 4b : Two phase on drive.

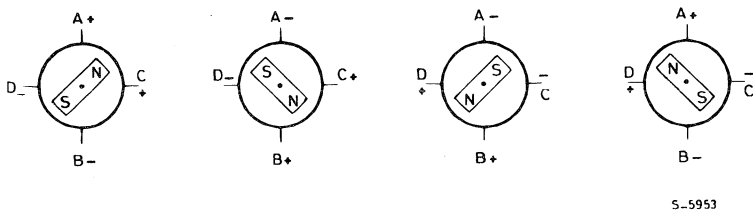


Figure 4c : Half step drive.

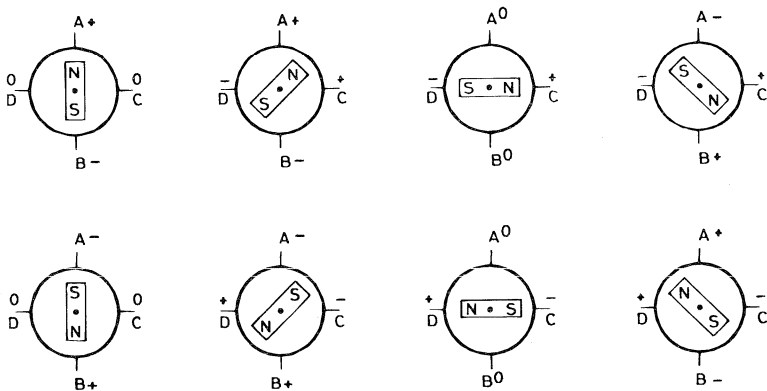


Figure 5 : A real motor. Multiple poles are normally employed to reduce the step angle to a practical value. The principle of operation and drive sequences remain the same.

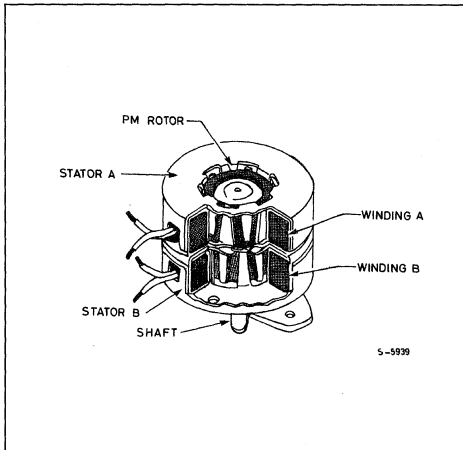
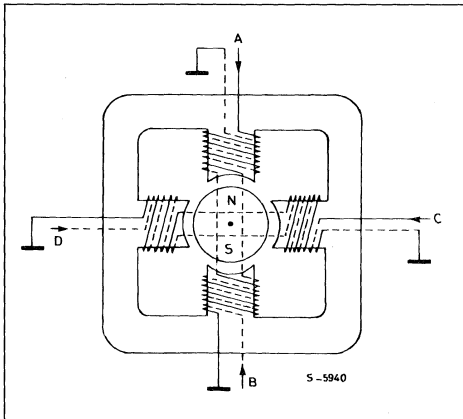


Figure 6 : A unipolar PM motor uses bifilar windings to reverse the flux in each phase.



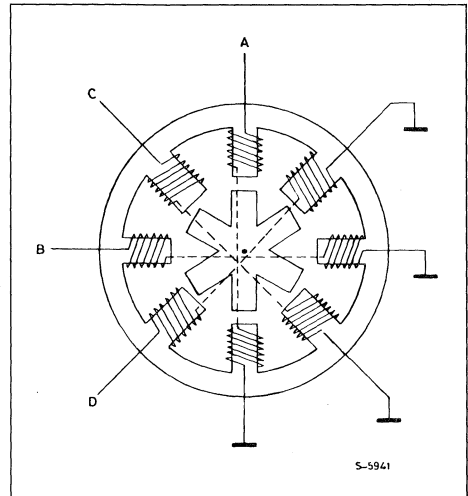
VARIABLE RELUCTANCE MOTORS

A variable reluctance motor has a non-magnetized soft iron rotor with fewer poles than the stator (figure 7). Unipolar drive is used and the motor is stepped by energizing stator pole pairs to align the rotor with the pole pieces of the energized winding. Once again three different phase sequences can be used. The wave drive sequence is A/C/B/D ; two-

phase-on is AC/CB/BD/DA and the half step sequence is A/AC/C/BC/B/BD/D/DA. Note that the step angle for the motor shown above is 15 °, not 45 °.

As before, practical motors normally employ multiple poles to give a much smaller step angle. This does not, however, affect the principle of operation of the drive sequences.

Figure 7 : A variable reluctance motor has a soft iron rotor with fewer poles than the stator. The step angle is 15 ° for this motor.



GENERATING THE PHASE SEQUENCES

The heart of the L297 block diagram, figure 8, is a block called the translator which generates suitable phase sequences for half step, one-phase-on full step and two-phase-on full step operation. This block is controlled by two mode inputs – direction (CW/ CCW) and HALF/ FULL – and a step clock which advances the translator from one step to the next.

Four outputs are provided by the translator for subsequent processing by the output logic block which implements the inhibit and chopper functions.

Internally the translator consists of a 3-bit counter plus some combinational logic which generates a basic eight-step gray code sequence as shown in figure 9. All three drive sequences can be generated easily from this master sequence. This state sequence corresponds directly to half step mode, selected by a high level on the HALF/ FULL input.

The output waveforms for this sequence are shown in figure 10.

Note that two other signals, $\overline{\text{INH1}}$ and $\overline{\text{INH2}}$ are generated in this sequence. The purpose of these signals is explained a little further on.

The full step modes are both obtained by skipping alternate states in the eight-step sequence. What happens is that the step clock bypasses the first stage of the 3-bit counter in the translator. The least significant bit of this counter is not affected there-

fore the sequence generated depends on the state of the translator when full step mode is selected (the HALF/ FULL input brought low).

If full step mode is selected when the translator is at any odd-numbered state we get the two-phase-on full step sequence shown in figure 11.

By contrast, one-phase-on full step mode is obtained by selecting full step mode when the translator is at an even-numbered state (figure 12).

Figure 8 : The L297 contains translator (phase sequence generator), a dual PWM chopper and output control logic.

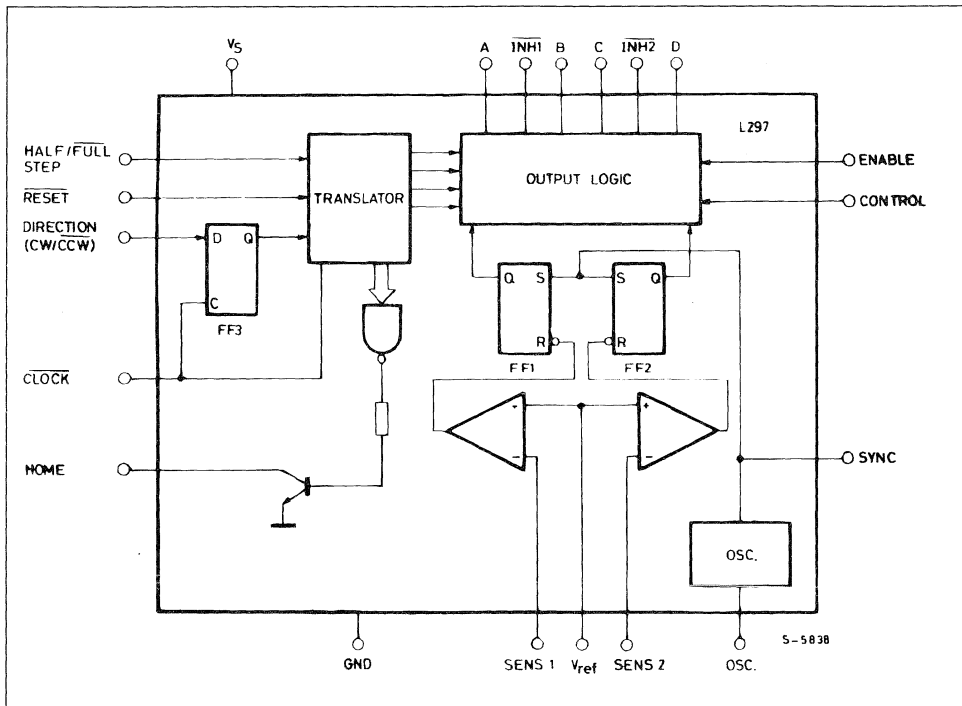


Figure 9 : The eight step master sequence of the translator. This corresponds to half step mode. Clockwise rotation is indicated.

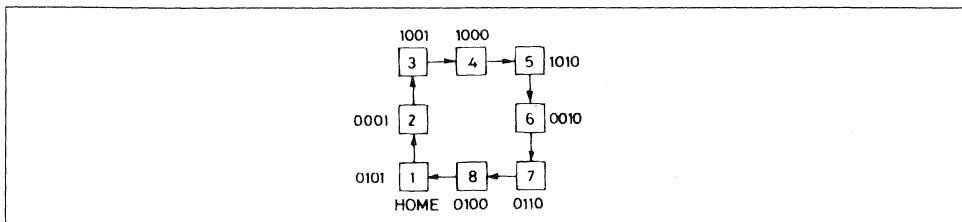


Figure 10 : The output waveforms corresponding to the half step sequence. The chopper action is not shown.

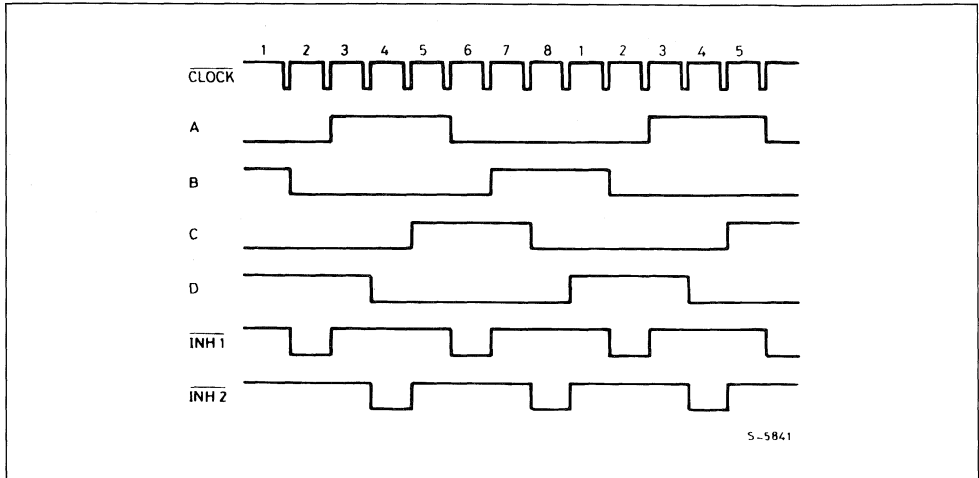


Figure 11 : State sequence and output waveforms for the two phase on sequence. $\overline{\text{INH}}1$ and $\overline{\text{INH}}2$ remain high throughout.

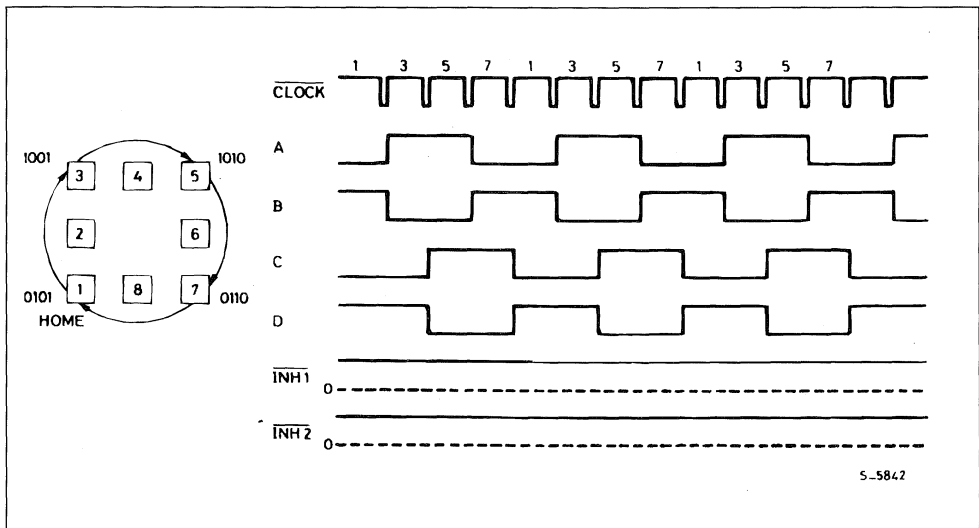
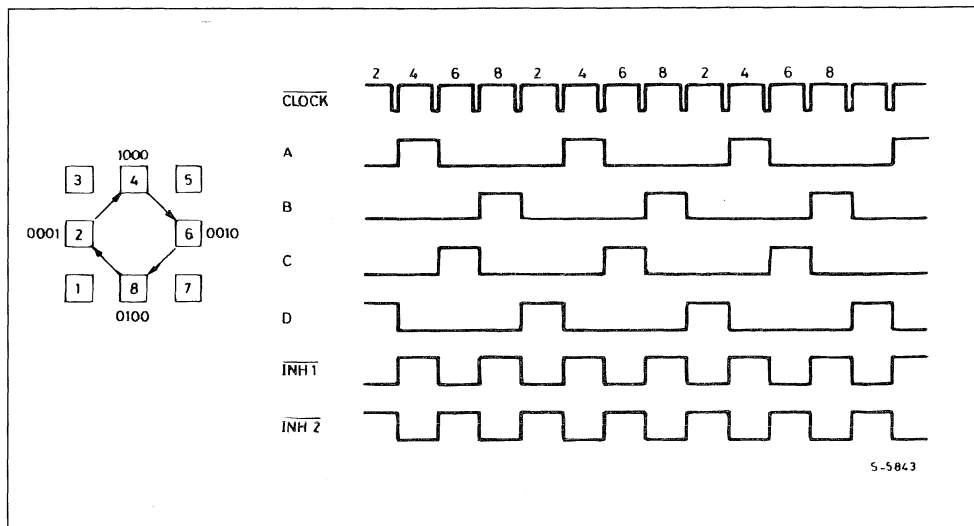


Figure 12 : State Sequence and Output Waveforms for Wave Drive (one phase on).

INH1 AND INH2

In half step and one-phase-on full step modes two other signals are generated : INH1 and INH2. These are inhibit signals which are coupled to the L298N's enable inputs and serve to speed the current decay when a winding is switched off.

Since both windings are energized continuously in two-phase-on full step mode no winding is ever switched off and these signals are not generated.

To see what these signals do let's look at one half of the L298N connected to the first phase of a two-phase bipolar motor (figure 13). Remember that the L298N's A and B inputs determine which transistor in each push pull pair will be on. INH1, on the other hand, turns off all four transistors.

Assume that A is high, B low and current flowing through Q1, Q4 and the motor winding. If A is now brought low the current would recirculate through D2, Q4 and R_s , giving a slow decay and increased dissipation in R_s . If, on a other hand, A is brought low and INH1 is activated, all four transistors are turned off. The current recirculates in this case from ground to V_s via D2 and D3, giving a faster decay thus allowing faster operation of the motor. Also, since the recirculation current does not flow through R_s , a less expensive resistor can be used.

Exactly the same thing happens with the second winding, the other half of the L298 and the signals C, D and INH2.

The $\overline{\text{INH1}}$ and $\overline{\text{INH2}}$ signals are generated by OR functions :

$$A + B = \overline{\text{INH1}} \quad C + D = \overline{\text{INH2}}$$

However, the output logic is more complex because inhibit lines are also used by the chopper, as we will see further on.

OTHER SIGNALS

Two other signals are connected to the translator block : the RESET input and the HOME output

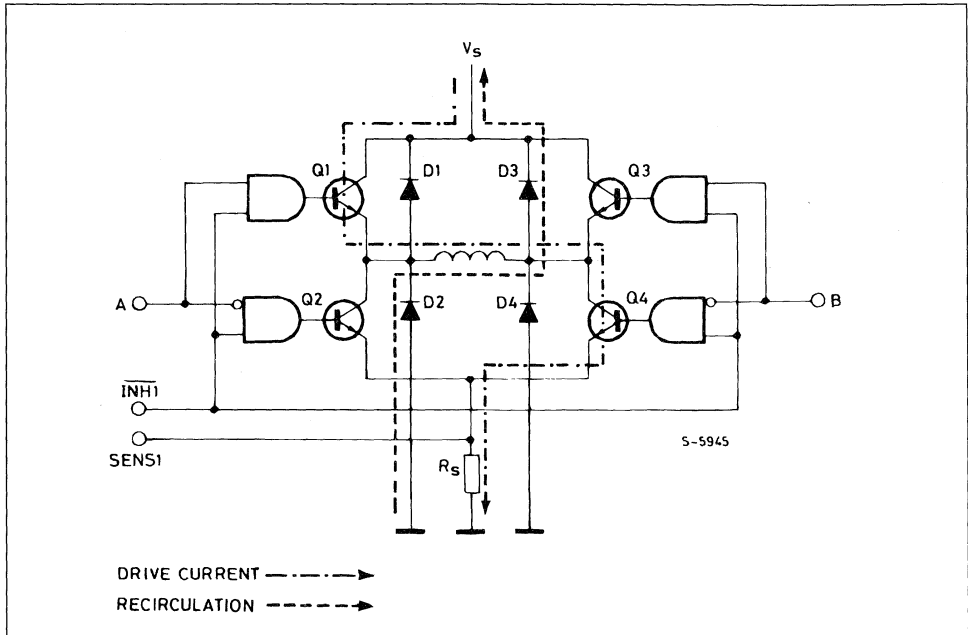
RESET is an asynchronous reset input which restores the translator block to the home position (state 1, ABCD = 0101). The HOME output (open collector) signals this condition and is intended to the ANDed with the output of a mechanical home position sensor.

Finally, there is an ENABLE input connected to the output logic. A low level on this input brings INH1, INH2, A, B, C and D low. This input is useful to disable the motor driver when the system is initialized.

LOAD CURRENT REGULATION

Some form of load current control is essential to obtain good speed and torque characteristics. There are several ways in which this can be done – switching the supply between two voltages, pulse rate modulation chopping or pulse width modulation chopping.

Figure 13 : When a Winding is switched off the Inhibit Input is activated to speed Current Decay. If this were not done the Current would recirculate through D2 and Q4 in this Example. Dissipation in R_s is also reduced.

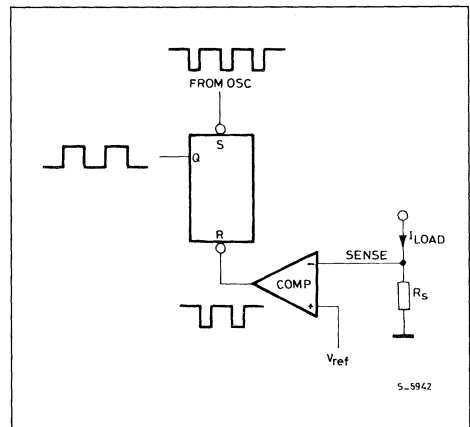


The L297 provides load current control in the form of two PWM choppers, one for each phase of a bipolar motor or one for each pair of windings for a unipolar motor. (In a unipolar motor the A and B windings are never energized together so they can share a chopper; the same applies to C and D).

Each chopper consists of a comparator, a flip flop and an external sensing resistor. A common on chip oscillator supplies pulses at the chopper rate to both choppers.

In each chopper (figure 14) the flip flop is set by each pulse from the oscillator, enabling the output and allowing the load current to increase. As it increases the voltage across the sensing resistor increases, and when this voltage reaches V_{ref} the flip flop is reset, disabling the output until the next oscillator pulse arrives. The output of this circuit (the flip flop's Q output) is therefore a constant rate PWM signal. Note that V_{ref} determines the peak load current.

Figure 14 : Each Chopper Circuit consists of a Comparator, flip flop and External Sense Resistor. A Common Oscillator Clocks both Circuits.



PHASE CHOPPING AND INHIBIT CHOPPING

The chopper can act on either the phase lines (ABCD) or on the inhibit lines INH1 and INH2. An input named CONTROL decides which. Inhibit chopping is used for unipolar motors but you can choose between phase chopping and inhibit chopping for bipolar motors. The reasons for this choice are best explained with another example.

First let's examine the situation when the phase lines are chopped.

As before, we are driving a two phase bipolar motor and A is high, B low (figure 15). Current therefore flows through Q1, winding, Q4 and R_s . When the voltage across R_s reaches V_{ref} the chopper brings B high to switch off the winding.

The energy stored in the winding is dissipated by current recirculating through Q1 and D3. Current decay through this path is rather slow because the

voltage on the winding is low ($V_{CEsat} Q1 + V_{D3}$) (figure 16).

Why is B pulled high, why push A low? The reason is to avoid the current decaying through R_s . Since the current recirculates in the upper half of the bridge, current only flows in the sensing resistor when the winding is driven. Less power is therefore dissipated in R_s and we can get away with a cheaper resistor.

This explains why phase chopping is not suitable for unipolar motors: when the A winding is driven the chopper acts on the B winding. Clearly, this is no use at all for a variable reluctance motor and would be slow and inefficient for a bifilar wound permanent magnet motor.

The alternative is to tie the CONTROL input to ground so that the chopper acts on INH1 and INH2. Looking at the same example, A is high and B low. Q1 and Q4 are therefore conducting and current flows through Q1, the winding, Q4 and R_s , (figure 17).

Figure 15 : Phase Chopping. In this Example the Current X is interrupted by activating B, giving the Recirculation path Y. The Alternative, de-activating A, would give the Recirculation path Z, increasing Dissipation in R_s .

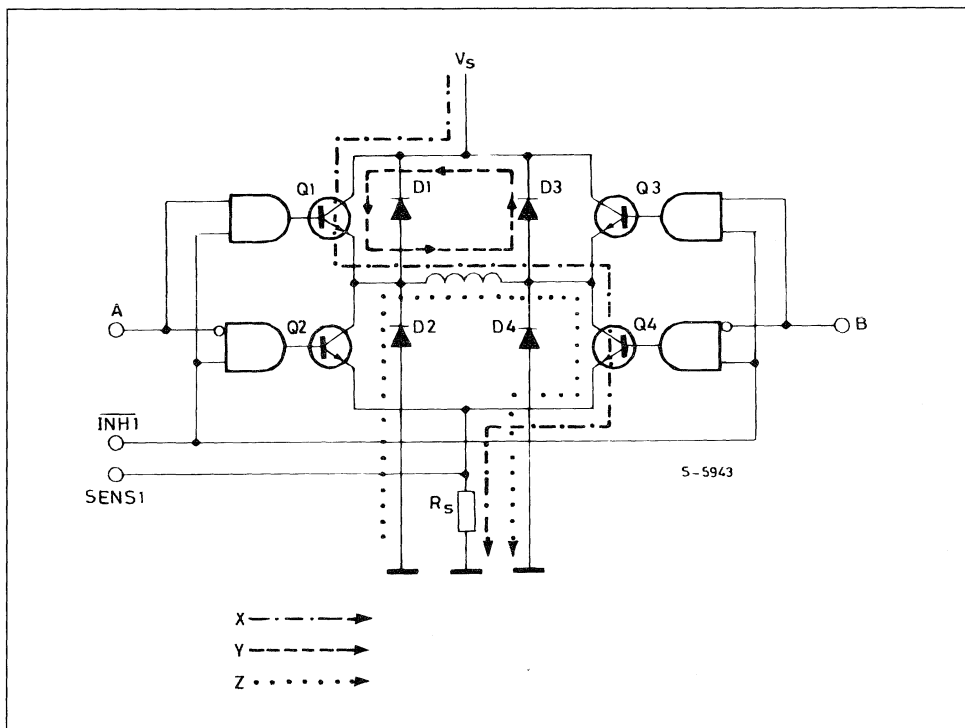


Figure 16 : Phase Chopping Waveforms. The Example shows AB winding energized with A positive with respect to B. Control is high.

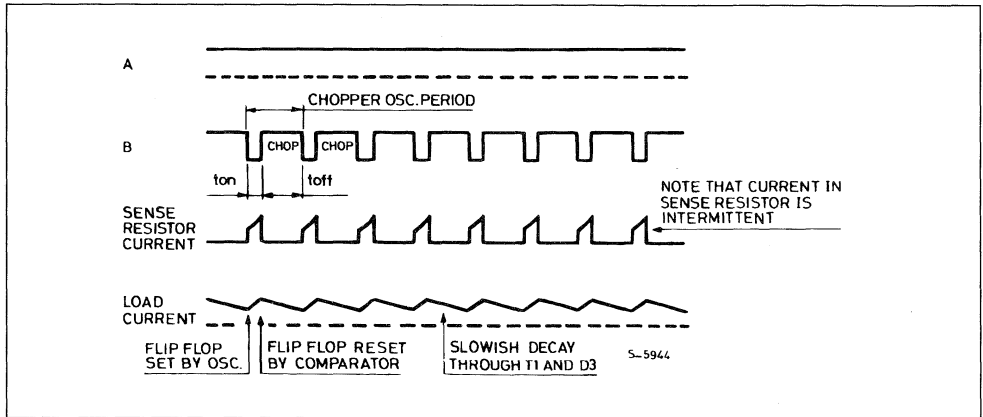
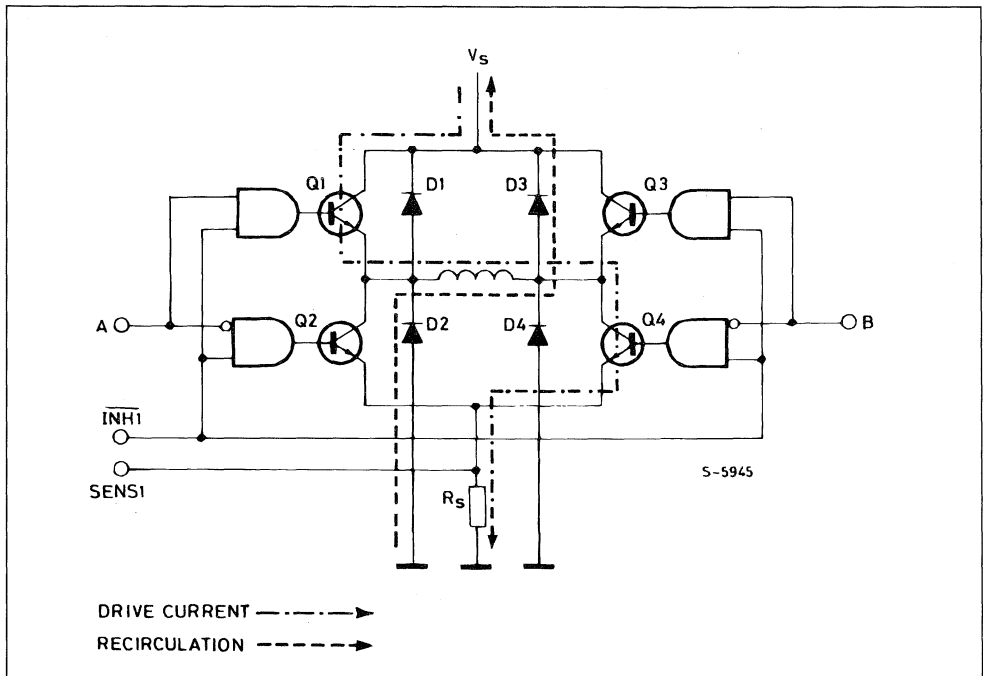


Figure 17 : Inhibit Chopping. The Drive Current (Q1, winding, Q4) in this Case is interrupted by activating INH1. The Decay Path through D2 and D3 is faster than the Path Y of Figure 15.



In this case when the voltage across R_S reaches V_{REF} the chopper flip flop is reset and $INH1$ activated (brought low). $INH1$, remember, turns off all four transistors therefore the current recirculates from ground, through D2, the winding and D3 to V_S . Discharged across the supply, which can be up to 46V, the current decays very rapidly (figure 18).

The usefulness of this second faster decay option is fairly obvious ; it allows fast operation with bipolar motors and it is the only choice for unipolar motors. But why do we offer the slower alternative, phase chopping ?

The answer is that we might be obliged to use a low chopper rate with a motor that does not store much energy in the windings. If the decay is very fast the average motor current may be too low to give an useful torque. Low chopper rates may, for example, be imposed if there is a larger motor in the same system. To avoid switching noise on the ground plane all drivers should be synchronized and the chopper rate is therefore determined by the largest motor in the system.

Multiple L297s are synchronized easily using the SYNC pin. This pin is the squarewave output of the on-chip oscillator and the clock input for the choppers. The first L297 is fitted with the oscillator components and outputs a squarewave signal on this pin (figure 19). Subsequent L297s do not need the oscillator components and use SYNC as a clock input. An external clock may also be injected at this terminal if an L297 must be synchronized to other system components.

Figure 18 : Inhibit Chopper Waveforms. Winding AB is energized and CONTROL is low.

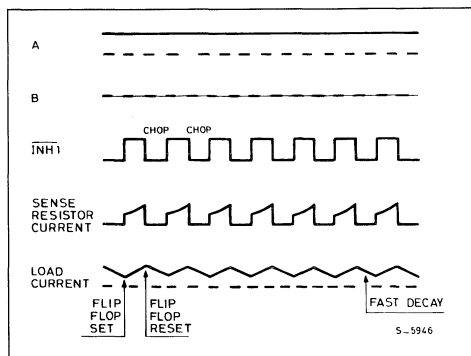
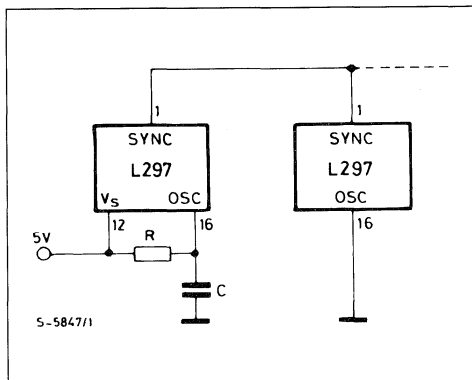


Figure 19 : The Chopper Oscillator of Multiple L297s are synchronized by connecting the SYNC Inputs together.



THE L297A

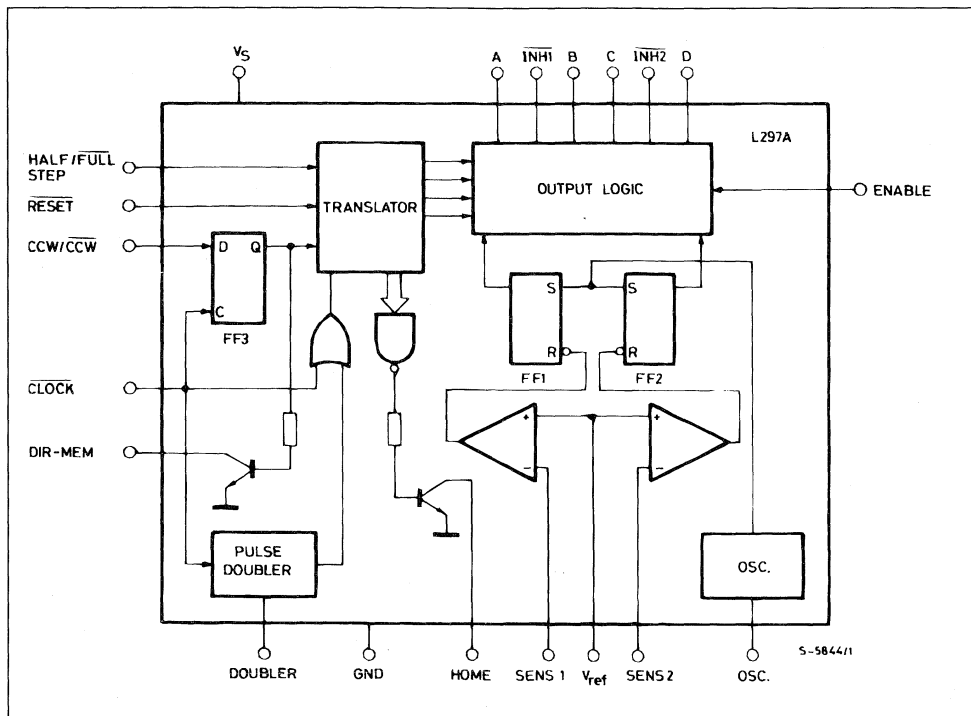
The L297A is a special version of the L297 developed originally for head positioning in floppy disk drives. It can, however, be used in other applications.

Compared to the standard L297 the difference are the addition of a pulse doubler on the step clock input and the availability of the output of the direction flip flop (block diagram, figure 20). To add these functions while keeping the low-cost 20-pin package the CONTROL and SYNC pins are not available on this version (they are not needed anyway). The chopper acts on the ABCD phase lines.

The pulse doubler generates a ghost pulse internally for each input clock pulse. Consequently the translator moves two steps for each input pulse. An external RC network sets the delay time between the input pulse and ghost pulse and should be chosen so that the ghost pulses fall roughly halfway between input pulses, allowing time for the motor to step.

This feature is used to improve positioning accuracy. Since the angular position error of a stepper motor is noncumulative (it cancels out to zero every four steps in a four step sequence motor) accuracy is improved by stepping two of four steps at a time.

Figure 20 : The L297A, includes a Clock Pulse Doubler and provides an Output from the Direction flip flop (DIR – MEM).



APPLICATION HINTS

Bipolar motors can be driven with an L297, an L298N or L293E bridge driver and very few external components (figure 21). Together these two chips form a complete microprocessor-to-stepper motor interface. With an L298N this configuration drives motors with winding currents up to 2.5A ; for motors up to 1A per winding and L293E is used. If the PWM choppers are not required an L293 could also be used (it doesn't have the external emitter connections for sensing resistors) but the L297 is underutilized. If very high powers are required the bridge driver is replaced by an equivalent circuit made with discrete transistors. For currents to 3.5A two L298N's with paralleled outputs may be used.

For unipolar motors the best choice is a quad darlington array. The L702 can be used if the choppers are not required but an L7150 or L7180 is preferred. These quad darlington have external emitter connections which are connected to sensing resistors

(figure 22). Since the chopper acts on the inhibit lines, four AND gates must be added in this application.

Also shown in the schematic is a zener diode in series with the suppression diodes. This serves to increase the voltage across which energy stored in the winding is discharged and therefore speed the current decay.

In all applications where the choppers are not used it is important to remember that the sense inputs must be grounded and V_{REF} connected either to V_S or any potential between V_S and ground.

The chopper oscillator frequency is determined by the RC network on pin 16. The frequency is roughly $1/0.7 RC$ and R must be more than 10 k Ω . When the L297A's pulse doubler is used, the delay time is determined by the network $R_d C_d$ and is approximately $0.75 R_d C_d$. R_d should be in the range 3 k Ω – 100 k Ω (figure 23).

Figure 21 : This Typical Application shows an L297 and L298N driving a Bipolar Stepper Motor with Phase currents up to 2A.

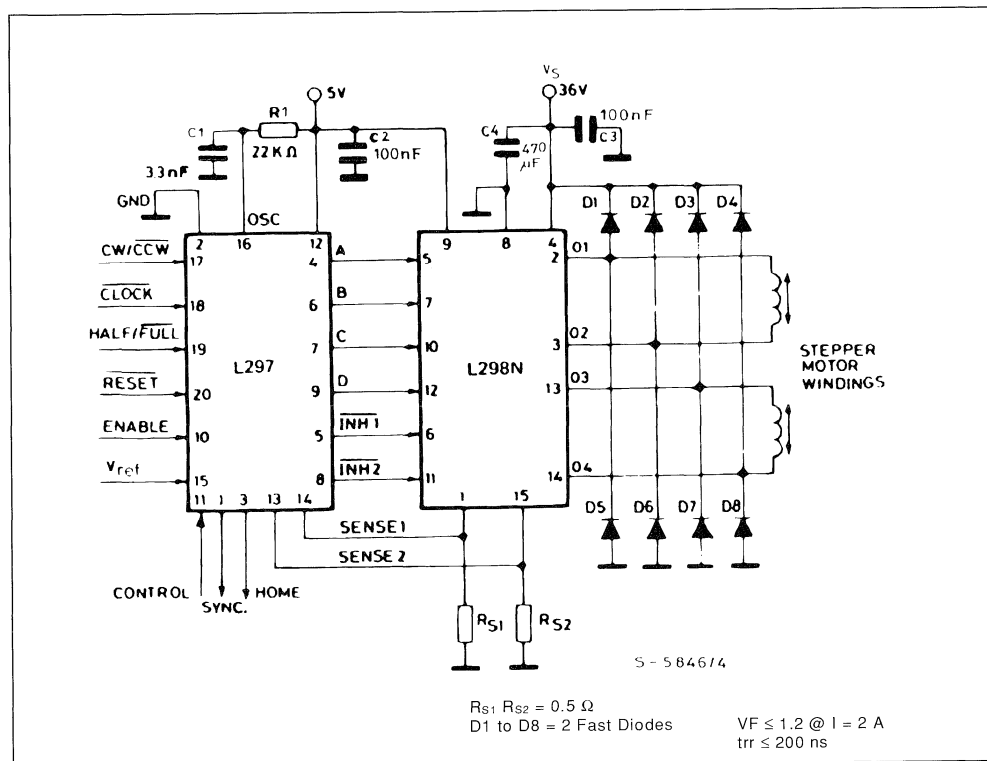


Figure 22 : For Unipolar Motors a Quad Darlington Array is coupled to the L297. Inhibit Chopping is used so the four AND Gates must be added.

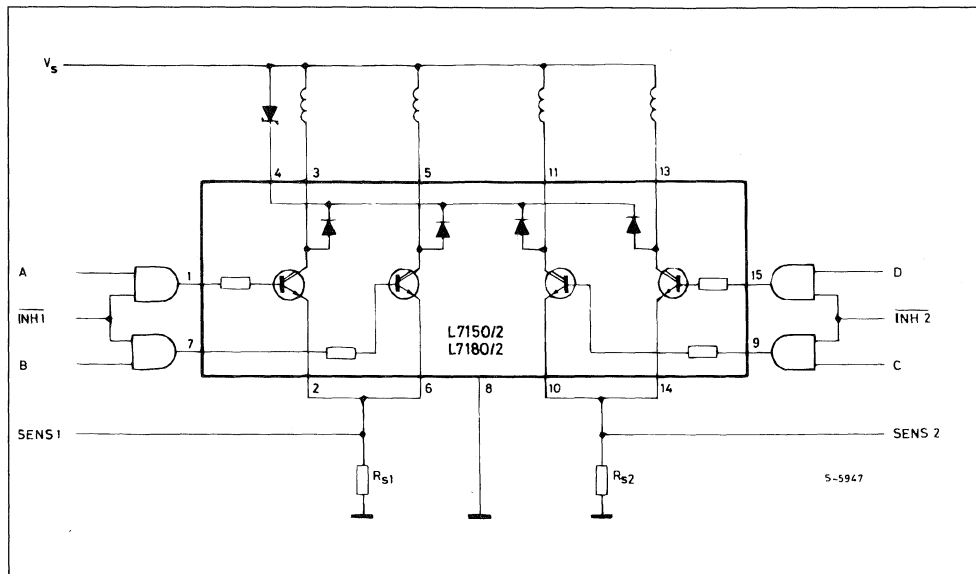
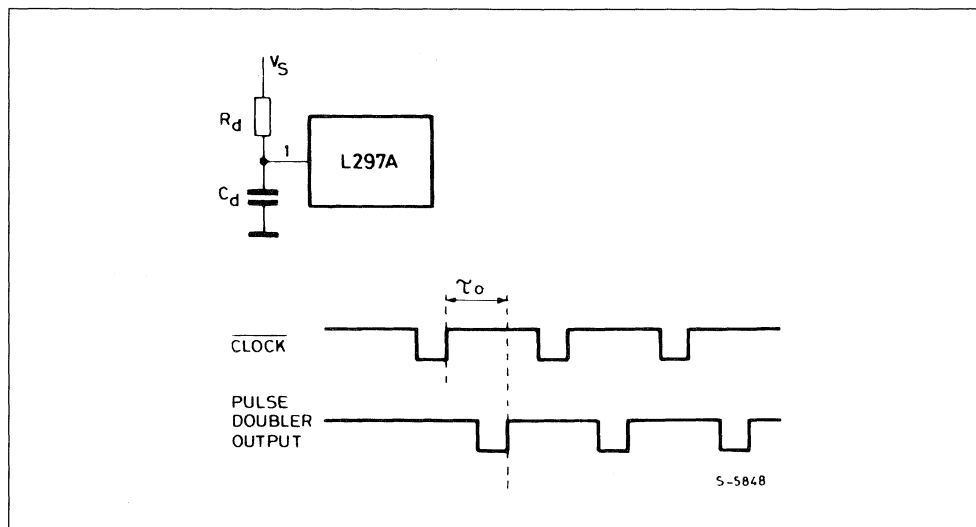


Figure 23 : The Clock Pulse Doubler inserts a Ghost Pulse τ_o seconds after the Input Clock Pulse. $R_d C_d$ is chosen to give a Delay of approximately Half the Input Clock Period.



PIN FUNCTIONS – L297

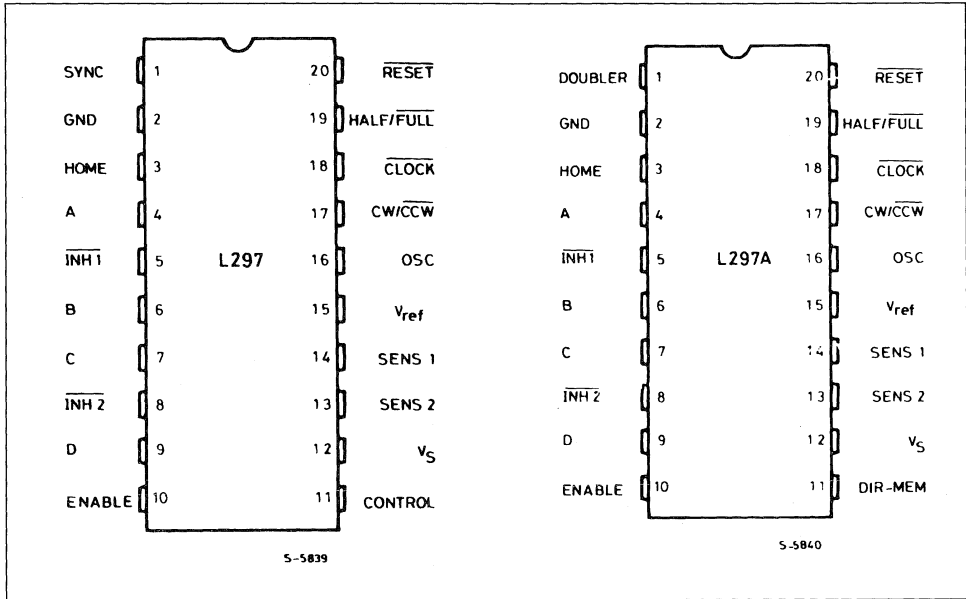
N°	Name	Function
1	SYNC	Output of the On-chip Chopper Oscillator. The SYNC connections of all L297s to be synchronized are connected together and the oscillator components are omitted on all but one. If an external clock source is used it is injected at this terminal.
2	GND	Ground Connection.
3	HOME	Open collector output that indicates when the L297 is in its initial state (ABCD = 0101). The transistor is open when this signal is active.
4	A	Motor phase A drive signal for power stage.
5	INH1	Active low inhibit control for driver stages of A and B phases. When a bipolar bridge is used this signal can be used to ensure fast decay of load current when a winding is de-energized. Also used by chopper to regulate loadcurrent if CONTROL input is low.
6	B	Motor phase B drive signal for power stage.
7	C	Motor phase C drive signal for power stage.
8	INH2	Active low inhibit control for drive stages of C and D phases. Same functions as INH1.
9	D	Motor phase D drive signal for power stage.
10	ENABLE	Chip enable input. When low (inactive) INH1, INH2, A, B, C and D are brought low.
11	CONTROL	Control input that defines action of chopper. When low chopper acts on INH1 and INH2 ; when high chopper acts on phase lines ABCD.
12	V _s	5 V Supply Input.
13	SENS ₂	Input for load current sense voltage from power stages of phases C and D.
14	SENS ₁	Input for load current sense voltage from power stages of phases A and B.
15	V _{ref}	Reference voltage for chopper circuit. A voltage applied to this pin determines the peak load current.
16	OSC	An RC network (R to V _{CC} , C to ground) connected to this terminal determines the chopper rate. This terminal is connected to ground on all but one device in synchronized multi - L297 configurations. $f \cong 1/0.69 RC$, $R > 10 k\Omega$.
17	CW/CCW	Clockwise/counter clockwise direction control input. Physical direction of motor rotation also depends on connection of windings. Synchronized internally therefore direction can be changed at any time.
18	CLOCK	Step Clock. An active low pulse on this input advances the motor one increment. The step occurs on the rising edge of this signal.
19	HALF/FULL	Half/full Step Select Input. When high selects half step operation ; when low selects full step operation. One-phase-on full step mode is obtained by selecting FULL when the L297's translator is at an even-numbered state. Two-phase-on full step mode is set by selecting FULL when the translator is at an odd numbered position. (the home position is designated state 1).
20	RESET	Reset Input. An active low pulse on this input restores the translator to the home position (state 1, ABCD = 0101).

PIN FUNCTIONS – L297A

Pin function of the L297A are identical to those of the L297 except for pins 1 and 11.

N°	Name	Functions
1	DOUBLER	An RC network connected to this pin determines the delay between an input clock pulse and the corresponding ghost pulse.
11	DIR-MEM	Direction Memory. Inverted output of the direction flip-flop. Open collector output.

Figure 24 : Connection Diagrams.



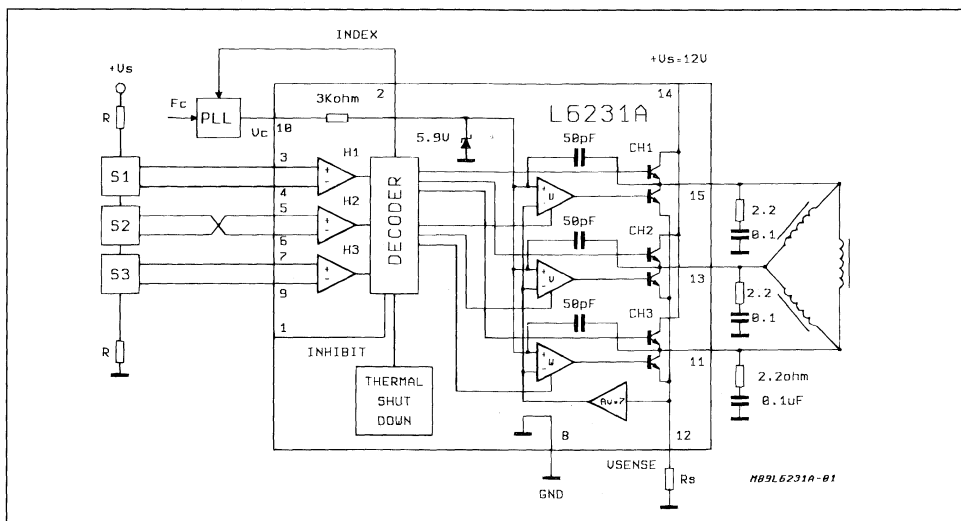
DC-AC AND BRUSHLESS MOTORS

by Antonio Massimini

In addition to operating in a linear mode, the rise and fall times of the output stages are controlled to limit EMI. The control of the power stages eliminates the possibility of simultaneous conduction of the upper and lower drivers of the same output channel. A speed control input linearly controls the base current of the lower drivers to limit the motor current. Integrated fly-back diodes recirculate energy back to the power supply if there is a discontinuity in the phase switching. It also includes thermal shutdown with hysteresis.

In a similar device, L6230A, the enable pin, FWD/TRI-STATE is replaced by a directional control input, FWD//REV. All other features are the same between these two devices.

Figure 1 : L6231A Block Diagram.



CURRENT MODE OPERATION

The L6131A power stage employs current-mode operation with transconductance gain defined by the value of an external sense resistor, R_s . As seen in *figure 1*, the IC amplifies sense voltage by a factor of 7. This minimizes sense resistor power dissipation.

Figure 2 shows the timing relationships of the device. While the upper drivers of the totem pole outputs are in saturation, when turned on, the lower drivers are linearly controlled. The speed control voltage, V_c , controls the base current of the lower driver, thus controlling motor speed. The relationship between output current I_o and V_c is :

$$I_o = \frac{(V_c - 1)}{7R_s} \quad (1)$$

Note that a 1.0V dead zone improves noise immunity to ground plane voltage spikes. This is also shown in *(figure 3)*.

V_c is internally clamped to 5.9V by a zener. If

$V_x = 5.9V$ is the full-scale value for the control voltage, the maximum output current is related to V_x

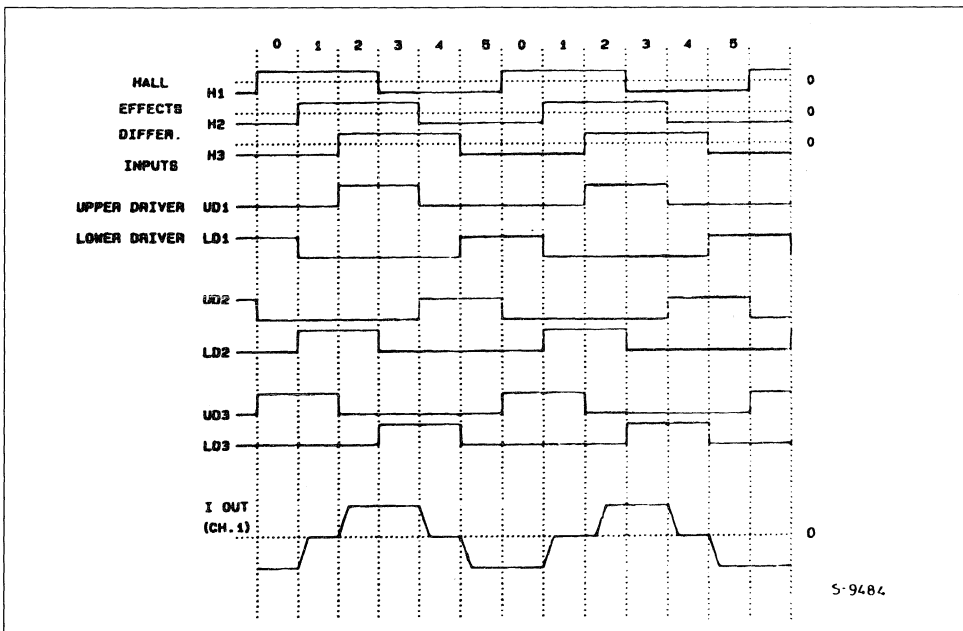
by :

$$R_s = \frac{(V_x - 1)}{7I_{max}} \quad (2)$$

In a closed-loop system, any type of speed control such as V-to-F or PLL, may be used by providing an analog signal compatible with the above equations. For these applications, the device provides a signal proportional to the motor speed. This open collector output is the buffered signal at the Hall Effect sensor input, H1.

While motor speed control can also be achieved in a closed-loop system by toggling the enable input (FWD/TRI-STATE) to maintain speed, this is not advisable. First, it defeats the purpose of a linear controller, i.e. to reduce EMI. Secondly, continuous toggling of the TRI-STATE function causes recirculation currents to flow constantly through the internal diodes. Occasional tri-stating for such purposes as head parking, etc. is not a problem. However, for speed control, the device exhibits increased heat dissipation and stress due to the pulsing recirculation current.

Figure 2 : L6231A Timing Diagram.



COMMUTATION SEQUENCE

The windings of a three-phase brushless DC motor must be energized in a specific sequence for proper operation. Therefore, the proper sequence of signals from the Hall Effect sensors must occur. The specific sequence for the forward mode (state A-F) is shown in figure 3. Table 1 shows the Hall Effect code and corresponding coil energization. The convention shown is plus for upper driver ON (source) and minus for lower driver ON (sink).

Table 1 : Coil Energization.

STATE	H1	H2	H3	R	S	T
A	1	0	0	+		-
B	1	1	0		+	-
C	1	1	1	-	+	
D	0	1	1	-		+
E	0	0	1		-	+
F	0	0	0	+	-	

Figure 3 : Output Current vs. Control Voltage.

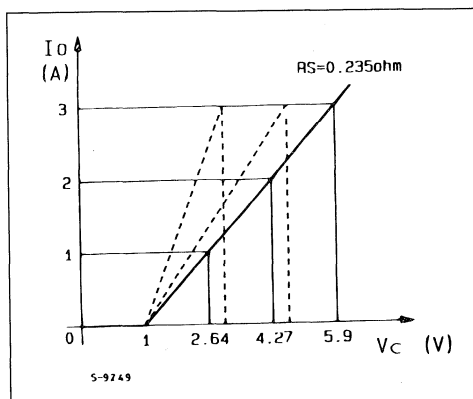
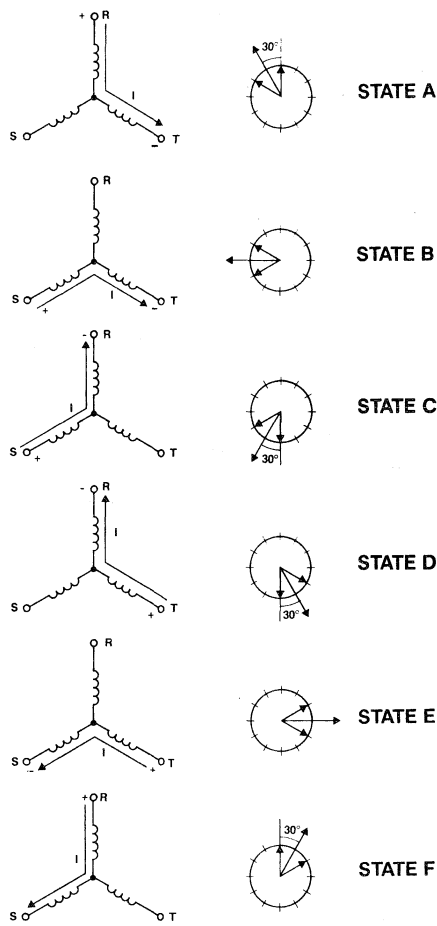


Figure 4 illustrates conceptually how a rotating magnetic vector results from energizing a simple model of a WYE connected motor. A similar analysis may be done for a DELTA connected motor. The convention for this model is that for a positively energized coil, current flows in and produces a magnetic flux flowing out. The converse is true for a negatively charged coil. The stator vector is the resultant of the two flux vectors.

It should be noted that only two output stages operate during any state. When switching from one state

to the next, the driver turning ON is *not* in the same stage as the one turning OFF, or the one not switching. With this type of sequence there is no possibility for shoot-through current. Also note that if the device is not driven directly from the motor's Hall Effect sensors but a derived set of signals (e.g. interfacing logic, Look Up Table, etc.), these signals must conform to the table. Jumping around in the state sequence can cause serious problems. For example, if state D is skipped, then going from state C to E can result in shoot-through current.

Figure 4 : Commutation Sequence.



SLEW RATE CONTROL

One method of EMI reduction is wave shaping. Taking into account that $V = L di/dt$, potential noise voltage can be significant. By controlling the turn-on and turn-off rates this factor can be reduced. An important feature is the controlled di/dt , which is achieved with integrated capacitors in the output stages. The typical dV/dt value is $0.1V/\mu\text{sec}$.

Besides slowing down the rise time of the output voltage to reduce the effects of high-frequency components, the controlled slew rate improves the torque profile. If the turn-on and turn-off times were not controlled and thus closely matched, there would be too much variability. For example, with a controlled slew rate as one lower driver turns ON and another turns OFF (with the third stage not switching) as in states B-C, there is a smooth transition of current flow from S-to-T to S-to-R. The current in coil T dies down at the same rate that current increases in coil R. The resultant stator vector rotates smoothly with a periodic ripple.

If there is a very slow turn-on and very fast turn-off, the current in coil T has to recirculate through the internal diodes to the power supply and coil R would not be conducting yet. Thus, there would be a momentary freewheeling condition and a dip in torque before current could flow through the windings once more. If there is a very fast turn-on and very slow turn-off, then there would be current flow in both coils T and R. The resultant stator vector is momentarily greater than it should be. Spikes and/or dips would be superimposed on the current profile and thus torque as well. A similar analysis can be done for the upper drivers.

One drawback to a controlled slew rate is that it is a limiting factor in applications that require toggling the directional input, such as head positioning. For $V_s = 10V$, the time for changing state in one stage, i.e. sink to tri-state or tri-state to source, is typically :

$$t = (V_s/2)/(0.1V/\mu\text{sec}) = 50\mu\text{sec} \quad (3)$$

Freq = 20kHz

Due to process variability, this frequency could be lower.

The L6231A design assumes that the positioning of the Hall Effect sensors in a three-phase brushless motor is physically at 30° intervals. You can imagine two "windows" on the rotor each of which is 90° wide and 180° apart (figure 5). The timing diagram in mechanical angles is shown in figure 6.

These waveforms must appear at the Hall Effect inputs. As a window passes over the sensor, the output goes high. The rotation shown in figure 5 must be counter-clockwise for forward rotation of the

motor as it is defined for the motor. This is a stylized concept for determining the Hall Effect code and does not reflect the actual direction of rotation of the motor in a physical sense. In an eight-pole (four pole pairs) motor, 360 electrical degrees corresponds to 180 mechanical degrees.

If a motor is selected whose sensor outputs do not match those required by the L6231A a signal set conversion is necessary. Developing a diagram similar to that of figure 5 is helpful for visualizing this.

Figure 5 : Hall Sensor positioning.

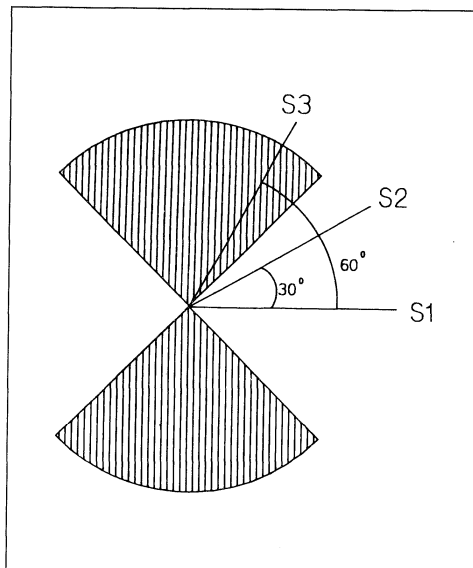
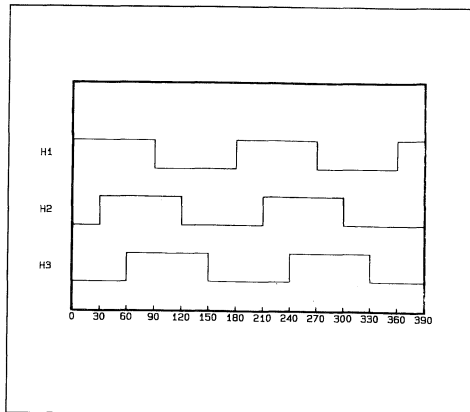
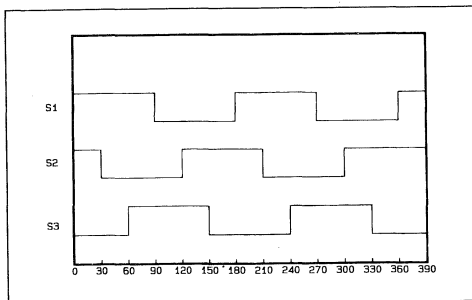


Figure 6 : Mechanical Angle of Rotation.



Given the timing diagram of *figure 7*, and assuming 90° windows 180° apart, the result is *figure 8*. In this case the sensors are 60° apart with their windows rotating clockwise for a corresponding forward rotation of the motor.

Figure 7 : Alternate Mechanical Angle of Rotation.



S3 is the first sensor encountered by the window in *figure 8*. This should be used for Hall Effect input H1. After 30° rotation CW, the H2 input must go high. The inverse of S1 would satisfy this. After another 30° of rotation, input H3 must go high. At this point the window encounters S2. Therefore, S2 should be connected to H3. The conversion for this motor is shown in *table 2*.

Figure 8 : Alternate Hall Sensor Positioning.

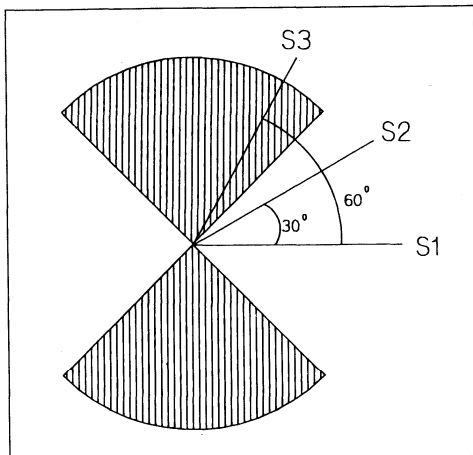


Table 2 : Alternate Coil Energization.

Motor Sensor	L6231A Inputs
S3	H1
S1 Inverse	H2
S2	H3

Inverting the above S1 signal is easy enough with the device's differential comparator inputs. Differential signals may be reversed to affect a signal inversion. For TTL-level signals the positive input is set to a reference point and the signal is connected to the negative input.

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DRIVING DC MOTORS

By G. MAIOCCHI and M. BUSSOLERA

INTRODUCTION

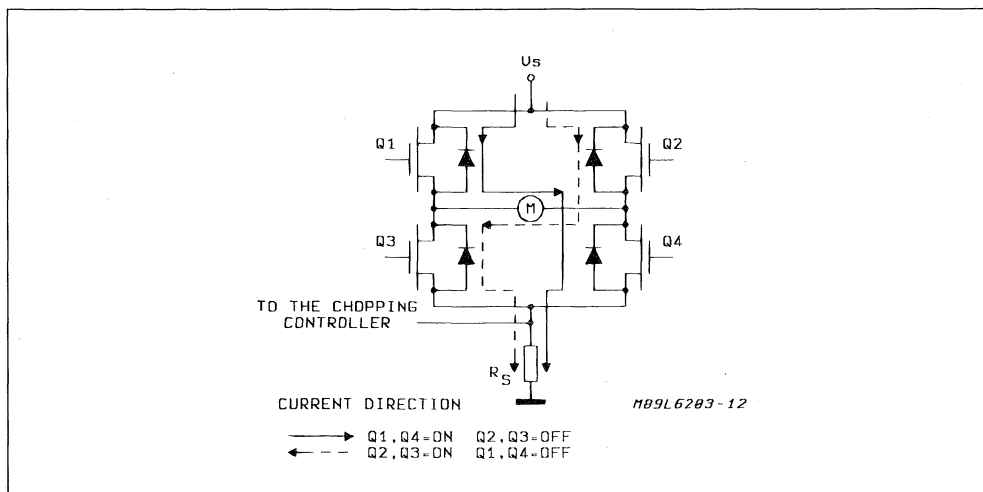
Driving DC motors with integrated circuits seems at first to be rather simple. Yet by analyzing the actual application it is possible to see if there exist conditions causing stresses to the IC during operation which in the end can cause failure. With proper de-

sign and analysis in critical applications it is possible to avoid conditions which lead to IC damage.

GENERAL CONSIDERATIONS

Figure 1 illustrates driving a DC motor using a power MOS bridge.

Figure 1.

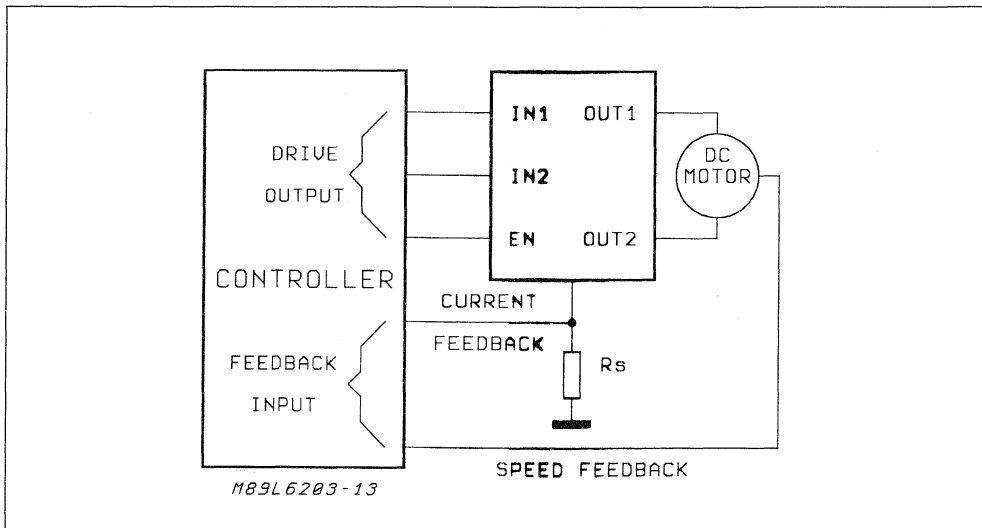


By driving the four MOS in the correct sequence the direction of current flow through the motor is reversed, consequently reversing the direction of the motor's rotation. The motor torque is a function of the current amplitude, the motor's internal parameters, and the external load. The resistive torque is dependent on the motor's internal friction. The current level can be controlled with current chopping. The controller checks the current level by monitoring the sense resistor voltage and then drives the appropriate power MOS. On the other

hand this means that when current does not flow in the sense resistor (which we will examine during recirculation) it is not possible to measure the current level and thus limit it.

Figure 2 shows a more general application circuit which includes an external control loop. Data relating to the actual motor speed is transmitted to the controller by the system which stabilizes the current in the bridge as a function of the requested rotation velocity. In this case also the current is limited through chopping.

Figure 2.



Electrically a DC motor can be viewed as a series RL network with a voltage generator $V(\omega)$. The generator represents the back electromotive force (BEMF) generated by the motor's rotation and which opposes the electromotive force of the supply.

The value of the BEMF is a function of the motor's angular velocity. If the motor has no external load and its velocity is not limited, it will accelerate up to the velocity w such that $V(w)$ equals the supply voltage V_s . In this situation the two EMF's cancel each other and thus the motor torque responsible for acceleration will go away. In reality $V(\omega)$ is always slightly less than V_s in which case a small motor torque is necessary to compensate resistive torque due to internal friction.

Thus it can be seen that the motor's BEMF can reach elevated values which in some cases can cre-

ate application problems due to a certain type of stress.

RECIRCULATION CURRENT

Part of the energy delivered to the circuit by the supply is stored in the motor's inductance. When an inductive load is driven, during chopping and during inversion of the diagonal of the bridge, there is always some recirculation current which allows this energy to discharge.

The following figures show the resulting current paths based on the type of chopping method used. In the first two cases, "two-phase" and "enable" chopping, the current decays quickly and, is thus, fast recirculation. When "one-phase" chopping is implemented the current requires a longer time period to decay and, is thus, slow recirculation.

Figure 3a : Two Phase Chopping.

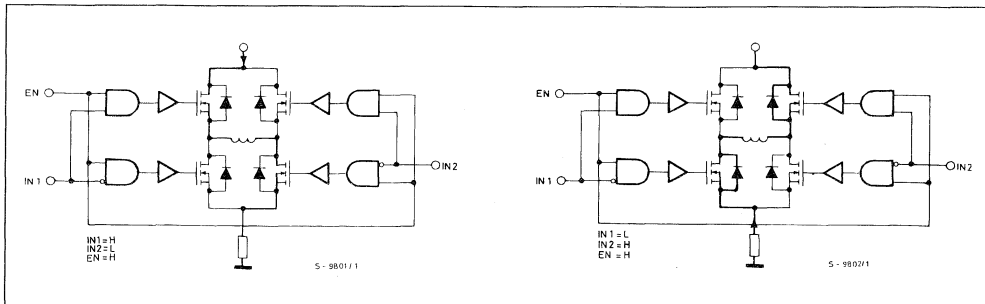


Figure 3b : Enable Chopping.

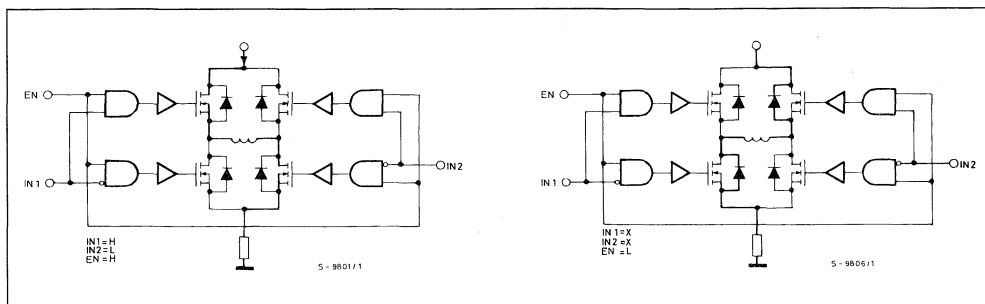
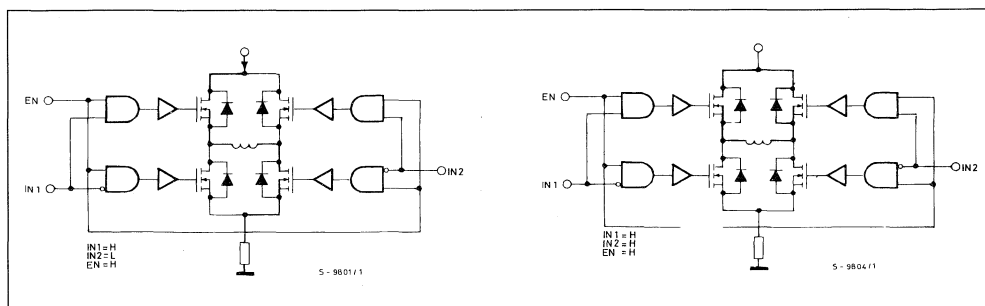


Figure 3c : One Phase Chopping.



DYNAMIC BEHAVIOUR

The driving of a DC motor will be analyzed dynamically during different motion phases. Fundamental to the working conditions of the IC is the type of load which the motor is driving. In fact if the load is frictional, the deceleration phase is not particularly serious for the IC since the load itself is supplying a braking torque. However, when the load is inertial it will appear to the IC to be a motor torque generator.

This could take the IC into critical operating conditions which can incur failure.

- Acceleration Phase : The current rises, delivering a torque which allows the motor to accelerate, up to the maximum velocity or till it is stabilized by the control loop. The type of load essentially determines the required current.

-Constant Velocity : In this case the required velocity is less than the maximum. The current is limited by chopping. This can be done by turning ON and

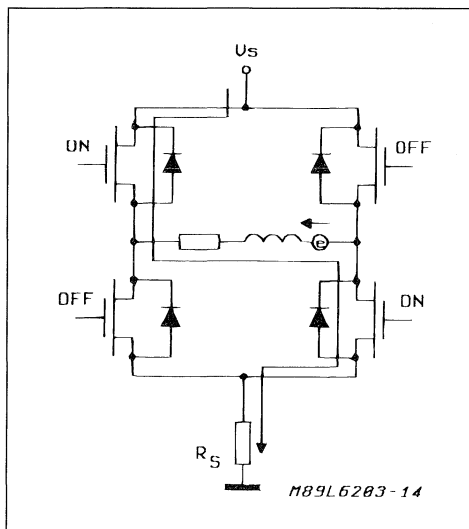
OFF a MOS of the diagonal which is in conduction.

- Deceleration : When a DC motor must be decelerated, the type of load being driven becomes important. As previously stated, in the case of a frictional load, the load is essentially braking the motor. Thus, in general, it could be sufficient to cancel the motor torque by opening the bridge (i.e. disable the driver). In the case of an inertial load, however, the braking torque is provided by the driver. It is this situation that is of most concern. Since every change of direction involves a braking phase, a detailed analysis of this situation will be done.

ROTATION INVERSION

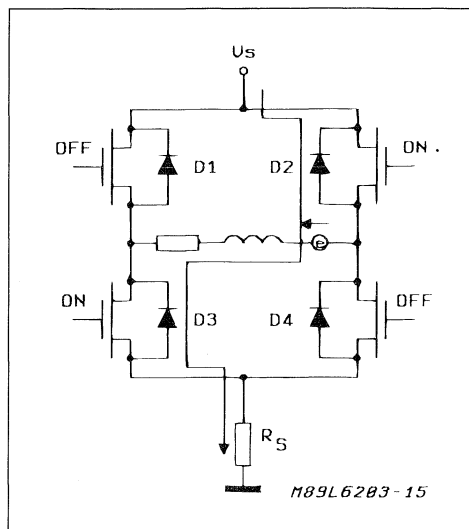
Initially the current flows in one direction as shown in figure 4. Figure 5 illustrates the situation when the diagonal is switched. The motor's inductance discharges the stored energy by fast recirculation through diodes D2 and D3.

Figure 4.



The inertial load of the motor, which can be viewed as a flywheel, has stored energy during the phase prior to inverting the diagonal. This energy is returned to the motor providing a motor torque which keeps the motor rotating. Greater still is the flywheel's moment of inertia, greater than the motor torque that it provides to the motor. The discharge time is longer because the flywheel must discharge its energy. Also associated with the motor's rotation is the BEMF. Thus, in order to stop the motor a brak-

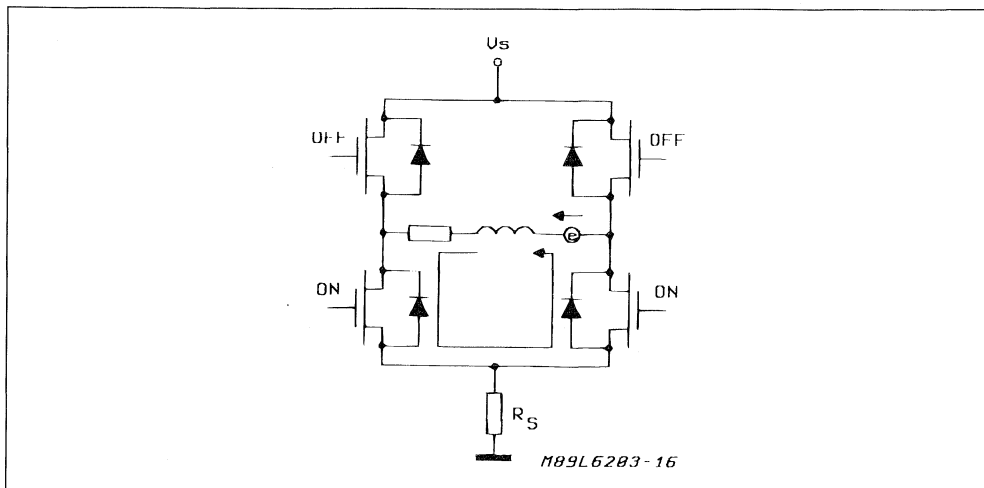
Figure 5.



ing torque must be applied. This is generated when, following completion of slow recirculation, the current begins to flow in the opposite direction from the previous state.

It is precisely at this point which effectively the braking phase begins. When the sense voltage rises to the preset level chopping is triggered. In figure 6 chopping results in slow recirculation (in practice the motor is short-circuited).

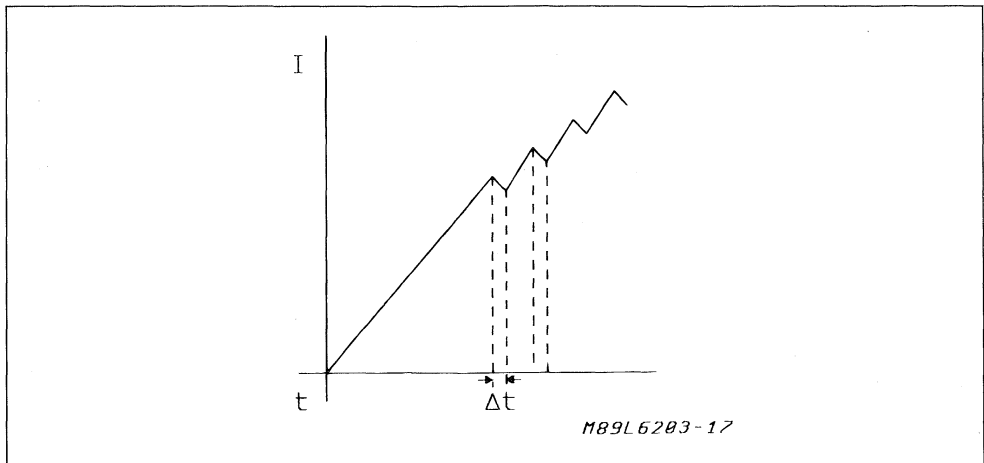
Figure 6.



As it can be seen, the BEMF is dropped across the relatively low resistances of the motor, the diode in line and the MOS that is ON. The sense resistor does not enter into this. If the motor's rotational velocity remains high the recirculation current could be very large, enough to damage the IC. Actually the current does not rise instantaneously to the steady state value of : $I = V(\omega)/(R_m + R_d + R_{dson})$. Rather, the current follows the graph shown in figure 7. In fact, when chopping begins the sense current goes to zero, thus turning MOS M2 ON again. The motor current flows through the sense resistor, re-enabling the

chopping. The cycle repeats in an iterative manner with a recirculation current that continues to rise. Due to the inertial load and the BEMF it generates and the recirculation current as described above, the current in the sense resistor will be greater than the desired value set by $I_m = V_{ref}/R_{sense}$. When the current reaches the maximum level (see previous paragraph) the current will fall to the preset level controlled by the chopping, the inertial load having discharged its energy from the previous phase. This elevated current level is temporary, but can be damaging to the IC.

Figure 7.



[caption for figure 7]

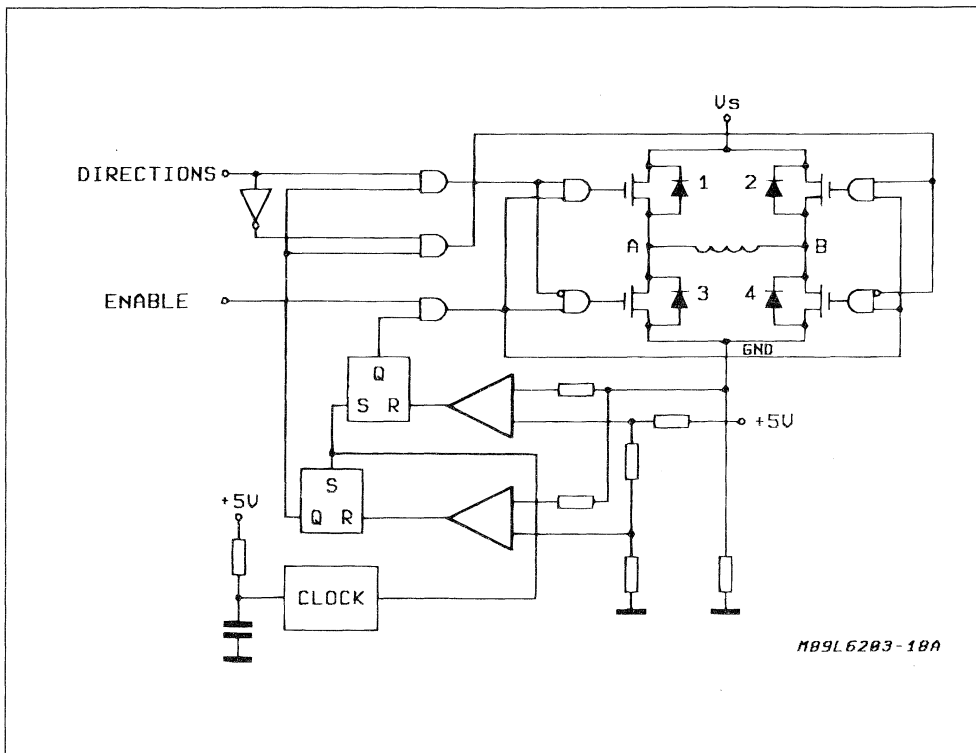
I = recirculation current

delta t = time interval during which current flows through R_{sense} .

Braking the motor by short-circuiting it involves an accurate study of the mechanical system during the design phase. Knowing the value of the BEMF generated by the motor during braking, the motor resistance, and the equivalent resistance of the

MOS and diode involved during recirculation it is possible to determine the recirculation current and if it is less than or greater than the maximum value that the IC can tolerate.

Figure 8.



If the recirculation current is too high it will be necessary to brake the motor with an alternative method. Using fast recirculation in combination with slow recirculation it is possible to brake the motor. Even if this is less than an efficient manner it avoids causing damage to the IC due to overcurrent. The basic circuit is shown in figure 8. Figure 9 is the application circuit which the Application Lab of Agrate, experimented with. This circuit uses an L6203 as the power driver. As seen in figure 8, as long as the recirculation current does not reach too high a value slow recirculation is used (one-phase chopping). Above a critical threshold slow recirculation is replaced with fast recirculation achieved by enable chopping. The slow and fast recirculations are triggered by two different reference voltages which determine the two current level thresholds. The higher current level for triggering fast recirculation is set little below the max current level available by the IC.

Figure 10 is the current waveform observed on the oscilloscope during few diagonal inversions. In this figure we can see the general trend of the motor current during three inversions of the rotation. A more detailed view of what really happens to the motor current is showed in fig. 11. Before the rotation inversion the motor is sinking its steady state current (about $\pm 250\text{mA}$ in this application, the sign depending from the current flow direction). At the rotation inversion, first the current rises, as previously described, to the current level defined by I_{ref2} . At this moment ENABLE chopping is activated starting the fast recirculation and the current level is clamped at this reference current level. When the motor has dissipated a sufficient rate of its inertial energy, the current falls down, first to the level defined by I_{ref1} (slow recirculation) for all that interval time that is required to dissipate the remaining inertial energy and then to its steady state working level.

Figure 9.

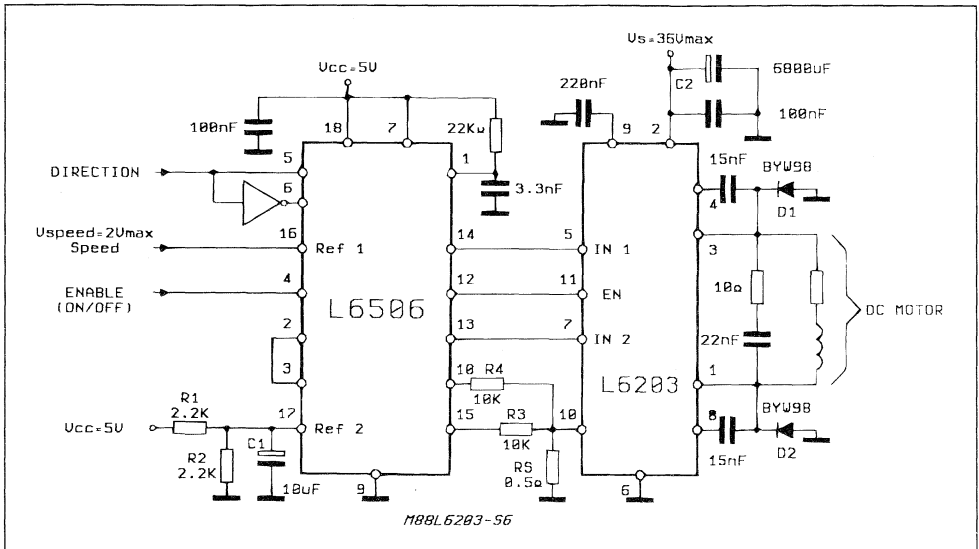
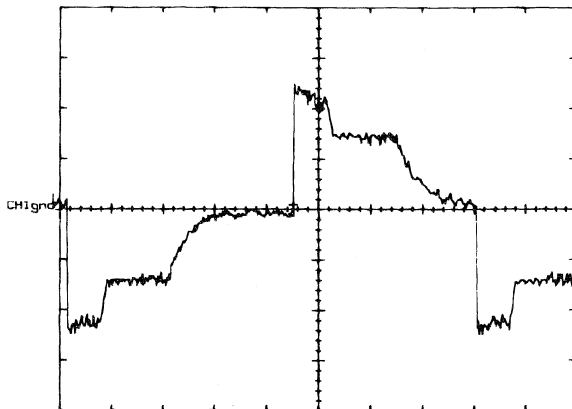


Figure 10.

VERT. 2A/DIV HOR. 100ms/DIV



Three diagonal inversion of a unloaded DC motor

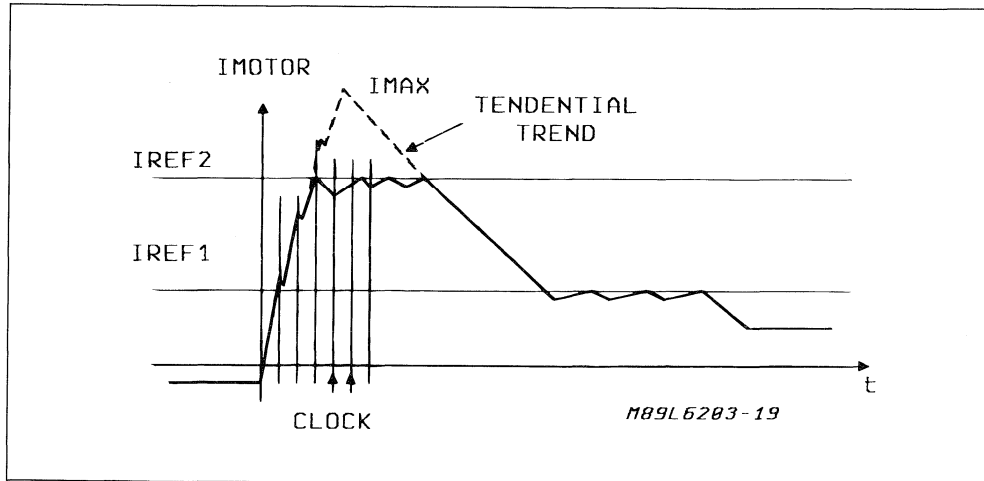
This scheme prevents damage to the IC due to over-current. However, failure due to overvoltage is still possible. An inertial load will return energy to the supply. If the power supply is the type which cannot sink current but can only source current, then the energy from the motor will load the power supply capacitor to a voltage above V_s . If the capacitor value is not large enough, during recirculation the capacitor voltage will rise rapidly. Meanwhile, the lower ac-

tive diode is below ground during recirculation. There is a differential voltage between the overvoltage and the point below ground. If this exceeds the absolute maximum voltage of the IC, damage can occur. Overvoltage can be limited with an appropriate value of power supply capacitor. For the below ground condition of the lower diodes, the sources of the upper MOS can be clamped to ground with schotky diodes.

When V_s is relatively low it may be sufficient to control the differential voltage drop by just limiting the overvoltage with the power supply capacitor and not

having to use the schottky diodes. The feasibility of this solution should nevertheless be verified experimentally in the specific application.

Figure 11.



High power monolithic bridge drivers are an attractive replacement for discrete transistors and half bridges in applications such as DC motor and stepper motor driving. This application guide describes three such devices - the L293, L293E and L298 - and presents practical examples of their application.

Additionally, the L293E and L298 are provided with external connections to the lower emitters of each

Figure 1 shows the internal structure of the L293, L293E and L298. The L293 and L293E are represented as four push pull drivers while the internal schematic is given for the L298. Though they are drawn differently the L293E and L298 are identical in structure ; the L293 differs in that it does not have external emitter connections.

Figure 1 : The L293, L293E and L298 contain four push pull drivers. Each driver is controlled by a logic input and each pair (a bridge) is controlled by an enable input. Additionally, the L293E has external emitter connections for each driver and the L298 has emitter connections for each bridge.

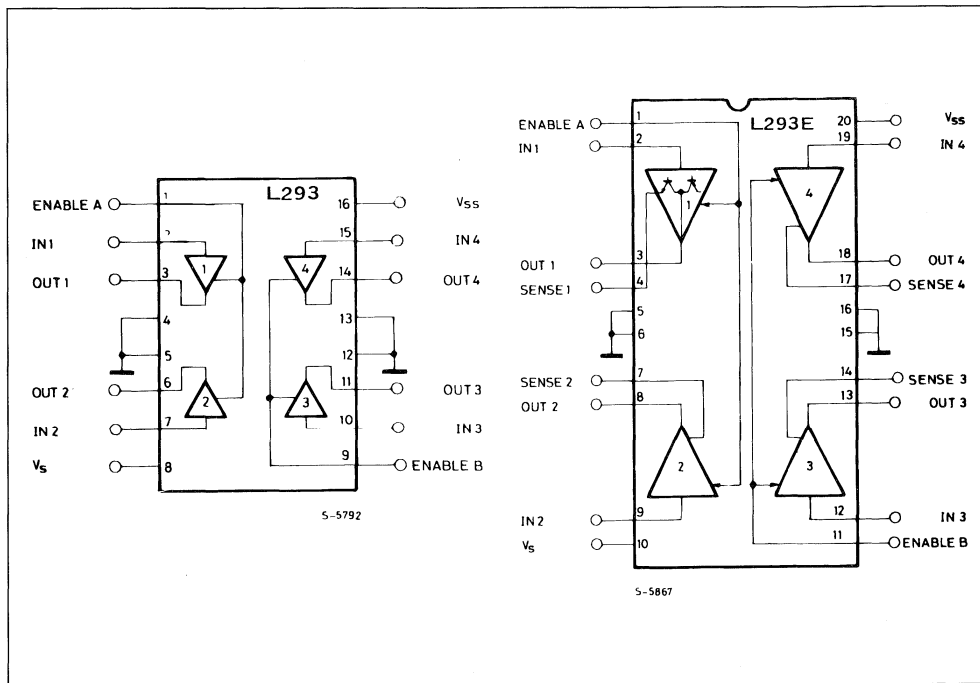
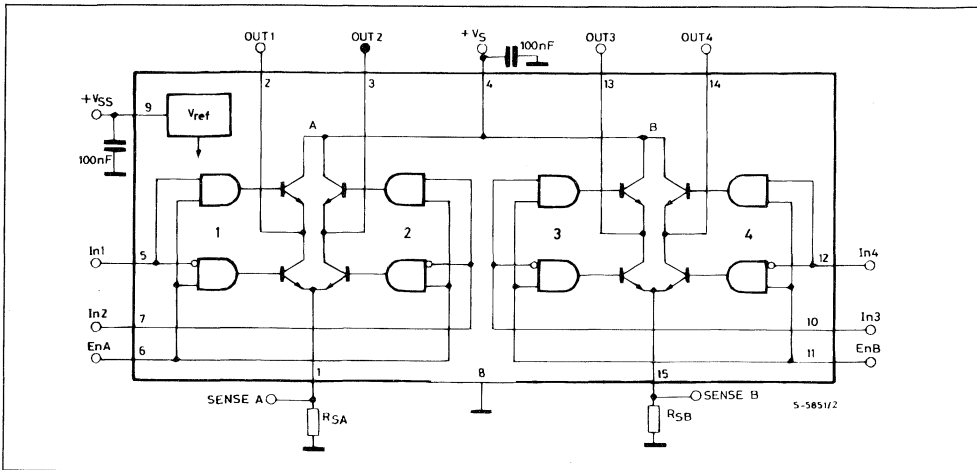


Figure 1 (continued).



The L293 is packaged in a 12 + 4 lead POWERDIP package (a 16-pin DIP with the four center leads used to conduct heat to the PC board copper) and handles 1A per channel (1.5 peak) at voltages up to 36 V.

The L293E, also rated at 1 A/36 V, is mounted in a 16 + 4 lead POWERDIP package. A 15-lead MULTI-WATT plastic power package is used for the L298N which handles up to 2A per channel at voltages to 46 V.

All three devices includes on-chip thermal protection and feature high noise immunity. The high switching speed makes them particularly suitable for switch mode control.

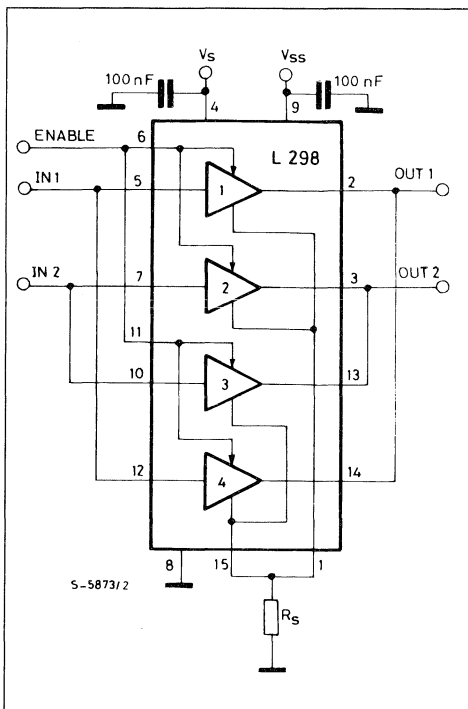
PARALLELING OUTPUTS

Higher output currents can be obtained by paralleling the outputs of both bridges. For example, the outputs of an L298N can be connected in parallel to make a single 3.5 A bridge. To ensure that the current is fairly divided between the bridges they must be connected as shown in figure 2. In other words, channel one should be paralleled with channel four and channel two paralleled with channel three. Apart from this rule the connection is very straightforward - the inputs, enables, outputs and emitters are simply connected together.

The outputs of an L293 or L293E can also be paralleled - in this case too channel 1 must be paralleled with channel 4 and channel 2 with channel 3.

But if two bridges are needed this is not a good idea because an L298N may be used. However, if only

Figure 2 : For higher currents outputs can be paralleled. Take care to parallel channel 1 with channel 4 and channel 2 with channel 3.



one bridge is required an L293 connected as a single bridge may be cheaper than an underutilized L298N.

SHORT CIRCUIT PROTECTION

L293 and L298N drivers can be damaged by short circuits from the output to ground or to the supply. Short circuits to ground are by far the most common and can be protected against by the circuit shown in figure 3.

When the output is short circuited the input is pulled

low after a delay of roughly $10\ \mu\text{s}$, a period determined by the RC time constant. The upper transistor of the output stage is thus turned off, interrupting the short circuit current. When the short is removed the circuit recovers automatically. This is shown by the waveforms of figure 4.

Note that if the short circuit is removed while V1 is high the output stays low because the capacitor C is charged to V_{IH} . The system is reset by the falling edge of V1, which discharges C.

Figure 3 : This circuit protects a driver from output short circuits to ground.

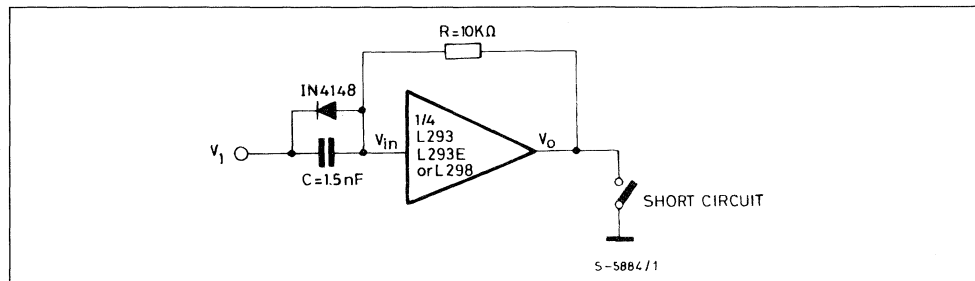
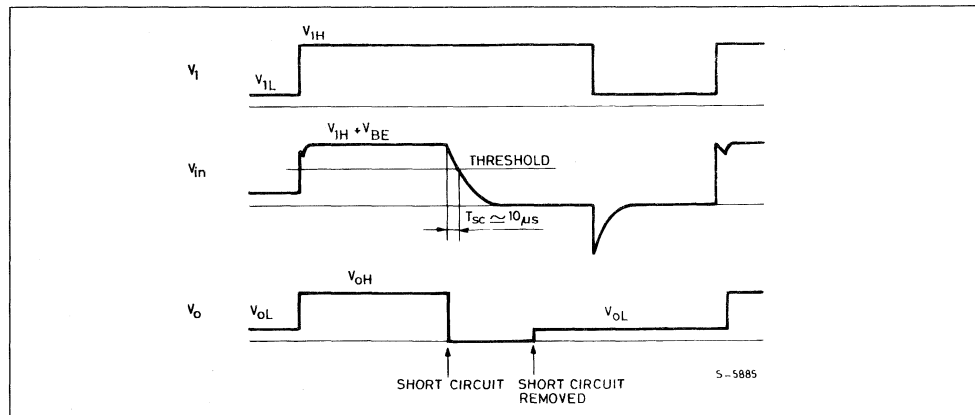


Figure 4 : Waveforms illustrating the short circuit protection provided by the circuit of fig. 3.



DC MOTOR DRIVING

In application where rotation is always in the same sense a single driver (half bridge) can be used to drive a small DC motor. The motor may be connected either to supply or to ground as shown in figure 5.

The only difference between these two alternatives is that the control logic is inverted - a useful fact to

remember when minimising control logic.

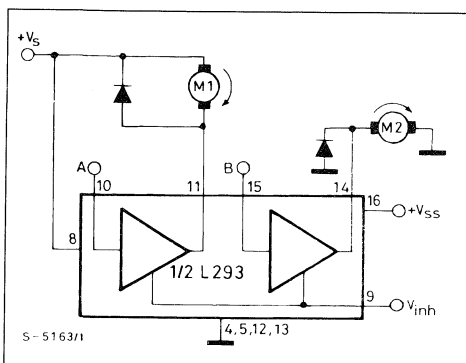
Each device can drive four motors connected in this way. The maximum motor current is 1A for the L293 and 2A for the L298N. However if several motors are driven continuously care should be taken to avoid exceeding the maximum power dissipation of the package.

Each motor in this configuration is controlled by its own logic input which gives two alternatives : run and fast stop (the motor shorted by one of the transistors).

The enable/inhibit inputs also allow a free running motor stop by turning off both transistors of the driver. Since these inputs are common to two channels (one bridge) this feature can only be used when both channels are disabled together.

A full bridge configuration is used to drive DC motors in both directions (figure 6). Using the logic inputs of the two channels the motor can be made to run clockwise, run anticlockwise or stop rapidly.

Figure 5 : For rotation in one direction DC motors are driven by one channel and can be connected to supply or ground.



V_{inh}	A	M1	B	M2
H	H	Fast Motor Stop	H	Run
H	L	Run	L	Fast Motor Stop
L	X	Free Running Motor Stop	X	Free Running Motor Stop

L = Low

H = High

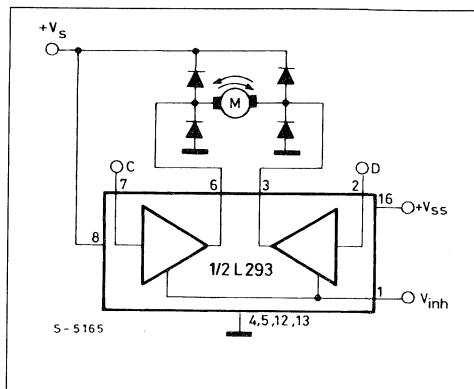
X = Don't Care

Again, the enable/inhibit input is used for a free running stop - it turns off all four transistors of the bridge when low. A very rapid stop may be achieved by reversing the current, though this requires more careful design to stop the motor dead. In practice a tachometer dynamo and closed loop control are usually necessary. Like the previous circuit, this configuration is suitable for motors with currents up to 1A (L293/L293E) or 2A (L298N).

The motor speed in these examples can be controlled by switching the drivers with pulse width modulated squarewaves. This approach is particularly suitable for microcomputer control.

For unidirectional drive with a single channel the

Figure 6 : A bridge is used for bidirectional drive of DC motors.



Inputs	Function
$V_{inh} = H$; C = H ; D = L	Turn Right
C = L ; D = H	Turn Left
C = D	Fast Motor Stop
$V_{inh} = L$; C = X ; D = X	Free Running Motor Stop

L = Low

H = High

X = Don't Care

PWM control signal can be applied to either the channel input or the appropriate enable input. In both cases the recirculation path is through the suppression diode and motor, giving a fairly slow decay. From a practical point of view it is preferable to control the channel input because the circuit response is faster. This is very convenient because each channel has an independent input.

The situation is different for bidirectional motors driven by a bridge. In this case the two alternatives have different effects. If the channel inputs are driven by the PWM signal, with suitable logic, the recirculation path is through a diode, the motor and a transistor (figure 7a), giving a slow decay. On the other hand, if the enable input is controlled the recirculation path is from ground to supply through two diodes and the winding. This path gives a faster decay (figure 7b).

Figure 8 shows a practical example of PWM motor speed control. This circuit includes the oscillator and modulator and allows independent regulation of the speeds of the two motors. The channel inputs are used to control the direction.

An interesting feature of this circuit is that it takes advantage of the threshold of the enable/inhibit input to economise on comparators. The TBA820M audio amplifier generates triangle waves, the DC

level of which is varied from 0 to 5 V by means of P1 and P2.

Since the switching threshold of the L293's enable/inhibit inputs is roughly 2 V the duty cycle of the output current (and hence the motor speed) is controlled by the setting of the potentiometer.

In this circuit the switching frequency is set by $R1/C1$ and the amplitude of the oscillator signal is set by the divider $R2/R3$.

Figure 7a : If the current shown by the solid line is interrupted by bringing A low the current recirculates round the dotted path. Decay is slow.

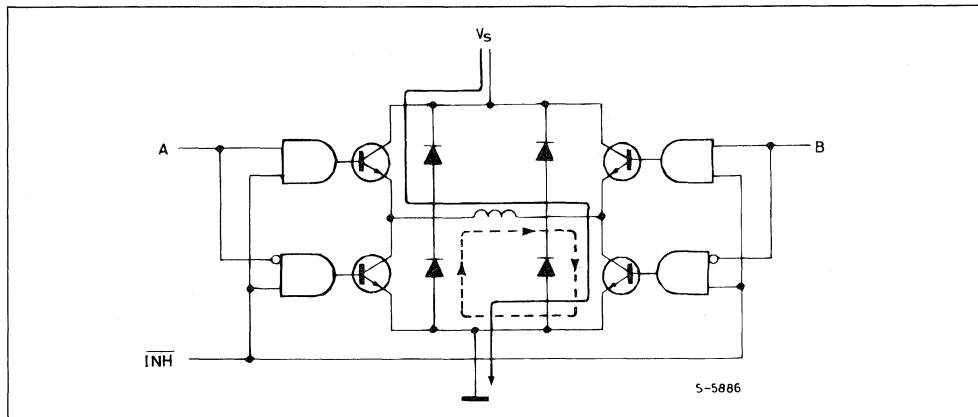


Figure 7b : If the enable input is brought low to interrupt the current indicated by the solid line the current recirculates from ground to V_S and the decay is faster.

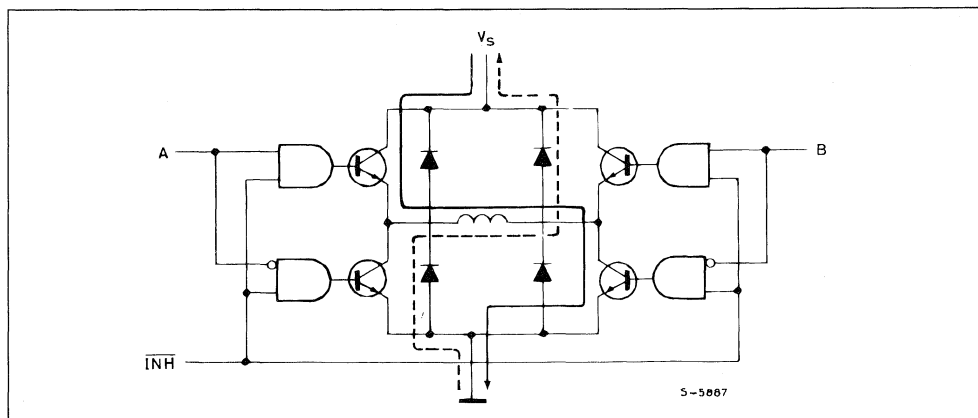
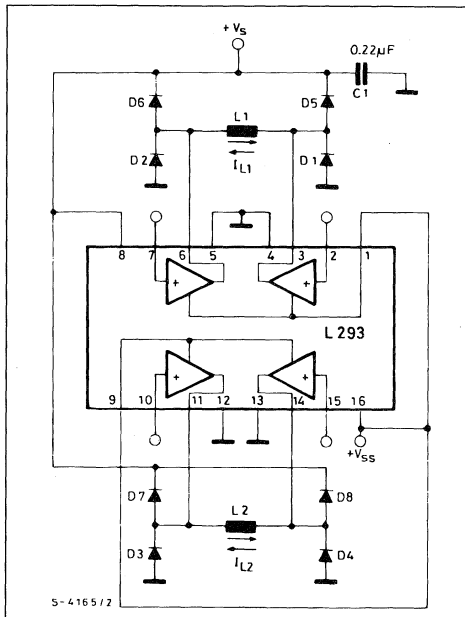


Figure 9 : A single device can be used to drive a two phase bipolar stepper motor.



The peak current in each winding is determined by V_{ref} (in this case it is 0.5 A) and the switching rate - and hence the average current - depends on the hysteresis of the comparator and R4C4. With the component values shown the switching frequency is roughly 20 kHz.

The figure 10 circuit uses only half of the LM339 quad comparator. With the addition of a few extra passive components we can take advantage of the spare comparators to implement short circuit protection. Figure 11 shows how this is done.

As before, comparators 1 and 2 regulate the current in the windings but in this case the connection is different because the inhibit/enable inputs are used for the short circuit protection. The PWM choppers act on the channel inputs through the four clamp diodes D9, D10, D11 and D12. This is a simple trick which allows us to use the channel inputs both for the step sequencing and the choppers.

Comparators 3 and 4 realize the short circuit protection function. Again looking at phase one, compara-

tor 3 operates as a flip flop. Its output is connected to the bridge enable inputs (pins 1 and 11) and is normally high, enabling the drivers. If the output current (sensed by RS1) reaches double the nominal value the comparator CP3 switches, inhibiting the two bridges.

The comparator remains in this state until the V_{SS} supply (5 V) is interrupted. The outputs of comparators 3 and 4 are ORed together so that a short circuit on one phase disables both bridges.

For this circuit V_A should be less than 300 mV (V_A is the voltage on the + input of CP1). From the value chosen for V_A and the desired phase current the sense resistor RS1 (and RS2) is chosen. The current ripple should be at least 30 mA to avoid spurious triggering of CP1 and CP2.

The component values indicated are for a motor with a resistance of $37\ \Omega$ /phase, inductance of $80\ \text{mH}$ /phase and a current of $280\ \text{mA}$ /phase. V_{ref} is $243\ \text{mV}$ giving $V_A = 274\ \text{mV}$ when the output is high and $243\ \text{mV}$ when the output is low. Since $RS1 = 1\ \Omega$ the current in the winding reaches $274\ \text{mA}$ peak and has a ripple of roughly $30\ \text{mA}$. The switching frequency depends on the hysteresis of the comparators and the motor characteristics. For this example the frequency is about $15\ \text{kHz}$.

Stepper motor drive circuits can be simplified using the L297 stepper motor controller which contains a translator to generate the phase sequences plus a dual PWM chopper to regulate the phase currents.

The L297 connects directly to the L293E or L298N as shown in figure 12. This example drives a bipolar stepper motor with winding currents up to 2.5 A. For lower currents an L293E is used and more powerful motors can be driven by two L298N's with paralleled bridges, giving up to 3.5 A.

In this configuration the motor is controlled through the L297. A step clock moves the motor one increment, the **CW/CCW** input controls the direction and the **HALF/FULL** input selects half step or normal operation. The input V_{ref} is connected to a suitable voltage reference and sets the peak winding current in the motor. The choppers in the L297 can operate on the phase lines or the inhibit lines, depending on the state of the logic input called **CONTROL**.

For a more detailed description of the L297 see "Introducing the L297 Stepper Motor Controller".

Figure 11 : With a quad comparator both current regulation and short circuit protection can be obtained.

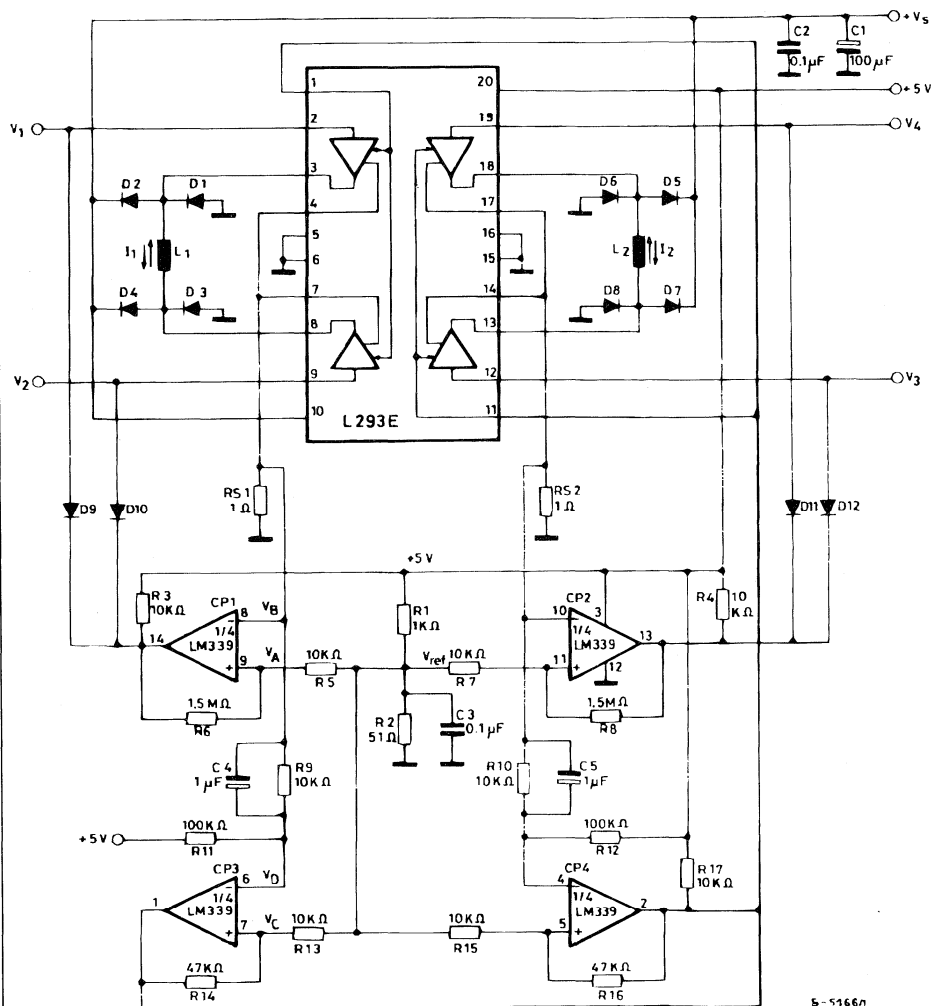
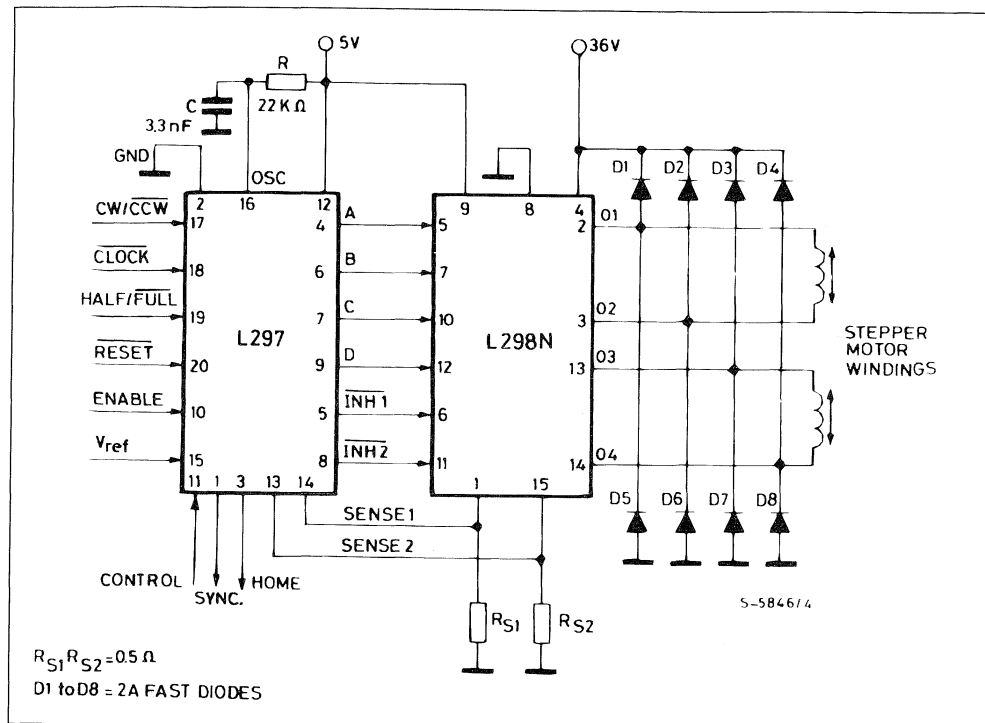


Figure 12 : An L297 stepper motor controller and a L298N driver together from a complete microprocessor-to-stepper motor interface. This circuit drives bipolar stepper motors with winding currents up to 2 A.



SPEED CONTROL OF DC MOTORS WITH THE L292 SWITCH-MODE DRIVER

Power dissipation in DC motor drive systems can be reduced considerably with an L292 switchmode driver. This application guide describes two speed control systems based on this device ; one voltage controlled and one controlled by a 6-bit binary word. Both examples are designed for 60 W motors equipped with tachodynamos.

The L292 is a monolithic power IC which functions effectively as a power transconductance amplifier. It delivers a load current proportional to an input voltage, handling up to 2 A at 18-36 V with a bridge output stage. Completely self-contained, it incorporates internal switchmode circuitry and all the active components to form a current feedback loop.

The L292 is designed primarily for use with an L290 and L291 in DC motor servopositioning applications. However, the L292 can be useful in a wide range of applications as the two examples here show. The first is a simple tachometer feedback circuit, the speed of which is controlled by a DC voltage ; direction is controlled by the polarity of this voltage. The second circuit is controlled digitally and includes an L291 D/A converter.

SYSTEM WITH DC CONTROL

In this system the control quantity is a dc voltage variable between

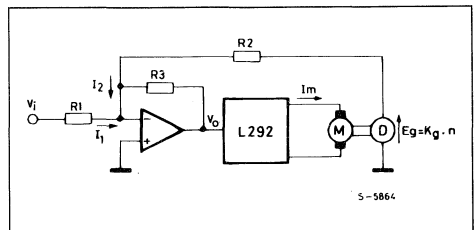
$$+ V_{IM} \text{ and } - V_{IM}$$

Since the quantity under control is the speed of the motor, it is required that it varies linearly in function of the control voltage.

A simplified circuit diagram of the system is shown in fig. 1.

The current I_1 , proportional to the set voltage V_i , and the current I_2 , proportional to the speed of the motor, are fed to the sum point of the error amplifier. Assuming that the motor does not drain current, the system is in a steady-state condition whenever $I_1 = -I_2$; as a matter of fact, in this case the output from the error amplifier V_o is 0V. During transients, the voltage V_o will assume a value $V_o = -R_3(I_1 + I_2)$ and consequently, since the L292 integrated circuit operates as a transconductance (G_m), a mean current $I_m = G_m \cdot V_o$ will flow in the motor determining an acceleration proportional to it.

Figure 1 : Simplified Circuit Diagram of DC control System.



CALCULATION OF R1, R2, R3

Let us call :

- V_{IM} the maximum control voltage value
- n_M the maximum speed allowed for the motor
- K_g voltage constant of the dynamo

By imposing that the balance condition be met in correspondance to the maximum rotation speed the following equation is obtained :

$$I_1 = -I_2 ; \quad \frac{V_{IM}}{R_1} = - \frac{K_g \cdot n_M}{R_2}$$

Since R_2 is the impedance which the tachometer dynamo is loaded on to and its value is recommended by the manufacturer, it is possible from the previous relationship to determine the value of R_1 .

Resistor R_3 determines the system gain. It's best to keep the gain as high as possible (and consequently R_3 as high as possible) to obtain a high response speed of the system, even of for small variations in the control voltage. On the other hand, an excessive gain would cause excessive overshoot around the balance conditions at the end of transients. Consequently, a trade-off must be made between the two opposing requirements in selecting the final gain.

The value for R_3 should be theoretically determined by studying the transfer function, by knowing the electrical and mechanical constants of the motor as well as the load applied to it.

A complete diagram of the circuit actually realized is shown in fig. 2, while fig. 3, shows the characteristic $n = f(V_i)$ obtained.

Resistor R2 drawn in the simplified circuit diagram has been split here in two parts and, in addition, a capacitor has been interposed to ground to filter the signal coming from the tachometer dynamo.

The curve n. 1 in fig. 3 refers to the operation of the motor in no-load condition, with a current drain of 200 mA ; the curve n. 2 refers to a motor loaded so as to drain a current of 1 A. By disregarding the discontinuity around the origin, it can be noted that the characteristics are linear over the whole control voltage range.

By analyzing the curves around the origin, it can be noted that the motor stands still as long as the input signal does not exceed a certain threshold level,

which is as much higher as the current drained by the motor is higher.

Let us call G_m the transconductance of L292, and I the starting current of the motor ; the voltage which must be available at the input of L292 in order that the motor starts turning is :

$$V_o = \frac{I}{G_m} \text{ with } G_m = 220 \frac{\text{mA}}{\text{V}} \text{ (typical value)}$$

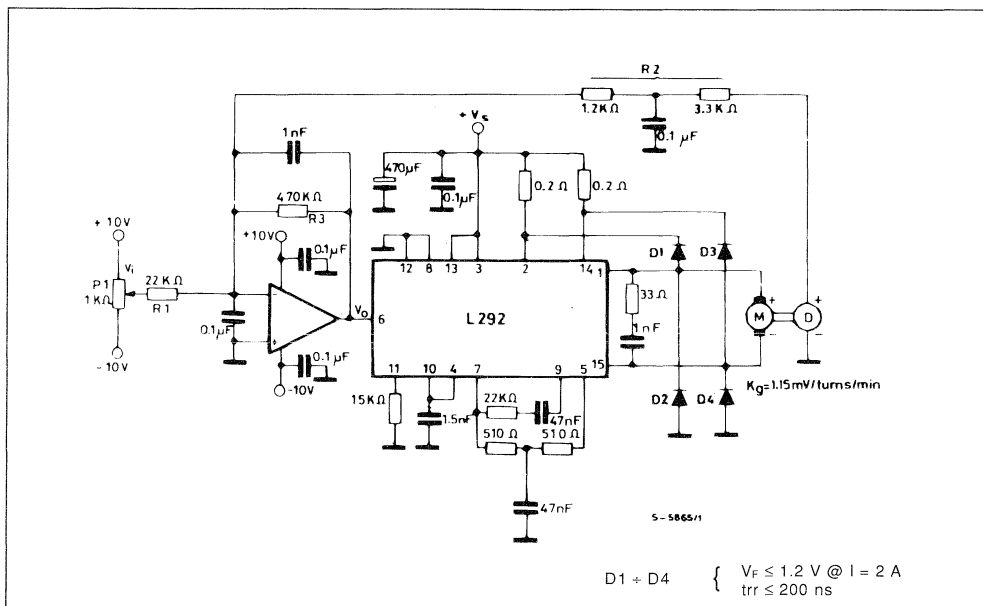
The corresponding control voltage will be :

$$V_i = V_o \cdot \frac{R_1}{R_3} = \frac{I}{G_m} \cdot \frac{R_1}{R_3}$$

and it is as much lower as the gain of the error amplifier is higher.

The presence of a control voltage interval in which the motor stands still, can be useful when it is required that, for a certain position of potentiometer P1 (see fig. 2), the motor speed be zero. An other method to hold the motor still is to use the inhibits of L292, for instance by grounding pin 13.

Figure 2 : Complete Circuit Diagram.



It can be noted from fig. 3 that, by keeping the control voltage V_i constant, the speed varies according to the motor current drain.

Let us call ΔI the current variation ; the voltage variation required at the input of L292 is

$$\Delta V_o = \frac{\Delta I}{G_m}$$

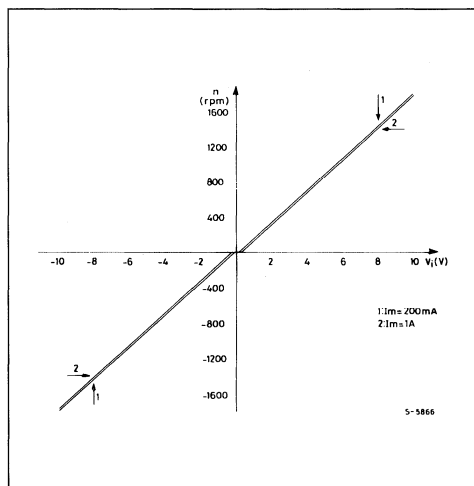
since the control voltage is constant, to generate this ΔV_o it is necessary that the rotation speed be varied by a quantity Δn such as to have :

$$K_g \cdot \Delta n \cdot \frac{R3}{R2} = \Delta V_o = \frac{\Delta I}{G_m}$$

$$\Delta n = \frac{\Delta I}{G_m K_g} \cdot \frac{R2}{R3}$$

(ΔI shall be taken with its sign)

Figure 3 : Output Characteristics of the Circuit in fig. 2.



In this case too, the variation Δn is as much lower as the error amplifier gain is higher. With the circuit shown in fig. 2 Δn is approximately 30 turns/min. with $\Delta I = 800$ mA, $\Delta n = 0.037$ turns/mA.min approx.

It is possible to adopt a circuit which prevents the variation in the number of turns in function of motor current. The problem is to "sense" the current flowing through the motor and to send a current proportional to it to the sum point of the error amplifier. The complete circuit which includes, beside the voltage feed-back loop, also a current feed-back loop, is illustrated in fig. 4.

In the integrated circuit L292, a current proportional to the mean current drained by the motor flows between pin 5 and pin 7.

An operational amplifier amplifies the voltage drop provoked by this current across a 510Ω resistor and sends a current to the sum point which is consequently proportional to the mean current in the motor, the value of which can be made vary by acting on potentiometer P2. By properly adjusting P2, a condition can be achieved in which the speed does not change when the current drained by the motor varies.

The discontinuity around the origin, which was present in the previous circuit (fig. 2), is practically negligible in the circuit shown in fig. 4.

The characteristic $n = f(V_i)$ relevant to the circuit of fig. 4 is shown in fig. 5, and this characteristic does not substantially change over the whole range of currents allowed by the L292 (up to 2A).

In the circuit described above if the motor stall condition is requested. It is preferable to act on the inhibits of the integrated circuit L292, for instance by grounding pin 13, instead of adjusting potentiometer P1 : as a matter of fact, the exact position of this potentiometer is difficult to obtain, since the characteristic crosses the axis V_i in one only point (this mean that n is only 0 for a very narrow interval of V_i).

Figure 4 : Complete Circuit with Current Feedback.

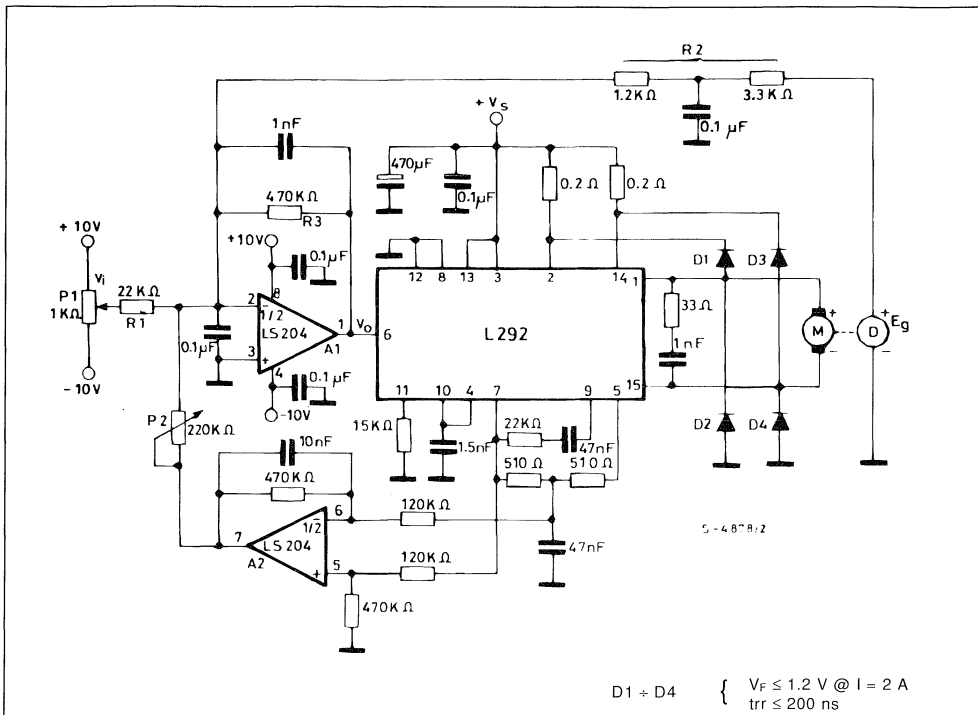
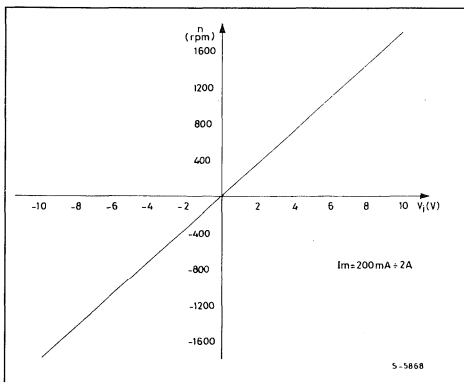


Figure 5 : Output Characteristics of the Circuit in fig. 4.



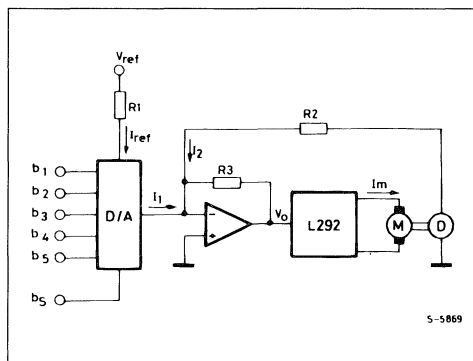
SYSTEM WITH DIGITAL CONTROL

In this system the speed information is given to the circuit by a binary code made up of 5 information bits plus one sign bit, which determines whether the

movement shall be clockwise or counter-clockwise. For the circuit implementation, the integrated circuits L291 (which includes a D/A converter and two operational amplifiers) and L292 are used.

A simplified circuit diagram is shown in fig. 6.

Figure 6 : Simplified Circuit Diagram (digital control).



The current value I_1 depends on the value of I_{ref} and on the value of inputs b_1 through b_5 , where its sign depends on the b_5 input.

The maximum value for I_1 , which is obtained whenever inputs b_1 through b_5 are low, is :

$$I_{1 \max} = I_{ref} \cdot \frac{31}{16} = \frac{V_{ref}}{R1} \cdot \frac{31}{16}$$

In order to have the system in a steady state condition (no current drained by the motor), it must be :

$$I_1 = -I_2$$

By imposing the balance condition at the maximum speed, one obtains : $I_{1 \max} = -I_{2 \max}$

$$\frac{V_{ref}}{R1} \cdot \frac{31}{16} = \frac{K_g \cdot n_M}{R2}$$

where

K_g = dynamo's voltage constant

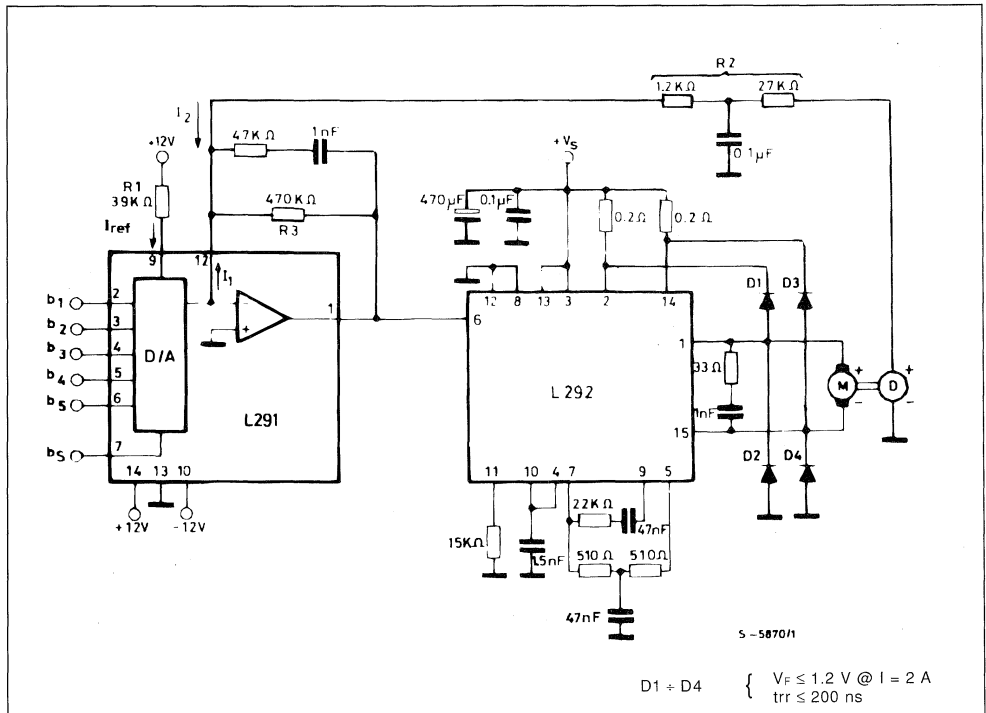
n_M = maximum speed preset for the motor.

The current I_{ref} , and consequently the ratio $V_{ref}/R1$, must lie within a certain range imposed by the D/A converter actually used.

In our case, this range is 0.3 to 1 mA. The values of $R1$ and $R2$ can be determined from the previous relationship. The same considerations made in the description of the DC control system apply for the selection of $R3$.

A complete diagram of the circuit implemented is indicated in fig. 7, while the input versus output characteristics is shown in fig. 8.

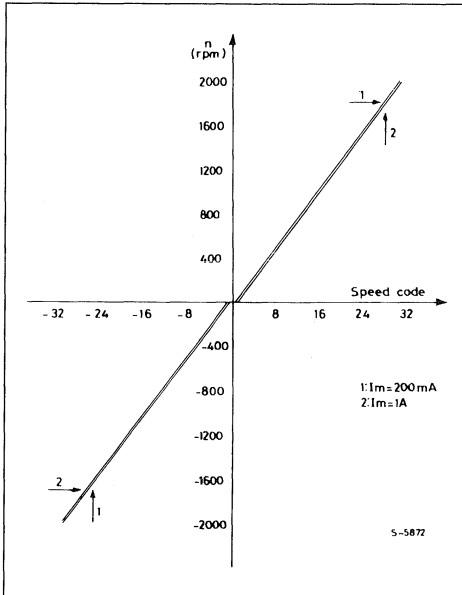
Figure 7 : Complete Circuit Diagram.



In the graph of fig. 8 the rotation speed of the motor is represented on ordinates, while the decimal speed code, corresponding to the binary code applied to inputs b_1 through b_5 , is represented on abscissae.

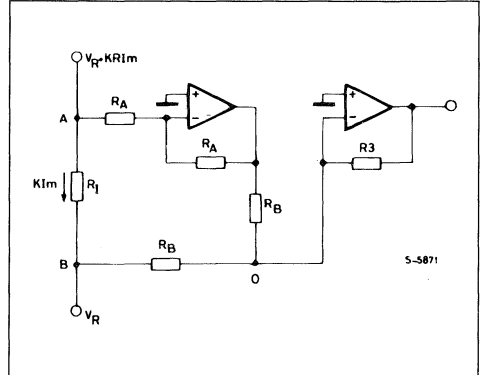
The abscissa 1 corresponds to the minimum speed code, i.e. input b_1 low and remaining inputs high, since the least significant input is b_1 and the active status of inputs is low. The abscissa 31 corresponds to the maximum speed code, i.e. all inputs b_1 through b_5 low. The negative abscissae have been obtained by changing the status of the b_5 input. The graph in fig. 8 should have been made up of a number of dots; these dots have been joined together with an uninterrupted line for convenience. This graph has the same features as the graph in fig. 3, i.e. the curve features a discontinuity around the origin, and it lowers as long as the motor current drain increases. In this case too, the circuit in fig. 7 can be modified in order to prevent that the speed vary in function of the motor load, by adding a current loop in the control circuit, by using the remaining operational amplifier available in the integrated circuit L291.

Figure 8 : Output Characteristic of the Circuit in fig. 7.



Since this amplifier has only the inverting input available, while the non-inverting input is grounded, a circuit arrangement as schematically shown in fig. 9 has been adopted in order to have an output signal referred to ground, given an input signal referred to a reference voltage (in L292) of approximately 8 V.

Figure 9 : Translator Circuit.



Resistors R_A and R_B must be high-precision resistors in order to have output 0 with no I_m current present. In the practical implementation, resistors with an accuracy of 5 % are used and the ends of a potentiometer are interposed between resistors R_B and the output to the sum point of the error amplifier is made through the cursor. The gain of this current loop is proportional to the ratio R_3/R_B . A complete circuit diagram is shown in fig. 10.

Since, for reasons of gain, resistor R_B must be 27 k Ω and, if connected to pin 7 of L292, should have subtracted too much current by thus affecting the correct operation of L292, it has been connected to pin 11, having the same potential as pin 7. Consequently, the resistance value between pin 11 and ground has been modified, in order to maintain the switching frequency of L292 unchanged. In order to have a correct adjustment of potentiometer P1, it is enough to set the 0 speed code (b_1 through b_5 high) and turn the cursor until the motor stops.

The input versus output characteristic obtained with the circuit of fig. 10 is indicated in fig. 11.

Figure 10 : Complete Circuit with Current Feedback.

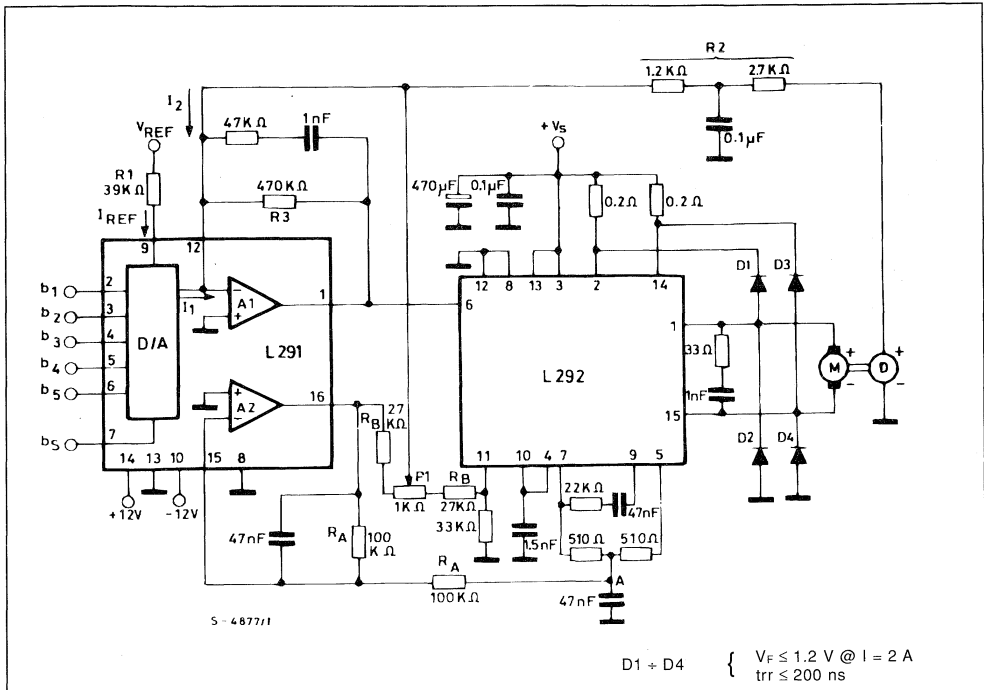
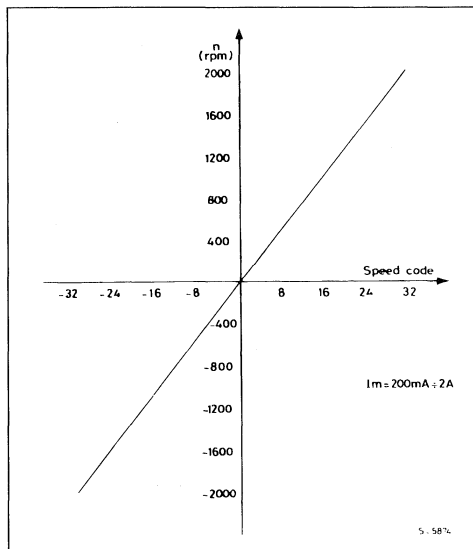


Figure 11 : Output Characteristic of the Circuit in fig. 10.



RESPONSE TO INPUT STEP

Measurements have been taken on the circuits described in the previous paragraphs, in order to analyze how the motor speed varies when a step variation is imposed to the input.

For the system DC control, the control voltage has been changed from 0 to the maximum value V_{IM} and down to 0 again. For the digital system the speed code has been changed from 0 (b_1 through b_5 high) to the maximum value (b_1 through b_5 low) and down to 0 again. When the control quantity changes from 0 to the maximum value, the output voltage of the error amplifier (V_o , fig. 1 and fig. 6) assumes its maximum value, since the feed-back signal coming from the tachometer dynamo initially 0. In these conditions, L292 supplies the motor with the maximum current (2A) and maintains it until the motor speed is sufficiently close to the maximum value.

Since the motor is powered from a constant current, it moves with a constant current, it moves with a constant acceleration and consequently its speed grows linearly from 0 up to the maximum value over the time interval t_a . The time needed for the motor to reach the maximum speed also depends, besides

the current, on the electrical and mechanical characteristics of the motor and on the moment of inertia of the load applied to the motor. When the control quantity changes from the maximum value to 0, the output of the error amplifier V_o assumes the maximum value, but with an opposite sign with respect to the previous case, and the current flowing in the motor is also reversed and tends to brake it, by making the speed linearly decrease from the maximum value down to 0 over the time period t_f . The no-load characteristics, relevant to the motor used for the previous tests, are shown in fig. 12. The times t_a and t_f are not equal to each other, which circumstance is basically due to the frictions which, during the acceleration phase, oppose increase of speed, while during the deceleration phase they contribute to make the speed decrease. As a matter of fact, from the movement equation :

$$J \ddot{\theta} + D \dot{\theta} + T_f = K_T I_M$$

where :

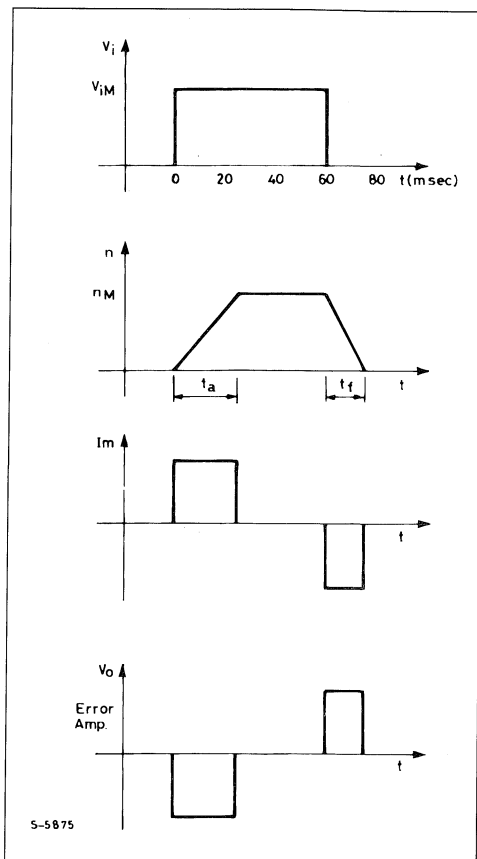
- J = System moment of inertia
- D = Coefficient of viscous friction
- T_f = Braking couple
- K_t = Motor constant
- $\dot{\theta}$ = Angular speed
- $\ddot{\theta}$ = Angular acceleration

and by disregarding the term $D\ddot{\theta}$, one obtains :

$$\ddot{\theta} = \frac{K_T \cdot I_M - T_f}{J}$$

where from it can be seen that $|\ddot{\theta}|$ is greater if I_M is negative.

Figure 12 : Pulse Response.



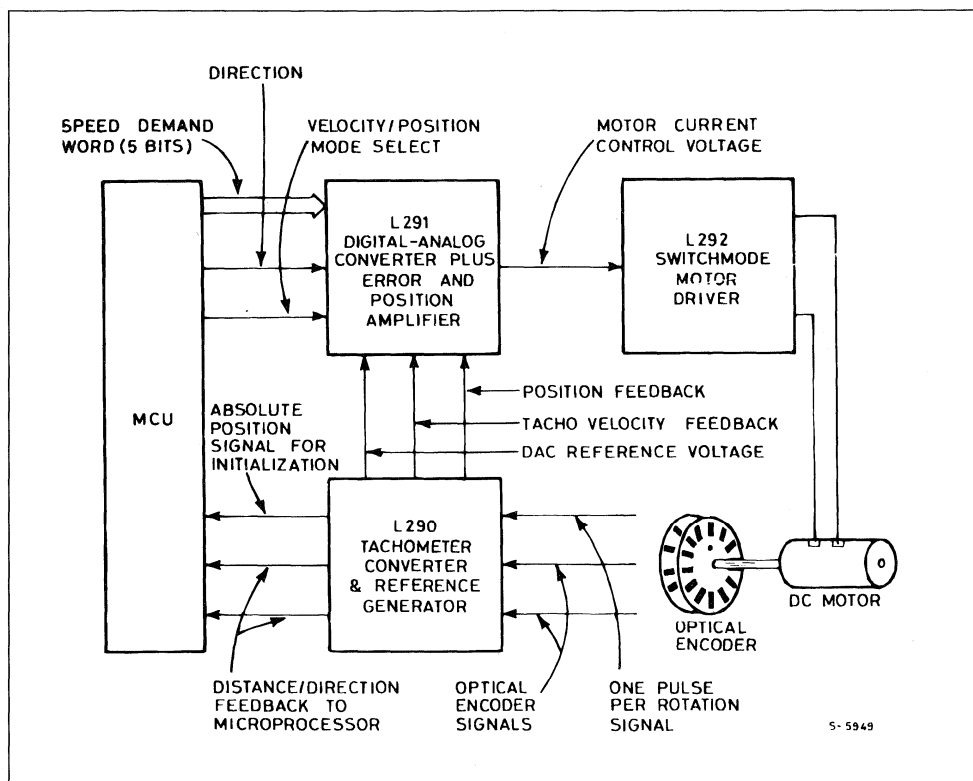
THE L290/L291/L292 DC MOTOR SPEED/POSITION CONTROL SYSTEM

The L290, L291 and L292 together form a complete microprocessor-controlled DC motor servopositioning system that is both fast and accurate. This design guide presents a description of the system, detailed function descriptions of each device and application information.

The L290, L291 and L292 are primarily intended for use with a DC motor and optical encoder in the configuration shown schematically in figure 1. This system is controlled by a microprocessor, or microcomputer, which determines the optimum speed profile for each movement and passes appropriate commands to the L291, which contains the system's D/A converter and error amplifiers. the

L291 generates a voltage control signal to drive the L292 switchmode driver which powers the motor. An optical encoder on the motor shaft provides signals which are processed by the L290 tachometer converter to produce tacho voltage feedback and position feedback signals for the L291 plus distance/direction feedback signals for the control micro.

Figure 1 : The L290, L291 and L292 form a complete DC Motor servopositioning System that connects directly to Microcomputer Chips.



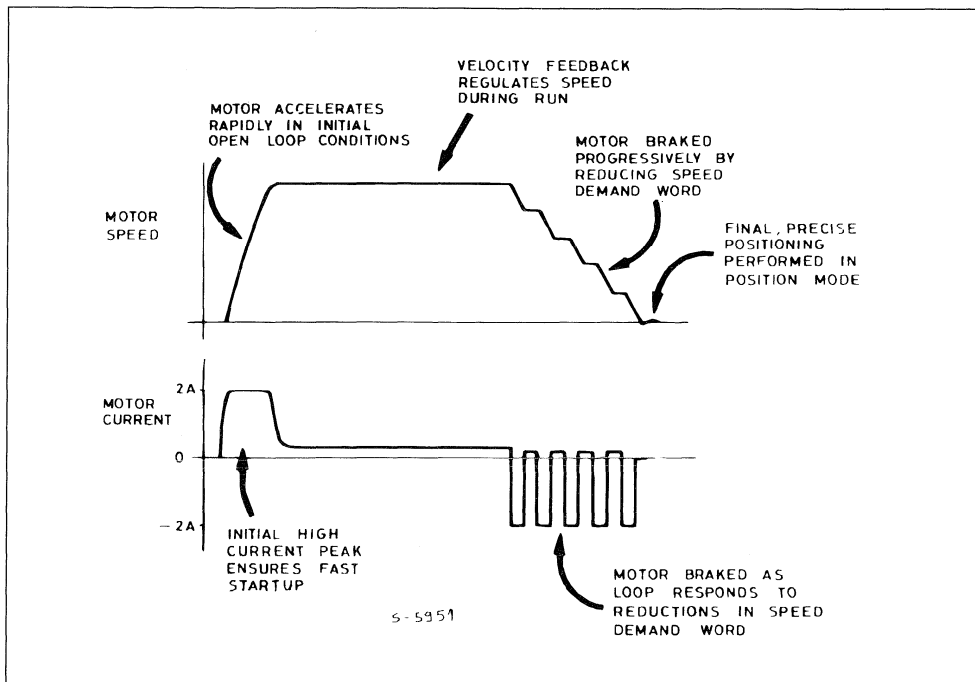
The system operates in two modes to achieve high speed and accuracy : closed loop speed control and closed loop position control. The combination of these two modes allows the system to travel rapidly towards the target position then stop precisely without ringing.

Initially the system operates in speed control mode. A movement begins when the microcomputer applies a speed demand word to the L291, typically calling for maximum speed. At this instant the motor speed is zero so there is no tacho feedback and the system operates effectively in open loop mode (see figure 2). In this condition a high current peak - up to 2A - accelerates the motor rapidly to ensure a fast start.

As the motor accelerates the tacho voltage rises and the system operates in closed loop speed mode, moving rapidly forwards the target position. The microcomputer, which is monitoring the optical encoder signals (squared by the L290), reduces the speed demand word gradually when the target position is close. Each time the speed demand word is reduced the motor is braked by the speed control loop.

Finally, when the speed code is zero and the target position extremely close, the micro commands the system to switch to position mode. The motor then stops rapidly at the desired position and is held in an electronic detent.

Figure 2 : The System operates in two Modes to achieve High Speed and Accuracy. Tachometer Feedback regulates the Speed during a Run and brakes the Motor towards the End. Position Feedback allows a Precise Final Positioning.



OPTICAL ENCODER

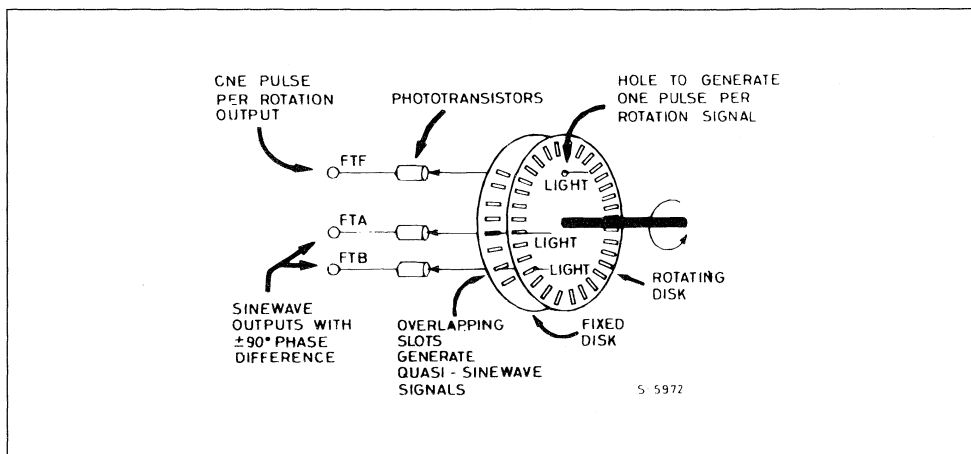
The optical encoder used in this system is shown schematically in figure 3. It consists of a rotating slotted disk and a fixed partial disk, also slotted.

Light sources and sensors are mounted so that the encoder generates two quasi-sinusoidal signals with a phase difference of $\pm 90^\circ$. These signals are referred to as FTA and FTB. The frequency of these signals indicates the speed of rotation and the rela

tive phase difference indicates the direction of rotation. An example of this type is the Sensor Technology STRE 1601, which has 200 tracks. Similar types are available from a number of manufacturers including Sharp and Eleprint.

This encoder generates a third signal, FTF, which consists of one pulse per rotation. FTF is used to find the absolute position at initialization.

Figure 3 : The System operates with an Optical Encoder of the Type shown schematically here. It generates two Signals 90° out of Phase plus a one Pulse-per-rotation Signal.



THE L290 TACHOMETER CONVERTER

The L290 tachometer converter processes the three optical encoder signals FTA, FTB, FTF to generate a tachometer voltage, a position signal and feedback signals for the microprocessor. It also generates a reference voltage for the system's D/A converter.

Analytically, the tacho generation function can be expressed as :

$$\text{TACHO} = \frac{dV_{AB}}{dt} \cdot \frac{\text{FTA}}{|\text{FTA}|} - \frac{dV_{AA}}{dt} \cdot \frac{\text{FTB}}{|\text{FTB}|}$$

In the L290 (block diagram, figure 4) this function is implemented by amplifying FTA and FTB in A1 and A2 to produce V_{AA} and V_{AB} . V_{AA} and V_{AB} are differentiated by external RC networks to give the signals V_{MA} and V_{MB} which are phase shifted and proportional in amplitude to the speed of rotation. V_{MA} and V_{MB} are passed to multipliers, the second inputs of which are the sign of the other signal before differentiation.

The sign $\left(\frac{\text{FTA}}{|\text{FTA}|} \text{ or } \frac{\text{FTB}}{|\text{FTB}|} \right)$ is provided by the

comparators CS1 and CS2. Finally, the multiplier outputs are summed by A3 to give the tacho signal. Figure 5 shows the waveforms for this process.

This seemingly complex approach has three important advantages. First, since the peaks and nulls of CSA and CSB tend to cancel out, the ripple is very small. Secondly, the ripple frequency is the fourth harmonic of the fundamental so it can be filtered easily without limiting the bandwidth of the speed loop. Finally, it is possible to acquire tacho information much more rapidly, giving a good response time and transient response.

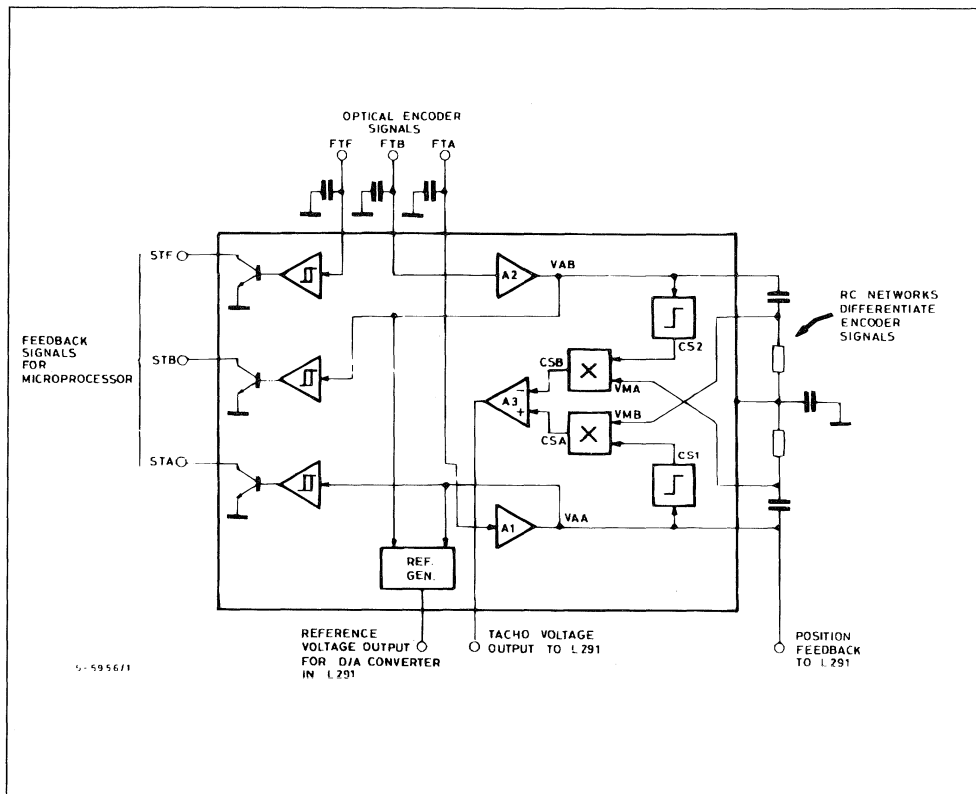
Feedback signals for the microprocessor, STA, STB and STF, are generated by squaring FTA, FTB and FTF. STA and STB are used by the micro to keep track of position and STF is used at initialization to find the absolute position.

Position feedback for the L291 is obtained simply from the output of A1.

The L290 also generates a reference voltage for the L291's D/A converter. This reference is derived from V_{AA} and V_{AB} with the function :

$$V_{ref} \equiv |V_{AA}| + |V_{AB}|$$

Figure 4 : The L290 processes the Encoder Signals, generating a Tacho Voltage and Position Signal for the L291 plus Feedback Signals for the Microprocessor. Additionally, it generates a Reference Voltage for the L291's D/A Converter.



Since the tacho voltage is also derived from V_{AA} and V_{AB} it follows that the system is self compensating and can tolerate variations in input levels, temperature changes and component ageing with no deterioration of performance.

Figure 5 : These Waveforms illustrate the Generation of the Tacho Voltage in the L290. Note that the Ripple is fourth Harmonic. The Amplitude of TACHO is proportional to the Speed of Rotation.

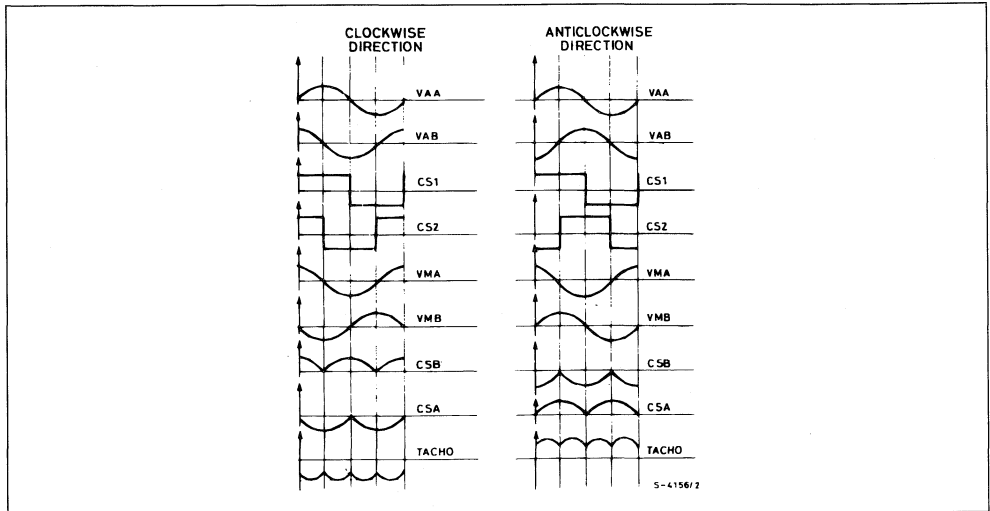
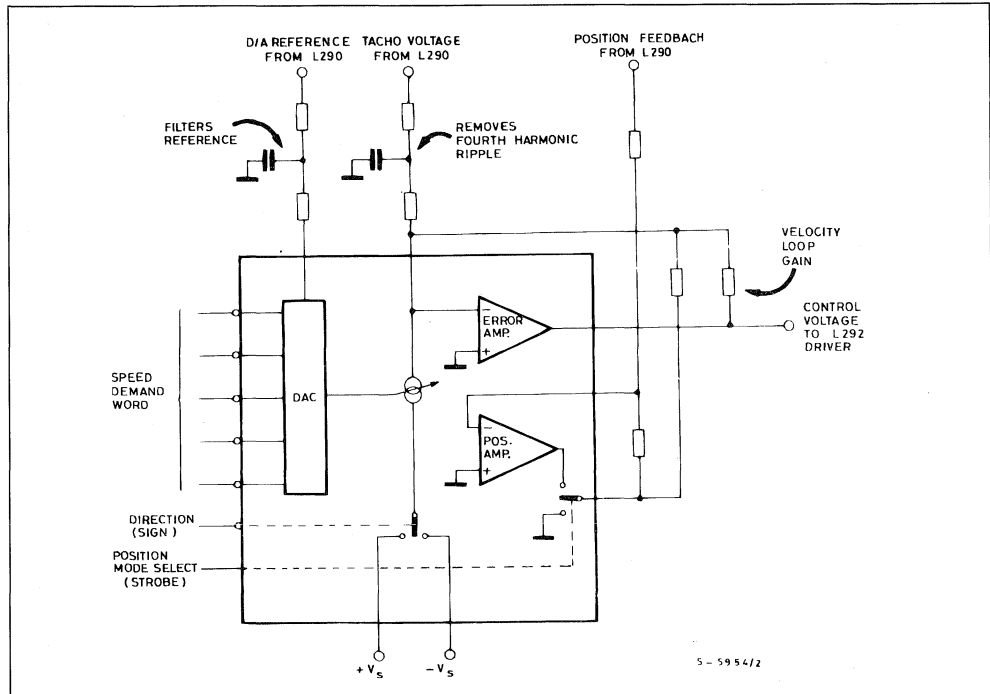


Figure 6 : The L291 Links the System to the Microprocessor. It contains the system DA converter, main error amplifier and position amplifier.



THE L291 D/A CONVERTER AND AMPLIFIERS

The L291, shown in figure 6, links the system to the micro and contains the system's main error amplifier plus a position amplifier which allows independent adjustment of the characteristics of the position loop.

It contains a five bit D/A converter with switchable polarity that takes its reference from the L290. The polarity, which controls the motor direction, is controlled by the micro using the SIGN input.

The main error amplifier sums the D/A converter output and the tachometer signal to produce the motor drive signal ERRV. The position amplifier is provided to allow independent adjustment of the position loop gain characteristics and is switched in/out of circuit to select the mode. The final position mode is actually 'speed plus position' but since the tachometer voltage is almost zero when position mode is selected the effect of the speed loop is negligible.

THE L292 SWITCHMODE MOTOR DRIVER

The L292 can be considered as a power transconductance amplifier - it delivers a motor current proportional to the control voltage (ERRV) from the L291. It drives the motor efficiently in switchmode and incorporates an internal current feedback loop to ensure that the motor current is always proportional to the input control signal.

The input control signal (see block diagram, figure 7) is first shifted to produce a unipolar signal (the L292 has a single supply) and passed to the error amplifier where it is summed with the current feedback signal. The resulting error signal is used to modulate the switching pulses that drive the output stage.

External sense resistors monitor the load current, feeding back motor current information to the error amplifier via the current sensing amplifier.

The L292 incorporates its own voltage reference and all the functions required for closed loop current control of the motor. Further, it features two enable inputs, one of which is useful to implement a power on inhibit function.

The L292's output stage is a bridge configuration capable of handling up to 2A at 36V. A full bridge stage was chosen because it allows a supply voltage to the motor effectively twice the voltage allowed if a half bridge is used. A single supply was chosen to avoid problems associated with pump-back energy.

In a double supply configuration, such as the example in figure 8 a, current flows for most of the time through D1 and Q1. A certain amount of power is thus taken from one supply and pumped back into the other. Capacitor C1 is charged and its voltage can rise excessively, risking damage to the associated electronics.

By contrast, in a single supply configuration like figure 8b the single supply capacitor participates in both the conduction and recirculation phases. The average current is such that power is always taken from the supply and the problem of an uncontrolled increase in capacitor voltage does not arise.

A problem associated with the system used in the L292 is the danger of simultaneous conduction in both legs of the output bridge which could destroy the device. To overcome this problem the comparator which drives the final stage consists of two separate comparators (figure 9). Both receive the same V_t , the triangular wave from the oscillator, signal but on opposite inputs.

Figure 7 : The L292 Switchmode Driver receives a Control Voltage from the L291 and delivers a switchmode regulated Current to the Motor.

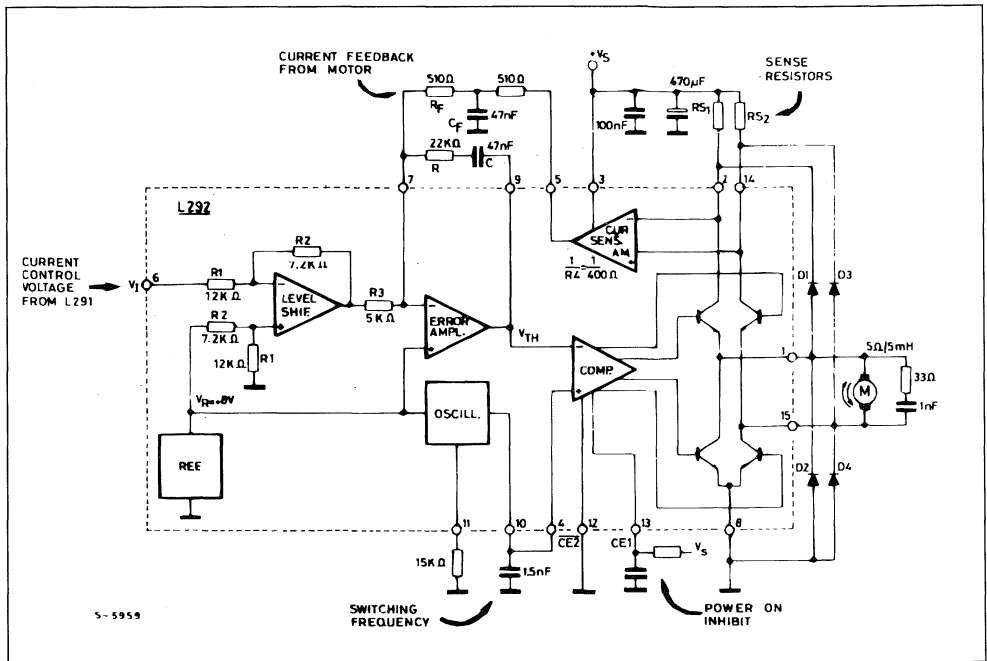
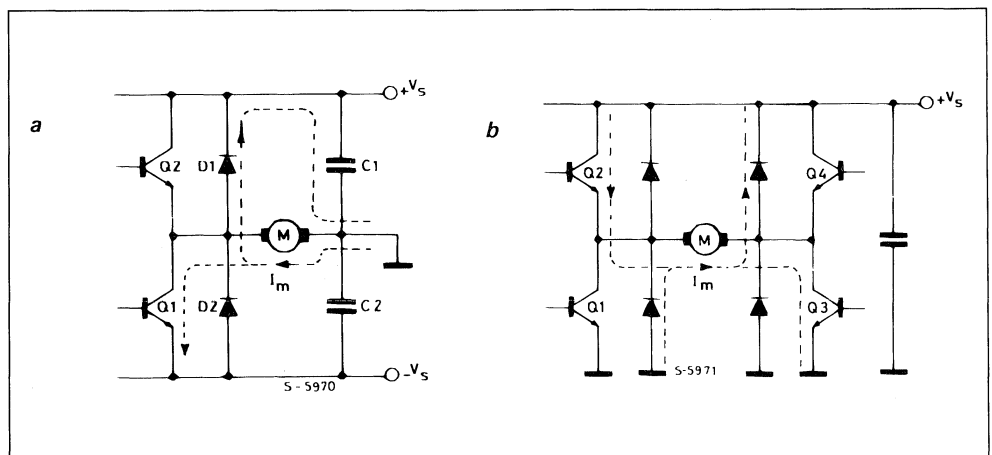
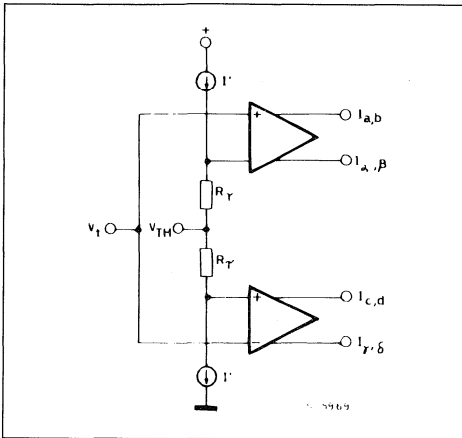


Figure 8 : A Simple Push Pull Output (a) needs a Split Supply and the Device can be damaged by the Voltage Built up on C1. The L292 has a Bridge Output to avoid these Problems. Only one Supply is needed and the Voltage across the Single Capacitor never rises excessively. Moreover, the Motor can be supplied with a Voltage up to twice the Voltage allowed with a Half Bridge.



The other two inputs are driven by V_{TH} , the error amplifier output, shifted by plus or minus $R_T I'$. This voltage shift, when compared with V_t , results in a delay in switching from one comparator to the other.

Figure 9 : The L292's final Comparator actually consists of two Comparators. This Configuration introduces a Delay to prevent simultaneous Conduction of two Legs.

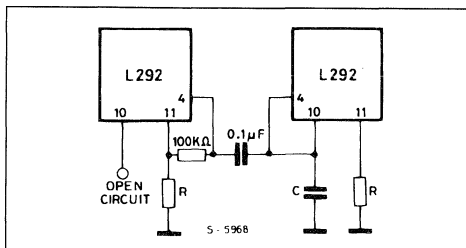


Consequently there will always be a delay between switching off one leg of the bridge and switching on the other. The delay τ is a function of the integrated resistor R_T (1.5k Ω) and an external capacitor C17 connected to pin 10 which also fixes the oscillator frequency. The delay is given by :

$$\tau = R_T C17$$

In multiple L292 configurations (in a typewriter, for example, there may be two systems) it is desirable to synchronise the switching frequencies to avoid intermodulation. This can be done using the configuration shown in figure 10.

Figure 10 : Ground Plane switching Noise and Modulation Phenomena are avoided in Multi-L292 Systems by synchronizing the Chopper Rate with this RC Network.

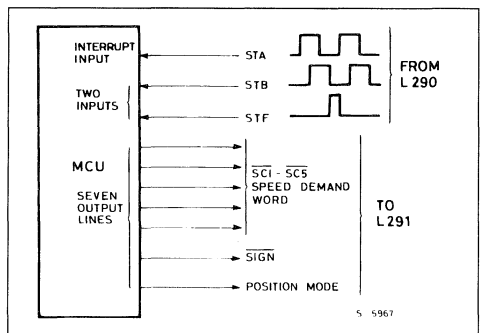


SOFTWARE AND INTERFACING TO THE MICRO

In a typical system the L290/1/2 system is connected to the control microcomputer through ten I/O lines : seven outputs and three inputs.

The outputs are all connected to the L291 D/A converter and consist of the five bit speed demand word, SIGN (which sets the direction) and the speed/position mode select line. Position feedback for the micro comes from the L290 tachometer converter and consists of the signals STA, STB (the squared encoder outputs) plus the one-pulse-per rotation signal, STF (figure 11).

Figure 11 : In a typical system the L290/L291/L292 combination is linked to the micro through seven output lines, two inputs and an interrupt input.



To follow the motor position the micro counts the STA pulses to measure the distance travelled and compares the phase of STA and STB to sense the direction. The most convenient way to do this is to connect the STA line to an interrupt input. An interrupt service routine will then sample STB and increment or decrement the position count depending on the relative phase difference : + 90° if STB is high ; -90° if STB is low.

It could be argued that the micro doesn't need to sense the direction of the rotation because it controls the direction. In practice, however, it is better to sense the direction to allow for the possibility that the motor may be moved by externally applied forces.

For each movement the micro calculates the distance to be travelled and determines the correct direction. It then sets the L291 to velocity feedback mode, sets the director appropriately and sets the speed demand word for maximum speed (possibly less if the move is very short).

By means of the STA interrupt service routine it follows the changing position, reducing the speed de-

Figure 13 : P.C. Board and Component layout (1 : 1 scale).

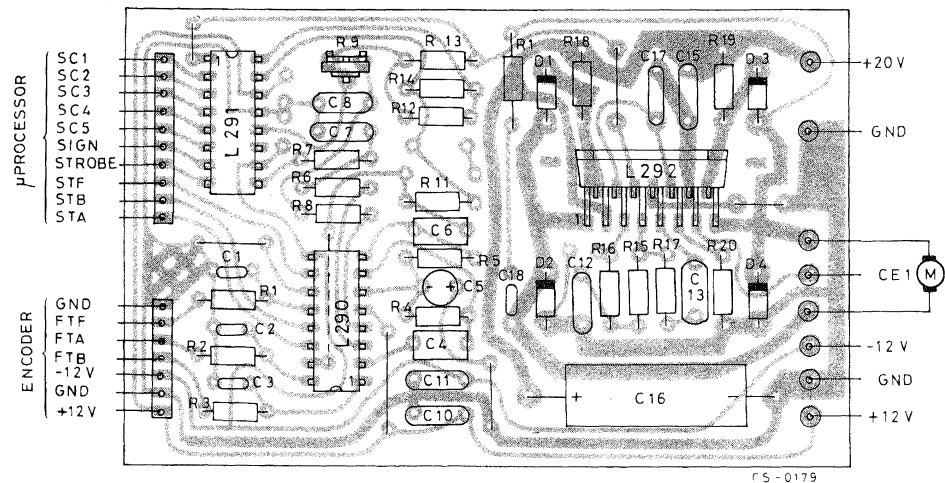


Figure 14.

Component	Recommended Value	Purpose	Larger than Recommended Value	Smaller than Recommended Value
R1, R2, R3	1 k Ω	To filter the noise on the encoder signals.	Offset voltage increase (V_{AA} , V_{AB}).	
R4, R5	820 Ω	Differentiator Network	Tacho offset and tacho signal increase.	Tacho offset increase. Tacho signal decrease.
R6, R7	4.7 k Ω	To set the D/A input current.	D/A input current decrease.	D/A input current increase.
R8	4.7 k Ω	To set the motor speed.	Motor speed increase.	Motor speed decrease.
R9	5 k Ω	To adjust the motor speed.	Danger of Oscillation $R9 \leq R13/10$	
R11	22 k Ω	To set the position loop gain.	– Position loop gain decrease.	– Position loop gain increase. – Danger of oscillation of the motor shaft.
R12	100 k Ω	To set the position loop gain.	– Position loop gain decrease.	– Position loop gain increase. – Danger of oscillation of the motor shaft.
R13	120 k Ω	To set the speed loop gain.	– Speed loop gain increase.	– Speed loop gain decrease.
R14	15 k Ω	To set the position loop gain.	– Position loop gain increase. – Danger of oscillation of the motor	– Position loop gain decrease.
R15, R16	510 Ω	To filter the feedback current.	Danger of output saturation of the current sensing amplifier $R15 + R16 \leq 3.3 \text{ k}\Omega$.	

Figure 14 : (continued).

Component	Recommended Value	Purpose	Larger than Recommended Value	Smaller than Recommended Value
R17	22 k Ω	To set the gain of the err. amplifier.	Increase of the gain at high frequencies.	Danger of Oscillations R17 > 5.6 k Ω
R18, R19	0.2 Ω	To set the transconductance value of the L292.	Transconductance decrease (R18 , R15). $I_m \leq 0.44$ V.	Transconductance increase.
R20	15 k Ω	To set the oscillator frequency.	Oscillator frequency decrease.	Oscillator frequency increase. R20 $\geq$ 8.2 k Ω
R 21	33 Ω	Compensation Network		Increase of the peak current in the output transistors during the communications.
C1, C2, C3	100 pF	To filter the noise on the encoder signals.	Bandwidth reduction of the low pass filter.	Bandwidth increment of the low pass filter.
C4, C6	15 nF	Differentiator Network	Tacho signal increase.	Tacho signal Decrease.
C5	2.2 μ F	By-pass Capacitor	Larger set-up time after power on.	Reduced by-pass effect at low frequencies.
C7	0.1 μ F	Low-pass filter for the D/A input current.		Increase of the current ripple at low speed.
C8	0.22 μ	- Low pass filter for the tacho signal. - To determine the dominant pole of the speed loop.	Bandwidth reduction of the speed loop.	Low filtering at low speed, causing noise on the motor.
C10, C11	0.1 μ F	Supply By-pass Capacitor		Danger of Oscillations.
C12	47 nF	To filter the feedback current	- Lower value of the damping factor. - Danger of Oscillations	Higher value of dumping factor.
C13	47 nF	To set the gain of the error amplifier C13 - R17 = L_M/R_M		
C15	0.1 μ F	Supply By-pass Capacitor		Danger of Oscillations
C16	470 μ F	Supply By-pass Capacitor		Ripple increment on the supply voltage.
C17	1.5 nF	To set the oscillator frequency and the dead time of the output transistors.	- Oscillation Frequency Reduction - Dead time increment.	- Oscillation Frequency Increment - Dead time reduction.
C18	1 nF	Compensation Network		Danger of Oscillations
D1, D2, D3, D4	1 A Fast Diodes	Recirculation Diodes		

APPLICATION CIRCUITS

The complete circuit is shown in figure 12 ; a suitable layout for evaluation is given in figure 13. Component values indicated are for a typical system using a Sensor Technology STRE1601 encoder and a motor with a winding resistance of 5Ω and an inductance of 5mH (this motor is described fully in figure 17). How to calculate values for other motors is explained further on.

Figure 14 explains what each component does and what happens if it is varied. Maximum and minimum values are also indicated where appropriate.

ADDING DISCRETE TRANSISTORS FOR HIGHER POWER

In the basic application, the L292 driver delivers 2 A to the motor at 36V. This is fairly impressive for an integrated circuit but not enough for some applications - robots, machine tools etc. The basic system can be expanded to accommodate these applications by adding external power transistors to the L292.

This is preferable to simply adding a discrete driver stage in place of the L292 because the L292's current control loop is very useful.

Figure 15 shows how four transistors are added to increase the current to 4, 6 or 8A, depending on the choice of transistor. When coupled to the L290 and L291 this configuration appears to the system as an L292.

The average motor current, I_m , is found from :

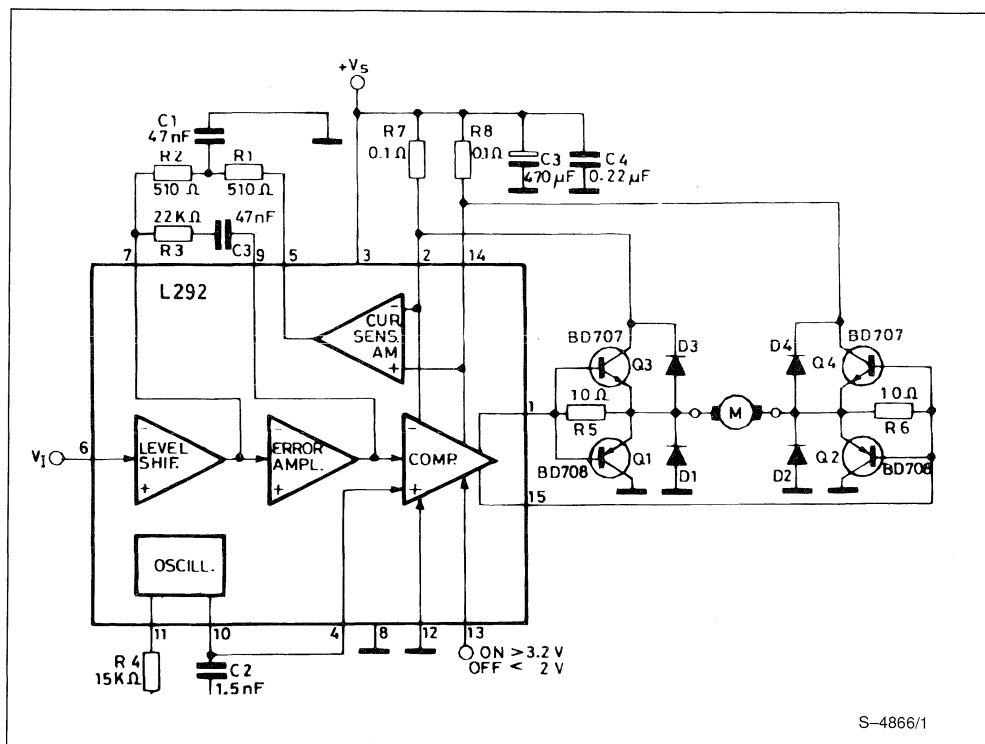
$$I_m = \frac{V_i 0.044}{R_x}$$

Where V_i is the input voltage and R_x is the value of the sense and resistors R7 and R8.

Suitable transistors for this configuration are indicated below :

I(A)	V_i (V)	R_x (m Ω)	Q1, Q2	Q3, Q4	D1 - D4
4	9.1	100	BD708	BD707	2A Fast Diodes
6	9.1	65	BD908	BD907	3A Fast Diodes
8	9.1	50	BDW52A	BDW51A	4A Fast Diodes

Figure 15 : For higher power external transistors are added to the L292. This circuit delivers up to 4A, if 2 BDW51A and 2 BDW52A are used it can deliver 8A.



S-4866/1

The circuit shown in figure 16 is suitable for motor currents up to 50A at voltages to 150V. Two supplies are used ; 24V for the L292 and LS141 and 150V for the external transistors and motor. This circuit too behaves just like an L292, except for the higher power, and connects to the L290 and L291 as usual.

The motor current is given by :

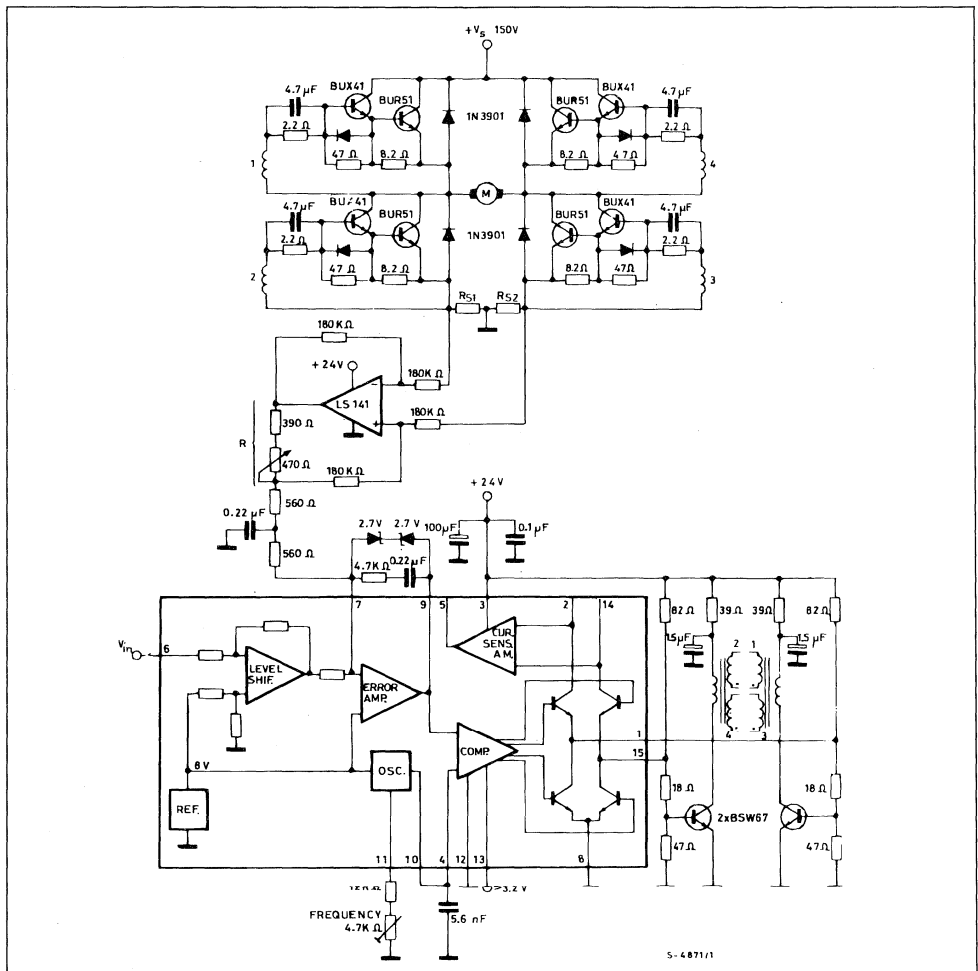
$$I_m = \frac{V_{in} \times 120 \times 10^{-6} R}{R_s}$$

where $R_s = R_{s1} = R_{s2} = 12 \times 10^{-3} \Omega$
and $390 \Omega < R < 860 \Omega$

This gives a range of transconductance values (I_m/V_{in}) from 3.0A/V ($R = 390 \Omega$) to 8.6A/V ($R = 860 \Omega$).

In this circuit the L292 drives two transformers whose secondaries drive the power transistors. The coil ratio of the transformers is 1 : 20. To limit the duty cycle at which the transformers operate from 15% to 85%, two zener diodes are inserted between pin 7 and pin 9 of the L292. The LS141 op amp supplies current feedback from the transistor bridge to the L292.

Figure 16 : For higher voltages and currents—up to 150V at 50A, this circuit can be used. It connects to the L290 and L291, behaving just like an L292.



DESIGN CONSIDERATIONS

The application circuit of figure 12 will have to be adapted in most cases to suit the desired performance, motor characteristics, mechanical system characteristics and encoder characteristics. Essentially this adaptation consists of choosing appropriate values for the ten or so components that determine the characteristics of the L290, L291 and L292.

The calculations include :

- Calculation of maximum speed and acceleration ; useful both for defining the control algorithm and setting the maximum speed.
- Calculation of R8 and R9 to set maximum speed.
- Laplace analysis of system to set C8, R11, R12, R13 and R14.
- Laplace analysis of L292 loop to set the sensing resistors and C12, C13, R15, R16, R17.
- Calculation of values for C4 and C6 to set max level of tach signal.
- Calculation of values for R6 and R7 to set D/A reference current.
- Calculation of R20 to set desired switching frequency.

MAXIMUM ACCELERATION

For a permanent magnet DC motor the acceleration torque is related to the motor current by the expression :

$$T_a + T_f = K_T I_m$$

where :

- I_m is the motor current
- K_T is the motor torque constant
- T_a is the acceleration torque
- T_f is the total system friction torque

The acceleration torque is related to angular acceleration and system inertia by :

$$T_a = (J_m + J_{oe} + J_L) a$$

where :

- J_m is the moment of inertia of the motor
- J_{oe} is the moment of inertia of the encoder
- J_L is the moment of inertia of the load
- a is the angular acceleration

In a system of this type the friction torque T_f is normally very small and can be neglected. Therefore, combining these two expressions we can find the angular acceleration from :

$$a = \frac{K_T}{J_m + J_{oe} + J_L} \cdot I_m$$

It follows that for a given motor type and control loop the acceleration can only be increased by increasing the motor current, I_m .

The characteristics of a typical motor are given in figure 17. From this table we can see that :

$$K_T = 4.3 \text{ N cm/A} \quad (6.07 \text{ oz. in/A})$$

$$J_m = 65 \text{ g} \cdot \text{cm}^2 \quad (0.92 \times 10^{-3} \text{ oz. in}^2)$$

We also know that the maximum current supplied by the L292 is 2 A and that the moment of inertia of the STRE 1601 optical encoder, J_{oe} , is $0.3 \times 10^{-4} \text{ oz. in}^2$.

The moment of inertia of the load J_L , is unknown but assume, for example, that $J_{oe} + J_L \approx 2 J_m$. Therefore the maximum angular acceleration is :

$$a = \frac{6.07 \times 2}{2 \times 0.92 \times 10^{-3}} = 6597.8 \text{ rad/s}^2$$

Fig. 17 - The Characteristics of a Typical DC Motor.

Motor - Parameter	Value
$U_{BB} (V_s)$	18 V
C. emf. K_E	4.5 mV/min ⁻¹
N_o (without load)	3800 rpm
I_{om} (without load)	190 mA
T_f (friction torque)	0.7 N cm
K_T (motor constant)	4.3 N cm/A
Amature Moment of Inertia	65 g. cm. ²
R_M of the Motor	5.4 Ω
L_M of the Motor	5.5 mH

MAXIMUM SPEED

The maximum speed can be found from :

$$V_{S \min} = 2 V_{CEsat} + R_S I_m + K_e \Omega + R_m I_m$$

where :

$E = K_e \Omega$ is the internally generated voltage (EMF)

K_e is the motor voltage constant

Ω is the rotation speed of the motor.

For example, if $V_{S \min} = 20 \text{ V}$

$$2 V_{CEsat} + R_S I_m = 5 \text{ V (from L292 datasheet)}$$

$$R_m I_m = 10.8 \text{ V (} R_m = 5.4 \Omega \text{)}$$

we obtain :

$$K_e \Omega (E) = 4.2 \text{ V}$$

and

$$\Omega = \frac{4.2 \text{ V}}{4.5 \text{ mV/min}^{-1}} = 933.3 \text{ rpm} = 97.74 \text{ rad/s}$$

The STRE1601 encoder has 200 tracks so this speed corresponds to :

$$V = \Omega \frac{200}{60} = 3111.1 \text{ tracks/s.}$$

The time taken to reach maximum speed from a standing start can be found from

$$\Delta t = \frac{\Omega}{a} = \frac{97.74 \text{ rad/s}}{6597.8 \text{ rad/s}^2} = 14.8 \text{ ms}$$

We can also express the acceleration in terms of tracks/s² :

$$K = \frac{V}{\Delta t} = \frac{3111.1 \text{ tracks/s}^2}{14.8 \text{ ms}} = 210209.5 \text{ tracks/s}^2$$

Therefore the number of tracks necessary to reach the maximum system speed for our example is :

$$p = \frac{V^2}{2K} = 23 \text{ tracks}$$

This information is particularly useful for the programmer who writes the control software.

SETTING THE MAXIMUM SPEED

The chosen maximum speed is obtained by setting the values of R6, R7, R8, R9, C4 and C6 (all shown on the application circuit, figure 12). This is how it's done :

The first step is to calculate R6 and R7, which define the DAC current reference. From the L291 datasheet we know that I_{ref} , the DA converter current reference, must be in the range 0.3mA to 1.2mA.

Choosing an I_{ref} of roughly 0.5mA, and knowing that V_{ref} (the L290s reference output) is typically 5V, it follows that :

$$R6 + R7 = \frac{V_{ref}}{I_{ref}} = 10k\Omega$$

Therefore we can choose $R6 = R7 = 4.7k\Omega$ (5% tolerance).

Substituting the minimum and maximum values of V_{ref} (from the L290 datasheet) and the resistance

variations we can now check that the variation of I_{ref} in the worst case is acceptable.

$$I_{ref \min} = \frac{V_{ref \min}}{(R6 + R7) \max} = 0.46 \text{ mA}$$

$$I_{ref \text{ typ}} = \frac{V_{ref \text{ (typ)}}}{4.7k + 4.7k} = 0.53 \text{ mA}$$

$$I_{ref \max} = \frac{V_{ref \max}}{(R6 + R7) \min} = 0.62 \text{ mA}$$

These values are within the 0.3mA to 1.2mA limits.

Now that the reference current is defined we can calculate values for R8 and R9 which define the tacho current at the summing point.

The full scale output current of pin 12 of the L291 (the D/A converter output) is :

$$I_o = 1.937 I_{ref}$$

which is typically 1.02mA.

The worst case output current is when I_{ref} is at a maximum (0.62mA) and the I_{out} error is maximum (+ 2 %) :

$$I_o = 0.62 \times 1.937 \times 1.02 = 1.22 \text{ mA}$$

This less than the 1.4 mA maximum value for I_{out} specified in the L291 datasheet.

Assuming that the maximum DC voltage at the TACHO output of the L290 (pin 4) is 7V (this is the tacho voltage generated at the maximum system speed), we can find the sum of R8 and R9 ;

$$R8 + R9 = \frac{V_{tacho \text{ DC}}}{I_o \text{ typ}} = \frac{7}{1.02} = 6.85k\Omega$$

Therefore we choose $R8 = 4.7k\Omega$ and a $5k\Omega$ trimmer for R9. R9 is used to adjust the maximum speed.

We can now calculate the ripple voltage and maximum tacho voltage :

$$V_{\text{ripple pp}} = \frac{\pi}{4} (\sqrt{2} - 1) V_{tacho \text{ DC}} \cong 2.3 V_{pp}$$

$$V_{tacho \text{ max}} = \frac{\pi}{4} \sqrt{2} V_{tacho \text{ DC}} \cong 7.8 V_p$$

This value is within the voltage swing of the tacho amplifier ($\pm 9V$) ; that means the choice of $V_{tacho\ DC} = 7V$ is correct.

At this point we know the values of R6, R7, R8 and R9. The maximum speed can now be set by choosing values for C4 and C6 which form the differentiation networks on the L290. These values depend on the number of tracks of the optical encoder. For the STRE1601 encoder the capacitor values can be found from figure 18. These curves show how the capacitor value is related to frequency (encoder rotation speed) for different tacho voltages and maximum speed. The example values are $V_{tacho\ DC} = 7V$ and maximum speed = 3111 tracks/sec therefore the value for C4 and C6 is 15nF.

The values of R4 and R5 must be 820Ω to minimize the offsets.

Figure 18 : C4 and C6 value versus rotation speed for various maximum tacho voltage values.

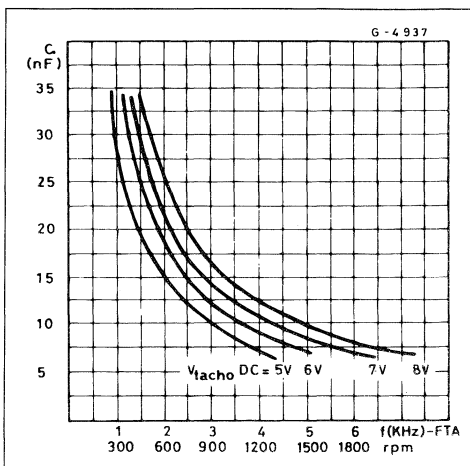
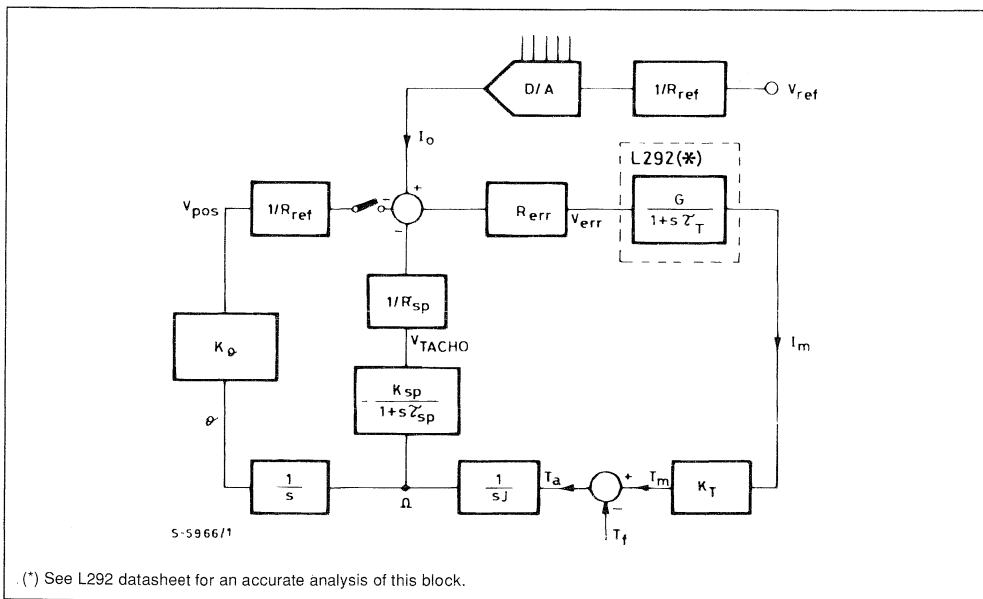


Figure 19.



(*) See L292 datasheet for an accurate analysis of this block.

List of terms

s : Laplace variable
 K_T : Motor torque constant
 T_a : Acceleration torque
 T_f : Total system friction torque
 J : Total moment of inertia ($J = J_{oe} + J_m + J_L$).

Ω : Speed
 θ : Angular position
 K_{sp} : Conversion factor that links the motor rotation speed and the TACHO signal.
 K_T : Conversion factor that links the motor position and the V_{pos} signal.

LAPLACE ANALYSIS OF THE SYSTEM

Table values for the components R11, R12, R13, R14 and C8 can be found from a Laplace analysis of the system. Figure 19 shows a simplified block diagram of the system which will be useful for the analysis.

The analysis is based on the angular speed Ω and on the motor position θ . The motor is represented, to a first approximation, by the current I_m and by the acceleration torque, T_a , which drives an inertial load J .

There are two conversion factors, K_{sp} and K_θ . They link the mechanical parameters (position and speed) with the equivalent feedback signals for the two loops. The values of K_{sp} and K_θ are determined by the encoder characteristics and the gain parameters of the integrated circuits. The openloop and closed-loop gains are fixed by four external resistors :

- R_{ref} – fixes the reference current ($R6 + R7$)
- R_{speed} – fixes the speed loop gain ($R8 + R9$)
- R_{pos} – controls the position loop gain ($R12$)
- R_{err} – controls the system loop gain ($R13$).

The stability both of the speed loop and of the speed-position loop are determined by external components.

The fundamental characteristics of the speed control system can thus be determined by the designer.

τ_{sp} is the time constant that determines the dominant pole of the speed loop and is determined by C8, R8 and R9

$$\tau_{sp} = C8 \frac{R8 R9}{R8 + R9}.$$

SETTING THE L292 COMPONENTS

The sensing resistor and feedback loop component values for the L292 can be calculated easily using the following formulae. A detailed Laplace analysis of this block is given on the L292 datasheet.

a) Sense resistors. $R_s = R18 = R19$

$$\frac{I_m}{V_i} = \frac{R2 R4}{R1 R3} \cdot \frac{I}{R_s}$$

$$\Rightarrow R_s = \frac{R2 R4 V_i}{I_m R1 R3}$$

(These resistors are all inside the L292).

where :

I_m is the motor current

V_i is the input voltage corresponding to I_m .

For example, $I_m = 2 \text{ A}$, $V_i = 9.1 \text{ V}$, resistor values as in figure 7 (L292 internal block diagram)

$$R_s = \frac{0.044}{I_m} \quad V_i = 0.2 \Omega$$

b) R17, R15, R16, C12, C13

$$G_{mo} = \frac{2 V_s}{R_m V_R}$$

V_s = L292 supply voltage

R_m = motor resistance

V_R = L292 reference voltage

and

$$\xi = \sqrt{\frac{R4 C13}{4 R15 C12 G_{mo} R_s}}$$

$R4$ = L292 internal resistor (400 Ω)

$R_s = R18 = R19$

A good choice for ξ is $1/\sqrt{2}$. Substituting this value, G_{mo} and the values of $R4$ and R_s :

$$\xi^2 = \frac{1}{2} = \frac{400 C13}{4 R15 C12 \times 0.2}$$

$$\Rightarrow \frac{1000 C13}{R15 C12} = 1$$

$$\text{Also } f_T = \frac{0.9}{2 \pi R15 C12}$$

Assuming that f_T is 3kHz, another recommended value :

$$R15 C12 \approx 47 \times 10^{-6} \text{ s}$$

Therefore we can find C13 :

$$1000 C13 \approx 47 \times 10^{-6}$$

$$\Rightarrow C13 = 47 \text{ nF}$$

Since

$$\frac{L_m}{R_m} = R17 C13$$

$$R17 = \frac{L_m}{C13 R_m}$$

For the example motor $L_m = 5 \text{ mH}$, $R_m = 5.4 \Omega$ therefore :

$$R17 = \frac{L_m}{C13 R_m} = 22 \text{ k}\Omega$$

From $R15 C12 \approx 47 \times 10^{-6} \text{ s}$, choosing a value of $R15$; 510 Ω , we have :

$$C12 = 82 \text{ nF}$$

Also, $R16 = R15 = 510 \Omega$.

DEAD TIME

C17 sets the switching delay of the L292 which protects against simultaneous conduction. The delay is :

$$\tau = R_{\tau} C17$$

and R_{τ} is an internal 1.5k resistor. The suggested 1.5nF value gives a switching delay of about 2.25 μ s. This is more than adequate because the transistors have a switch off delay of only 0.5 μ s.

SWITCHING FREQUENCY

The switching frequency is set by C17 and R20 :

$$f_{osc} = \frac{1}{2 R20 C17}$$

R20 must be at least 8.2k Ω and is varied to set the frequency : the value of C17 is imposed by dead time requirements. Typically the frequency will be 15-20kHz.

It should be outside the audio band to reduce noise but not too high or efficiency will be impaired. The maximum recommended value is 30kHz.

CURRENT RIPPLE

To reduce dissipation in the motor and the peak output current the ripple, ΔI_m , should be less than 10% of the maximum current.

Since

$$\Delta I_m = \frac{V_s}{L_m} \cdot \frac{T}{2}$$

($\frac{T}{2}$ = half period oscillator)

and

$$\Delta I_m = 0.1 I_{m \max}$$

$$0.1 I_{m \max} = \frac{V_s}{2 f L_{M \min}}$$

$$L_{M \min} = \frac{5 V_s}{f I_{m \max}}$$

Therefore there is a minimum inductance for the motor which may not always be satisfied. If this is the case, a series inductor should be added and the value is found from :

$$L_{\text{series}} = \frac{5 V_s}{f I_{m \max}} - L_M$$

EFFICIENCY AND POWER DISSIPATION

Neglecting the losses due to switching times and the dissipation due to the motor current, the efficiency of the L292's bridge can be found from :

$$\eta = 1 - \frac{\Delta t_1}{\Delta t_1 - \Delta t_2} \cdot \frac{V_{\text{sat}}}{V_s} - \frac{\Delta t_1}{\Delta t_1 - \Delta t_2} \cdot \frac{V_{\text{over}}}{V_s}$$

where :

$$V_{\text{over}} \equiv 2V (2V_{BE} + R_s I_m)$$

$$V_{\text{sat}} \equiv 4V (2V_{CE\text{sat}} + 3 V_{BE})$$

Δt_1 = transistor conduction period

Δt_2 = diode conduction period.

If $\Delta t_1 \geq \Delta t_2$ and $V_s = 20V$ we obtain :

$$\eta = 1 - \frac{4}{20} = 80\%$$

In practice the efficiency will be slightly lower as a results of dissipation in the signal processing circuit (about 1W at 20V) and the finite switching times (about 1W).

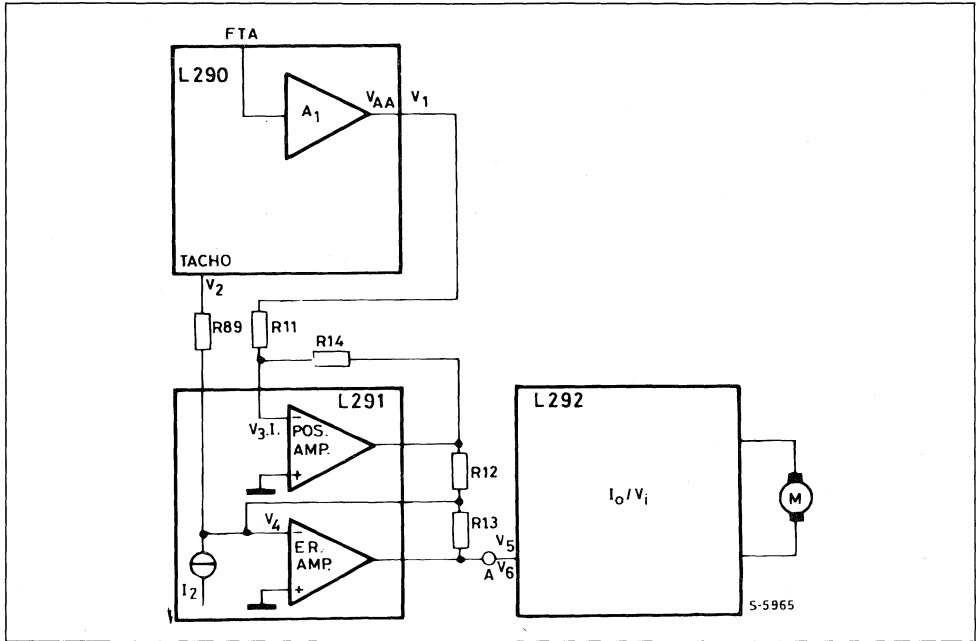
If the power transferred to the motor is 40W, the 80% efficiency implies 10W dissipated in the bridge and a total dissipation of 12W. This gives an actual efficiency of 77%. Since the L292's Multiwatt package can dissipate up to 20W it is possible to handle continuous powers in excess of 60W.

POSITION ACCURACY

The main feature of the system L290, L291, L292 is the accurate positioning of the motor. In this section we will analyse the influence of the offsets of the three ICs on the positioning precision.

When the system is working in position mode, the signal FTA coming from the optical encoder, after suitable amplification, is sent to the summing point of the error amplifier (L291). If there were no offset and no friction, the motor would stop in a position corresponding to the zero crossing of the signal FTA, and then at the exact position required. With a real system the motor stops in a position where FTA has such a value to compensate the offsets and the friction ; as a consequence there is a certain imprecision in the positioning. The block diagram, fig. 20, shows the parts of the 3 ICs involved in the offsets. First we will calculate the amount of the offsets at the input of the IC L292 (point A of fig. 20).

Figure 20.

**L290**

The offset of the TACHO signal, V2, is the main cause of the imprecision of the positioning. Another offset in L290 is V1, the output offset voltage of A1. The contribution at point A is :

$$V_{1A} = V1 \cdot \frac{R14}{R11} \cdot \frac{R13}{R12}$$

$$V_{2A} = V2 \cdot \frac{R13}{R89}$$

L291

In this IC there are the following offsets :

V3 = input offset voltage of the position amplifier

I1 = input bias current of the position amplifier

I2 = output offset current of the D/A converter plus ER. AMP bias current

V4 = input offset voltage of the error amplifier.

Their contribution at point A is :

$$V_{3A} = V3 \cdot \left(1 + \frac{R14}{R11}\right) \cdot \frac{R13}{R12}$$

$$V_{1A} = I1 \cdot R14 \cdot \frac{R13}{R12}$$

$$V_{2A} = I2 \cdot R13$$

$$V_{4A} = V4 \left(1 + \frac{R13}{R12/R89}\right)$$

L292

Referring to this IC we must consider the input offset voltage V5. Moreover, we call V6 the input voltage that must be applied to the L292 to keep the motor in rotation, i.e. to compensate the dynamic friction. V6 is not an offset voltage, but has the same effects, and for this reason we have to put it together with the offsets.

$$V_{5A} = V5 \cdot \frac{I_o}{V_i} = \text{Transconductance of L292}$$

$$V_{6A} = V6 = \frac{I6}{\left[\frac{I_o}{V_i}\right]}$$

I_6 = Motor current necessary to compensate the dynamic friction

The total offset voltage referred to point A is given by the sum of all the precedent terms :

$$V_A = V_{1A} + V_{2A} + V_{3A} + V_{I1A} + V_{I2A} + V_{4A} + V_{5A} + V_{6A}.$$

The amplitude of the signal FTA necessary to compensate the offset VA is :

$$V_{FTA} = V_A \cdot \frac{R_{12}}{R_{13}} \cdot \frac{R_{11}}{R_{14}} \cdot \frac{1}{A_1}$$

Calling V_M the maximum value of the signal FTA, the phase error of the system is :

$$\alpha = \sin^{-1} \frac{V_{FTA}}{V_M}$$

If α_c is the phase between two consecutive characters, (it may be equal 360° or multiple of it) the percentage error in the character positioning is :

$$\varepsilon = \frac{\alpha}{\alpha_c} \cdot 100$$

In these calculations we have not considered how the precision of the signal FTA, coming from the optical encoder, influences the positioning error. The percentage value of the pitch accuracy must be added to ε to have the total percentage error in the character positioning. Any DC offset of the mean value of the signal FTA must be multiplied by A_1 and added to V_1 to obtain its effect on the error.

NUMERICAL EXAMPLE

In this numerical example we will calculate the precision of the positioning in the worst case, i.e. with all the offsets at the max value. The values of the external components are taken from the application circuit. (fig. 12).

$$R_{11} = 22K \quad R_{12} = 100K \quad R_{13} = 120K \quad R_{14} = 15K \\ R_{89} = R_8 + R_9 = 6K$$

From the data sheets of the three ICs we can find :

$$V_1 = 55mV \quad V_2 = 80mV \quad V_3 = 4.5mV$$

$$V_4 = 2mV \quad V_5 = 350mV$$

$$I_1 = 0.3\mu A \quad I_2 = 0.4\mu A$$

$$A_1 \text{ min} = 22dB = 12.6$$

$$\frac{I_0}{V_i} \text{ min} = 205 \quad \frac{mA}{V}$$

$$V_{Mmin} = 0.4 V$$

For I_6 we will consider the value $I_6 = 50mA$

$$V_{1A} = 55 \cdot 10^{-3} \cdot \frac{15}{22} \cdot \frac{120}{100} = 45mV$$

$$V_{2A} = 80 \cdot 10^{-3} \cdot \frac{120}{6} = 1.6V$$

$$V_{3A} = 4.5 \cdot 10^{-3} \left(1 + \frac{15}{22} \right) \cdot \frac{120}{100} = 9.1mV$$

$$V_{I1A} = 0.3 \cdot 10^{-6} \cdot 15 \cdot 10^3 \cdot \frac{120}{100} = 5.4mV$$

$$V_{I2A} = 0.4 \cdot 10^{-6} \cdot 120 \cdot 10^3 = 48mV$$

$$V_{4A} = 2 \cdot 10^{-3} \cdot \left(1 + \frac{120}{5.6} \right) = 44.9mV$$

$$V_{5A} = 350mV$$

$$V_{6A} = \frac{50}{205} = 244mV$$

$$V_A = 2.346V$$

$$V_{FTA} = 2.329 \cdot \frac{100}{120} \cdot \frac{22}{15} \cdot \frac{1}{12.6} = 0.228V$$

$$\alpha = \sin^{-1} \frac{0.226}{0.4} \cong 35^\circ$$

If we consider an optical encoder with 200 tracks/turn and a daisy wheel with 100 characters, the phase between two consecutive characters is $\alpha_c = 720^\circ$, and then the maximum percentage error we can have is.

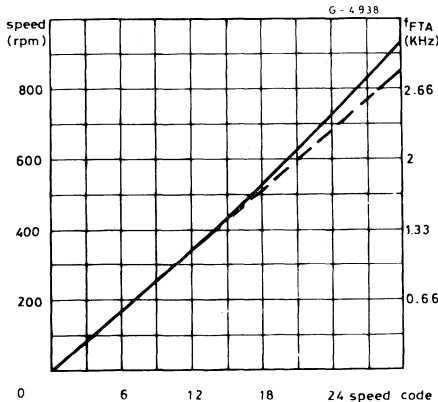
$$\varepsilon = \frac{35}{720} \cdot 100 \cong 4.8\%$$

From this numerical example we can see that the main contribution to the positioning error is given by the offset of the TACHO signal (V_{2A}), other big contributions are given by the input offset voltage of L292 (V_{5A}) and by the voltage necessary to compensate the dynamic friction of the motor (V_{6A}). This last term is only determined by the motor and can also have greater values.

The error we have calculated is the maximum possible and it happens when all the offsets have the max value with the same sign, i.e. with a probability given by the product of the single probabilities. Considering as an example every offset has a probability of 1% to assume the max value, the probability the error assumes the max value is :

$$P = (10^{-2})^7 = 10^{-14}$$

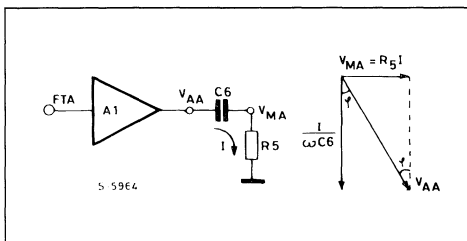
Figure 21.



SPEED ACCURACY

If we consider the complete system with L290-L291-L292 driving a DC MOTOR with optical encoder, we can note the speed of the motor is not a linear function of the speed digital code applied to L291. The diagram of fig. 21 shows this function and it is evident that the speed increases more than a linear function, i.e. if the speed code doubles, the speed of the motor becomes more than the double. The cause of this non linearity is the differentiator network R4 C4 and R5 C6 (see fig. 22) that has not an ideal behaviour at every frequency.

Figure 22.



$$1) V_{MA} = V_{AA} \sin \varphi$$

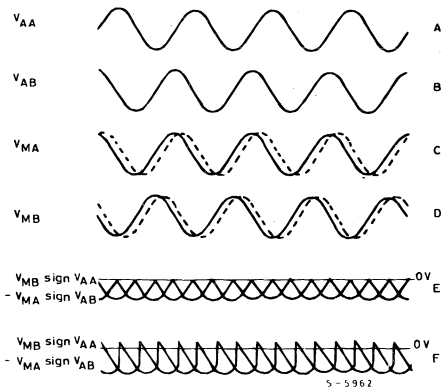
$$\varphi = \text{tg}^{-1} \quad \omega R5 C6 \quad \omega = 2 \pi f$$

$$2) V_{MA} = V_{AA} \sin \text{tg}^{-1} \omega R5 C6$$

f = frequency of the signal FTA

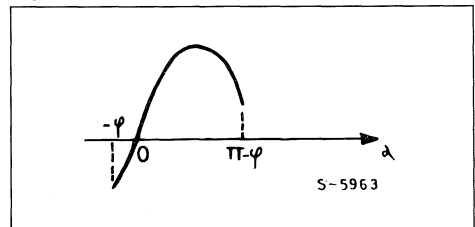
This last relation gives the amplitude of the signal V_{MA} ; it is evident there is not a linear function between V_{MA} and ω , like $V_{MA} = K\omega$ and the difference is greater if the product $\omega R5 C6$ doesn't respect the disequation $\omega R5 C6 \ll 1$, i.e. at high frequencies.

Figure 23.



The phase angle between V_{MA} and V_{AA} should be 90° and then $\varphi = 0$, in our case φ increases with the frequency according to the equation $\varphi = \text{tg}^{-1} \omega R5 C6$, and influences the amplitude of the output signal TACHO. In fig. 23 are shown the waveforms that contribute to generate the TACHO signal. A and B are the signals V_{AA} and V_{AB} in phase with the input signals FTA and FTB. C and D are the signals V_{MA} and V_{MB} : the continue line indicate the ideal case, in fact the phase between V_{MA} and V_{AA} is 90° ; the dotted line is referred to the real case in which the phase is lower than 90° . By adding the two signals shown in E we obtain the TACHO signal, whose expression is:

Figure 24.



$$V_{TACHO} = V_{MB} \cdot \text{sign } V_{AA} - V_{MA} \cdot \text{sign } V_{AB}$$

The signals in E are referred to the ideal case, the ones in F to the real case. It is possible to demonstrate the mean value of the TACHO signal in the real case is lower than the one we could have with an ideal differentiator network and this explains why in fig. 21 the speed of the motor increases more than a linear function. The mean value of the waveforms F is (fig. 24).

$$3) V_m = \int_{-\varphi}^{\pi-\varphi} K1 \sin \alpha d\alpha = \frac{2K1}{\pi} \cos \varphi$$

Since the waveforms E are half sinewaves, the mean value is

$$4) V_m = \frac{2 K1}{\pi}$$

We can conclude that two causes contribute to give a TACHO signal lower than the theoretical one, both due to differentiator network :

a) the amplitude of the signal V_{MA} is lower than $V_{MA} = K\omega$ and we can call ϵ_1 the relative percentage error.

$$\epsilon_1 = \frac{\sin \text{tg}^{-1} \omega R5 C6 - \omega R5 C6}{\omega R5 C6} \cdot 100$$

b) the mean value of the signals V_{MA} . sign V_{AB} and V_{MB} . sign V_{AA} is lower than the theoretical one because there is a shift in the phase of the signals V_{MA} and V_{MB} . The relative percentage error only due to the shift of the phase is

$$\epsilon_2 = (\cos \varphi - 1) \cdot 100 \quad \varphi = \text{tg}^{-1} \omega R5 C6$$

The total percentage decrease of the TACHO signal is given with a good approximation by the sum of ϵ_1 and ϵ_2 .

Example :

Consider :

$f = 3000\text{Hz}$ corresponding to

$$n = \frac{3000}{200} \cdot 60 = 900\text{rpm of the motor if } 200 \text{ are the tracks/turn of the encoder}$$

$$\epsilon_1 \approx -2.6\% \text{ with } R5 = 820\Omega$$

$$C6 = 15\text{nF}$$

$$\epsilon_2 \approx -2.6\%$$

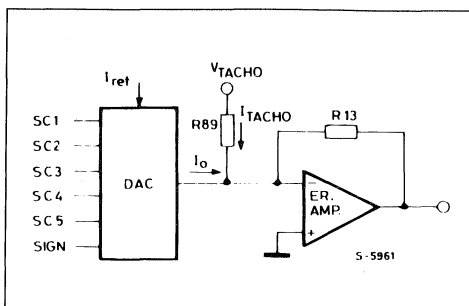
$$\epsilon_3 \approx \epsilon_1 + \epsilon_2 \approx -5.2\%$$

From the diagram of fig. 21 we note that at a speed of 900 rpm corresponds a theoretical speed of 855rpm with a percentage difference of about 5.2%.

SPEED ACCURACY DUE TO THE D/A CONVERTER

To analyse the influence of the DAC precision on the speed accuracy we will refer to the following (fig. 25).

Figure 25.



The value of the output current of the DAC I_o depends on I_{ref} and on the digital code defined by the inputs SC1-SC5, while its direction depends on the value of the SIGN input, the max theoretical value of I_o , obtained with SC1-SC5 low is :

$$I_{OM} = \pm \frac{31}{16} I_{ref}$$

The motor will run at a speed corresponding to the following value of the TACHO signal :

$$V_{TACHO} = - I_{OM} \cdot R89 = \pm \frac{31}{16} I_{ref} \cdot R89$$

This last relation is true if we don't consider the motor friction and the offsets. Consider now the possible friction and the offsets. Consider now the possible spreads we can have in the motor speed due to the DAC. If we call I_{OM1} the value of the max output current I_o corresponding to the SIGN LOW and I_{OM2} the one corresponding to the SIGN HIGH, the percentage error we have in the max speed from the positive to the negative value is :

$$\epsilon_4 = \frac{I_{OM1} + I_{OM2}}{I_{OM}} \cdot 100$$

Note that we have consider the sum of I_{OM1} and I_{OM2} because they have opposite signs. This kind of error is principally due to a different gain of the DAC between the two conditions of the SIGN LOW and HIGH. An equal difference of I_{OM1} and I_{OM2} , from I_{OM} ($|I_{OM1}| - |I_{OM}| = |I_{OM2}| - |I_{OM}|$) doesn't constitute a speed error because this shift from the theoretical value can be compensated by adjusting the resistor R89 that is formed by a fixed resistor in series with a potentiometer.

With the guaranteed values on the L291 data sheet we can calculate for ϵ_4 the max value :

$$\epsilon_4 = \frac{21 \mu\text{A}}{1.4 \text{ mA}} \cdot 100 = 1.5 \%$$

Another characteristic of a D/AC is the linearity, that in our case is better than $\pm 1/2$ LSB. This value is sufficient to guarantee the monotonicity of I_o , and then of the speed of the motor, as a function of the input digital code. The precision of $\pm 1/2$ LSB implies a spread of the speed at every configuration of the input code of $\pm 1.61\%$ referred to the maximum speed. The max percentage error we can have is then greater at low level speed ($\pm 50\%$ at min speed) and has its minimum value at the maximum speed (1.61%).

ACCURACY DUE TO THE ENCODER

The amplitude of the signals FTA and FTB determines the value of the TACHO signal. This amplitude must be constant on the whole range of the frequency, otherwise it is not possible to have a linear function between the TACHO signal and the frequency. The spread of the amplitudes of the two signals FTA and FTB between several encoders can be compensated by adjusting the potentiometer R9 (see fig. 12). The phase between the two signals should be 90° . If there is a constant difference from this value, a constant factor reduction of the TACHO signal results that can be compensated with the potentiometer R9. If the difference from 90° is random, also the reduction of the TACHO signal is random in the same way, and by means of R9 it is possible to compensate only the mean value of that reduction.

MICROCONTROLLER BASED UNIVERSAL MOTOR SPEED CONTROL

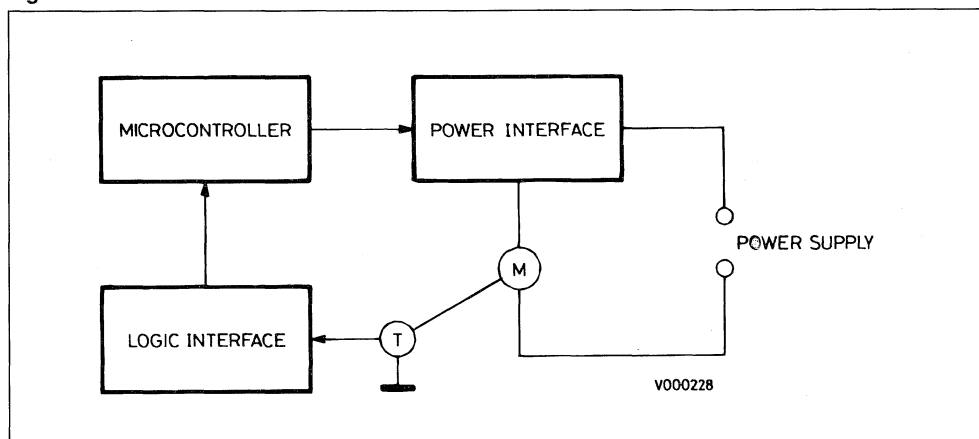
DESCRIPTION

Many appliance applications include universal motor speed control. The use of a low cost microcontroller instead of an analog motor control device is a versatile solution allowing easy control of motor speed and the possibility of managing other functions of the applications. The purpose of this note is to explain how to implement efficient speed regulation by optimizing the resources of SGS-THOMSON Microelectronics ST6 microcontrollers Family.

REGULATION PRINCIPLE

The microcontroller must provide the motor with a controlled power supply in order to keep its rotation speed as constant as possible. The motor main shaft is coupled with a tacho generator which informs the microcontroller of the real motor speed. The regulation loop can be summarized by the synoptic in figure 1.

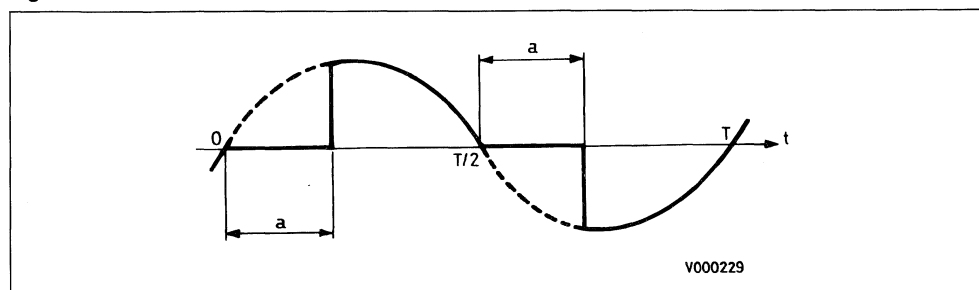
Figure 1 .



In this note we will consider the case in which the power supply is the AC mains and the power interface is a triac. The microcontroller controls the

power delivered to the motor by modulating the firing angle of the triac (see figure 2).

Figure 2 .



The voltage applied to the motor is :

$$V = \sqrt{\frac{2}{T} \int_a^{1/2} V_{\max}^2 \cdot \sin^2(wt) \cdot dt}$$

The delay is generated by software and obtained after a calculation depending on the difference between the desired speed and the real motor speed. This implies that the microcontroller must manage three main functions :

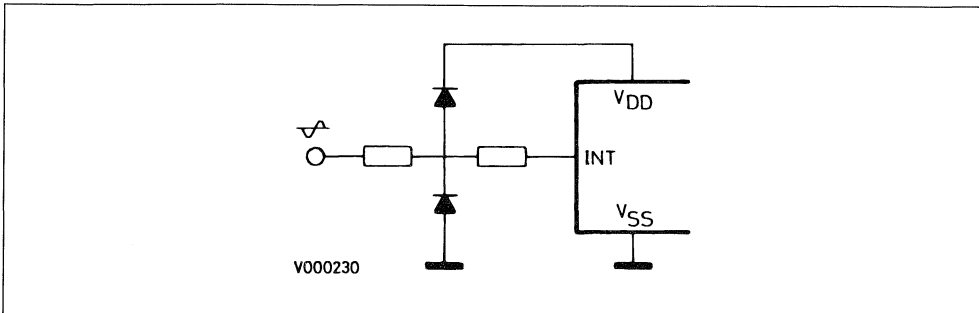
- motor speed measurement
- firing angle calculation

- AC synchronization and triac firing

AC MAINS SYNCHRONIZATION AND TRIAC FIRING

The best way to synchronize the microcontroller with the AC mains and to be sure that it will remain synchronized is to apply the AC mains voltage through a logic interface to an interrupt input of the microcontroller, as shown in figure 3.

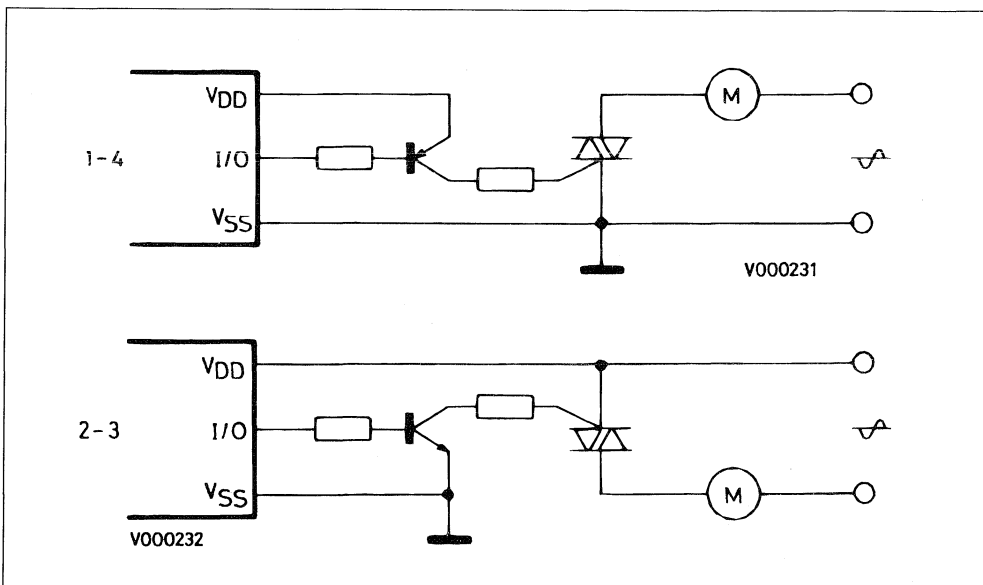
Figure 3 .



In this way, each interrupt will be the starting event for internal generation of the temporization corresponding to the firing angle. After this temporization,

it is easy to toggle a port in order to command the triac gate for about 50µs.

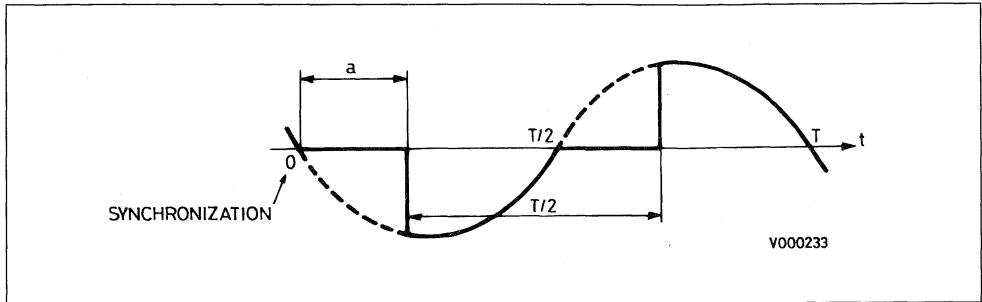
Figure 4 : Block Diagram for Triac Drive in Cadrans.



Very often, the microcontrollers' interrupt inputs are activated on falling edges only. In this case, synchronization will be done every AC mains period instead of each AC mains half period. That means that

the temporization for the first firing pulse can be applied from the interrupt event, and the second pulse will be fired one-half period after the first (figure 5).

Figure 5.



TIMING GENERATION

The best way is to use the internal timer of the microcontroller. If the microcontroller does not have timers, all the software would have to be calibrated in time. We will suppose here that the timer decrements to 0.

When the AC mains synchronization is detected, the Timer must be initialised with the value ANG , where $a = ANG \cdot t_T$ (t_T = timer clock period), and started. When the timer decrements to 00, the triac must be switched on and the timer reloaded with the value $DELAY$ resulting from $T/2 = DELAY \cdot t_T$. After this second temporization the triac is switched on again on the next AC mains half period. The timer may be reloaded with the $DELAY$ value, but, in all cases, it will be re-initialized to the ANG value with the next AC mains synchronization.

If the timer generates an interrupt to the CPU when it reaches 00, the end of temporization is easy to detect and the microcontroller can manage other tasks when a temporization is running. Otherwise, the CPU must continuously look into the timer contents in order to detect the moment when it reaches 00. Note that all the CPU calculations must be made at definite times, for instance, after the first triac pulse during a time shorter than the $DELAY$ time.

The timer clock should be chosen in order to cover the $T/2$ delay : e.g., for an 8-bit timer and a 50Hz AC mains, t_T must be higher than $10\text{ms}/255 = 39,2\mu\text{s}$. This can be done by adjusting the prescaler value (if there is one) or by changing the MCU clock. All ST6 devices offer at least one 8-bit Timer with 7-bit programmable prescaler and interrupt generation at 00 decrement.

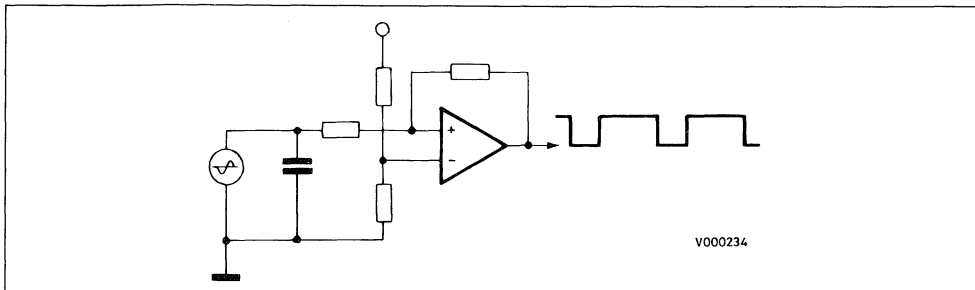
MOTOR SPEED MEASUREMENT

The speed information is given by a tacho generator integral with the main shaft. The tacho generator provides a signal whose frequency changes in relation with rotation speed according to the formula : $f = p\Omega$, where f = tacho signal frequency, p = num-

ber of tacho pairs of poles and Ω = speed in rotation per second.

The signal delivered by the tacho must be interfaced with the microcontroller in order to be monitored, as described in figure 6.

Figure 6.

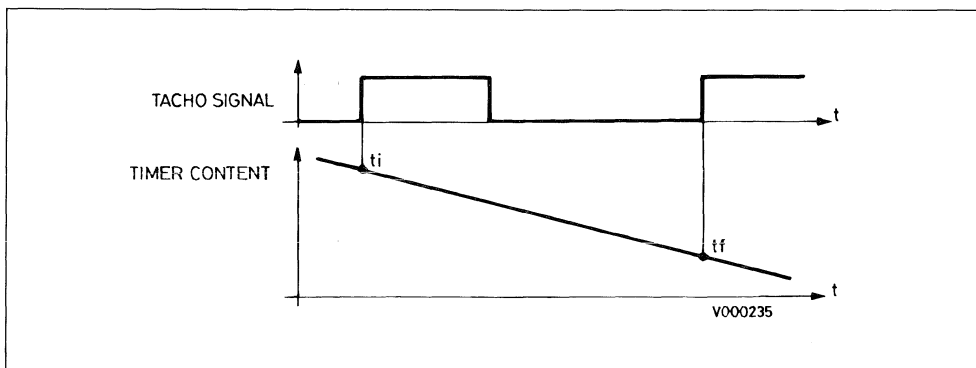


Signal period : $T = 1/(p\Omega)$ where Ω is rotation per second or $60/(p\Omega)$ where Ω is R.P.M.

As the signal is not half duty cycle type, the microcontroller must measure its period (not only the half period). If a second timer is available, the measure can be made with it ; otherwise the timer, used for triac firing, may also be used for period measurement.

The measure is started on the first edge appearing on the input : the initial timer value (t_i) is stored (MES). The measurement is stopped at the end of a tacho period ; the timer value (t_f) is then subtracted from the initial value $MES = MES - t_f$. MES is the image of the tacho period ($MES \cdot t_r$) : $MES = 60/(p \cdot \Omega \cdot t_r)$, (see figure 7).

Figure 7.



Examples : with $t_r = 40\mu s$ and $p = 8$ pairs of poles

500 RPM $\rightarrow$ tacho period = 15ms $\rightarrow$ MES = $60/(8 \times 500 \times 40\mu s) = 375$ timer counts.

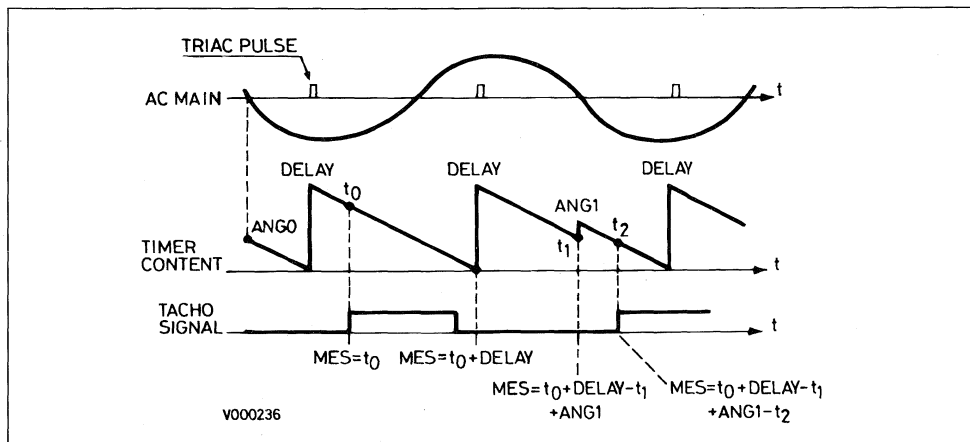
1000 RPM $\rightarrow$ tacho period = 7.5ms $\rightarrow$ MES = 187 timer counts.

10000 RPM $\rightarrow$ tacho period = 0.75ms $\rightarrow$ MES = 19 timer counts.

As shown in the examples, the tacho period may be long and the timer may reach 00 before the end of the measurement. So each time the timer reaches 00, the different values of the timer must be added

together. It should be noted that each timer access may involve an error on the tacho measurement as it can occur synchronously with the measurement end (see figure 8).

Figure 8.



Of course, if the tacho period is short enough, the measure should be started after the timer has been loaded with the DELAY value, to avoid its decrement 00. It must be taken into account that the measure really begins after the first edge on the tacho signal :

the waiting time must be taken into account to evaluate the global measurement time (see figure 9). An example of a tacho measurement flowchart is shown in figure 10, 11 and 12.

Figure 9.

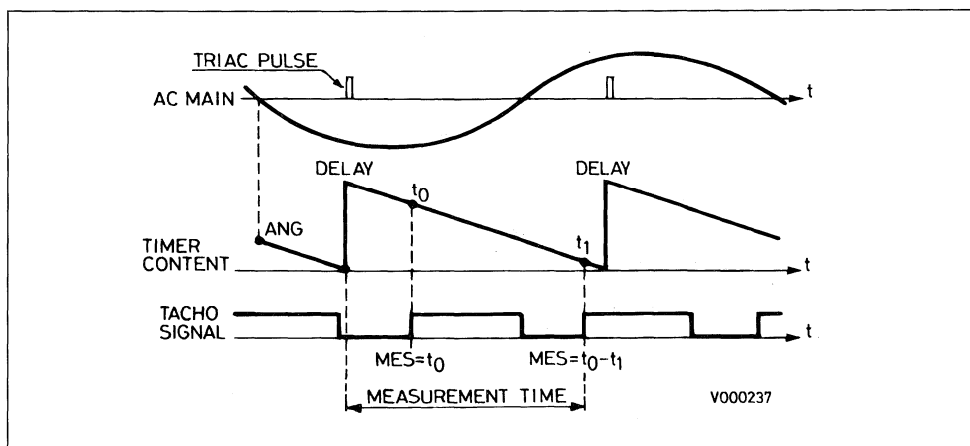
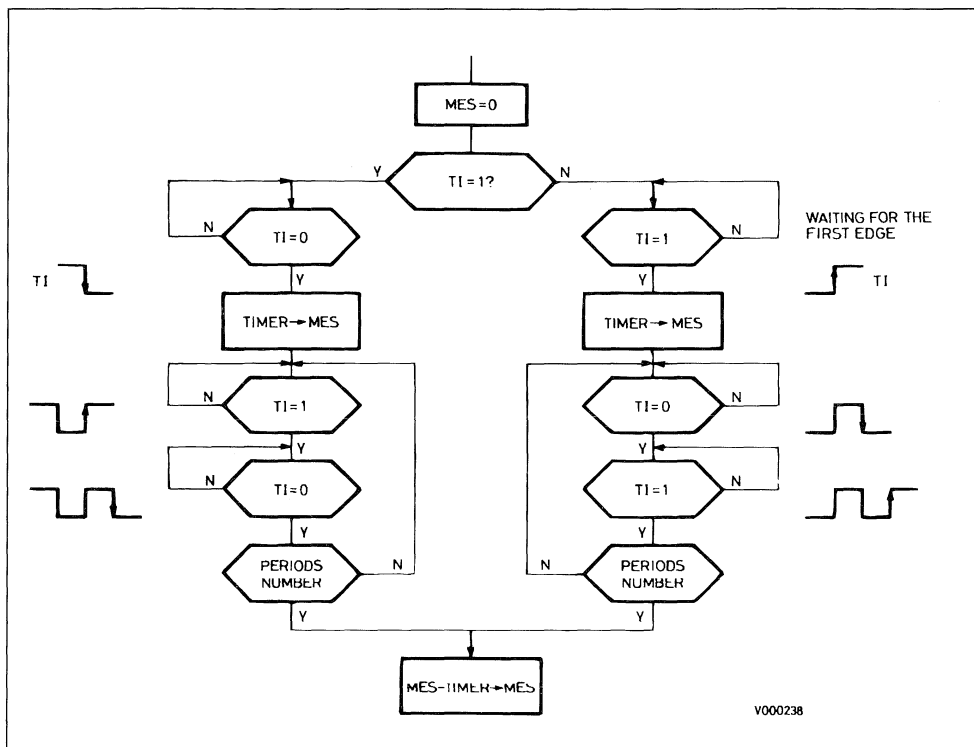
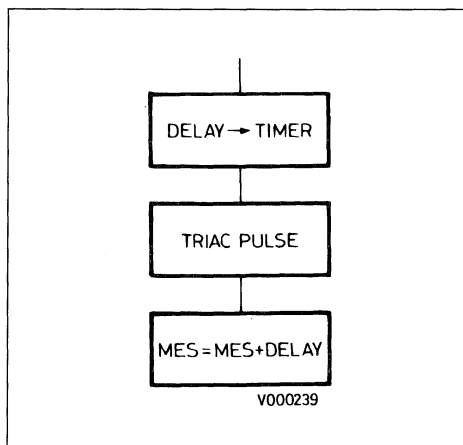


Figure 10 : Measurement Routine Example.



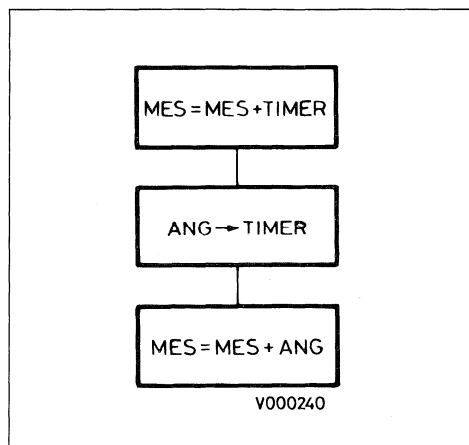
Note : N = Number of periods to be measured.
TI = Tacho Input.

Figure 11 : Timer Subroutine Example.



Note : Called when timer reaches 00.

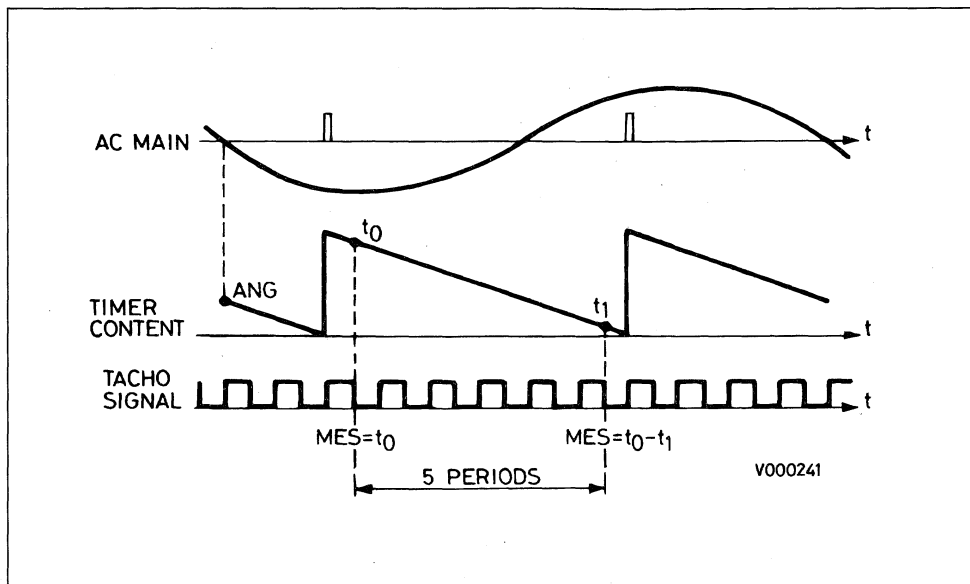
Figure 12 : Synchronization Subroutine Example.



If the tacho signal period is too short, the number of timer samples will not be significant (in the above example, only 19 timer counts for a 10000RPM motor speed). In this case, it is better to measure

several tacho periods. The number of measured tacho periods must be continuously increased over the entire speed range in order to keep the accuracy as constant as possible (see figure 13).

Figure 13.



FIRING ANGLE CALCULATION

The firing angle value will be calculated depending on the error between the desired motor speed and the real measured speed. If the real speed is lower than the desired speed, the firing angle must be reduced (more conduction). On the contrary if the real speed is higher than the speed desired, the firing angle must be increased (less conduction).

Of course, the desired speed is programmed in the microcontroller, in the same way as real speed is measured, i.e. $SPEED = 60 / (p \cdot \Omega \cdot \tau)$. It is then easy for the microcontroller to calculate the error between desired and real speed by calculating the difference between the two speeds. Knowing this error and its sign, it is possible to apply three kinds of actions on the firing angle :

PROPORTIONAL CORRECTION

The correction applied to the firing angle is proportional to the speed error and is added to or sub-

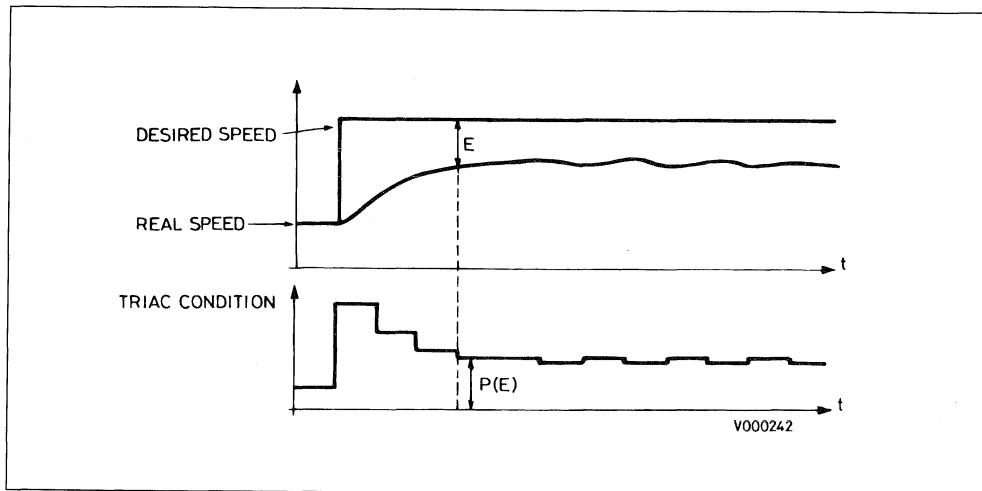
tracted from the average constant firing angle $ANG0$. There is no memorisation of the evolution of the firing angle : the firing angle at "t" time only depends on the error at "t" time. A simple way to calculate the correction is to use the error as a pointer on a look-up table containing the correction coefficients. Furthermore, the coefficients of the table may be adjusted allowing a non linear response curve.

E.g. : $ANG0 = 125$ (5ms/40 μ s) ; desired speed = 500 RPM $\rightarrow$ SPEED = 375 ; Measured speed MES = 370, i.e. 507 RPM.

Error = $375 - 370 = +5$: the real speed is too high : the firing angle must be increased. 5th coeff. of the look-up table = 10 : the firing angle applied on the next AC mains period will be 135 (5.4ms).

Example of response of a proportional correction to a speed step is shown in figure 14.

Figure 14.



As the figure 14 shows, there will always be a gap between the real speed and the desired speed : this is called static error. A solution to reduce (but not suppress) this gap, could be the increase of the gain loop (more correction for the same error). But in this case, the system will be sensitive to any small speed change and a lot of current spikes will be generated (reducing the motor life) and there will be a risk of creating an instability in the loop, implying an oscillation of the system.

INTEGRAL CORRECTION.

To suppress the static error, an integral correction can be applied. Instead of implementing a correction on a constant average firing angle base, the integral correction will change the base for the next

calculation. There is a memorisation of the average firing angle ANG0 which evolves depending on the successive speed errors.

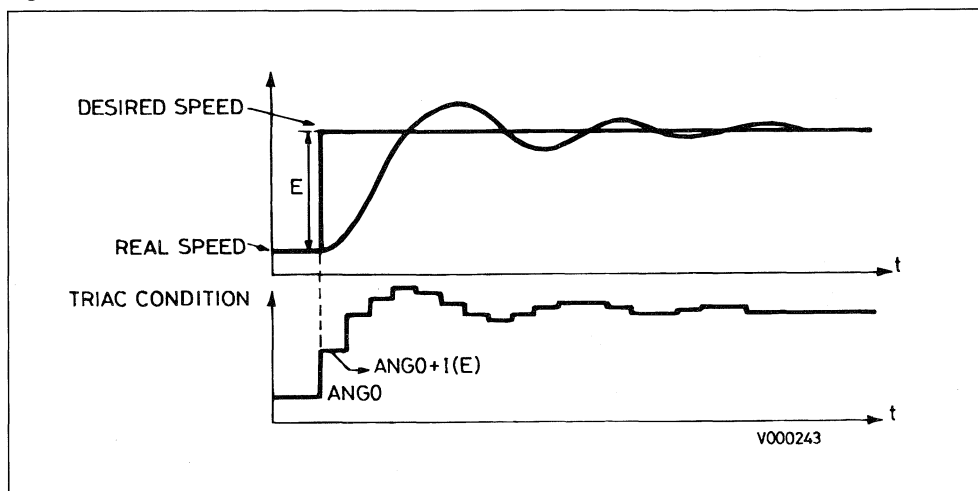
$$ANG0(t) = ANG0(t-1) \pm I(E(t)) = \sum_{n=0}^t I(E(n))$$

where $I(E(t))$ is the integral correction depending on the error E measured at time "t". As described before, a simple way of calculating the correction is to use the error as a look-up table pointer.

E.g. : ANG0 = 125 ; desired speed = 500RPM →
SPEED = 375 ; measured speed = 370 i.e. 507 RPM.

error = 375 - 370 = +5 ; 5th table coefficient = 3 ;
the new firing angle will be 128 and will be the base of calculation for the next correction.

Figure 15.



In this case, static error has been suppressed, but the system takes more time to stabilise to a constant speed. Response time can be improved by combining both proportional and integral correction. The firing angle calculation becomes :

$$ANG(t) = ANG0(t) \pm P(E(t)) \text{ with } ANG0(t) = ANG0(t-1)I(E(t)).$$

Proportional correction can be lower than before to avoid current spikes and instability. The firing angle will evolve "continuously" and with regularity. The integral corrections should also not be too high, otherwise the response time of the loop will be shorter, and the loop would have a tendency to oscillate.

To avoid instability, the look-up tables can be reduced to few values (for instance 15). This way, the gain of the loop is saturated even if the error is big. The Proportional-Integral regulations are often sufficient for slow devices tolerating pseudo-oscillations before stabilisation (washing-machines for instance).

DIFFERENTIAL CORRECTION

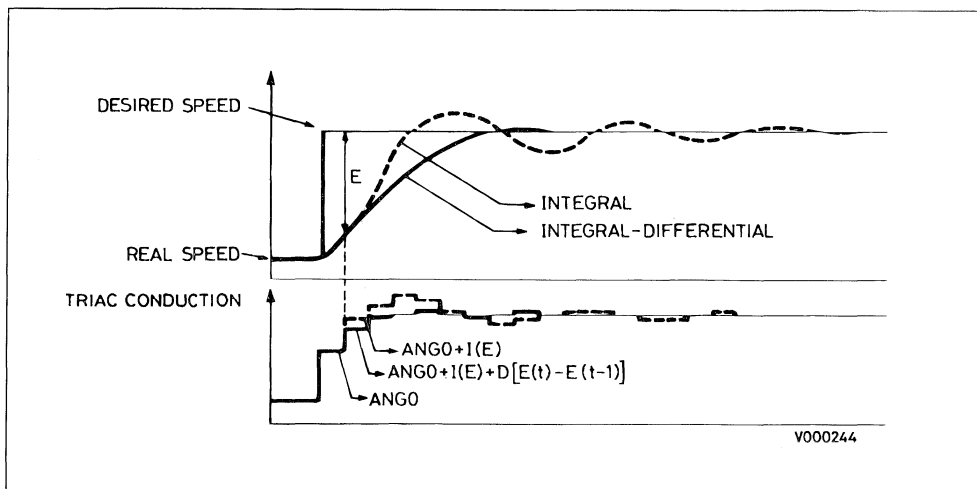
To improve the stability of the system, a third correction, the differential correction, can be added in relation to the slope of the error. This correction acts

on the firing angle by anticipating the evolution of the error between desired and real motor speed. The correction, as in the previous cases, will be in a look-up table addressed by the difference between the current error and the previous one, i.e., $\text{correction} = D(E(t) - E(t-1))$.

This correction is not effective when the speed remains stable ; the differential action will accentuate the correction if the difference between real and desired speed is increasing and will slow down the correction the faster the real speed approaches the desired speed.

E.g. : desired speed = 500 RPM $\rightarrow$ SPEED + 375.
Previous measurement = 385, i.e. 487 RPM : the real speed was lower than the desired one. Let's suppose $ANG0 = 120$. Current measurement = 378, i.e. 496 RPM : that means that the real speed approaches the desired speed. The current error is -3, the previous one was -10 ; differential error = +7 ; 7th differential table coefficient = 2 ; 3rd integral table coefficient = 3. The next firing angle will be : $ANG0 - 3 + 2 = ANG0 - 1 = 119$, whereas only with the integral correction the next firing angle would have been $ANG0 - 3 = 117$. The differential action permits reducing the overshoot.

Figure 16.



The evolution of the error is anticipated and corrected : the gain of the loop can be increased without reducing the to instability of the system.

The resulting firing angle becomes :

$$ANG = ANG0(t) \pm P(E(t)) \text{ with } ANG0(t) = ANG0(t-1) \pm I(E(t)) \pm D(E(t)) - E(t-1))$$

In order to improve the response time of the system to a step of speed, it is possible to suppress the differential correction as long as the error is important and then to apply again the differential correction when the error is smaller in order to help the system to stabilize better.

GENERAL REMARKS ON LOOP CORRECTIONS

Of course, we can not give here the values that must be put in the different look-up tables. Those values depend on the transfer function of the loop, and they must be adjusted to the regulated system, depending on whether the user wants to improve the precision of regulated speed or to improve the average current in the motor.

It must be noted that the gain of the different corrections is not necessarily constant with the error : it can be easily adjusted in the look-up tables. What is more, it is possible to change error influence all

over the speed range in order to adjust the gain to the system characteristics. For instance, the measurement produces a lot of samples : even a low speed error will involve a lot of digital error samples : in this case, the error should be divided before pointing to the look-up tables. This is more efficient when the motor inertia is lower in low speeds : the correction must be more gradual. On the contrary, in high speeds, the measurement samples are fewer and the motor inertia is higher : the correction must be stronger, the error must not be divided before pointing to the tables (it is also the reason why several periods of the tachometer signal must be measured instead of only one).

One disadvantage of a numeric regulation may be the sampling error : the first parameter is that the value obtained after measurement may be ± 1 bit plus the measurement errors. To limit measurement errors, the number of samples must be increased (more consecutive periods measured, especially in high speed) and the measurement should never be interrupted by other events : that is why it is preferred to do the measurement after the AC mains synchronization and between the two triac firing pulses (of course, this is not always possible in low speeds).

The second parameter is the minimum step of correction that cannot be less than 1 bit. For regulations needing a current in the motor without spikes, it will be necessary, for instance, to put zeroes in the first coefficients of the integral table because a correction of one step will involve too high speed and current change. This means that a speed error will remain in this case. In order to increase accuracy without increasing the number of bits available for the triac firing angle, it is possible to work on firing angle ANG1 - four times higher (for instance) than the normal angle ANG0 - to apply the correction on ANG1 and then to divide ANG1 by 4 in order to obtain the firing angle that must be applied to the triac. E.g. : ANG0 = 100

Integral look-up table without the use of ANG1 :
0-0-0-0-1-1-2-2-3...

If the error between real and desired speed is in the range -3 to +3, no correction will be applied to the firing angle. For instance, the error can remain at +1.

Integral look-up table with the use of ANG1 :
0-1-2-3-4-6-8-10-12...

Let's assume that the error between real and desired speed is always + 1. In this case, the first time ANG1 becomes 101, but ANG0 = ANG1/4 remain at 100 ; second time ANG1 = 402, ANG0 = 100 ; third time ANG1 = 403, ANG0 = 100 ; fourth time ANG1 = 404; ANG0 = 101 ; as the error remained at +1 four consecutive times a correction is applied to the firing angle to reduce this error. This correction includes a time criteria and is more gradual and more accurate than the previous one (of course, the gain of the integral table remains the same).

CONCLUSION

The aim of this note was to point out the different parameters involved in numeric motor speed control, and to show how to manage them in order to perform efficient regulation. Of course, the different parameters of the tables must be determined by the user to fit into the regulated system. But, in all cases, it is certain that the use of a microcontroller will be a versatile and low cost solution.

AN ECONOMIC MOTOR DRIVE WITH VERY FEW COMPONENTS

INTRODUCTION

The main objectives of this design are the economy and circuit simplicity which enable costs to be reduced to a minimum. For this reason the design is particularly suitable for domestic appliances powered by the 220 V AC mains. In this area, characteristics such as low cost, simplicity (and consequently greater reliability) have priority.

With these objectives the choice of the power switch is very important because the complexity of the drive circuit, the number and the power of the auxiliary supplies and the protection networks, depend on its characteristics. These factors lead to the decision to use a HIMOS device (an IGBT) as a power switch. The main characteristics of a HIMOS device are that:

- It switches high current with very low ON resistance, similar to a BJT (bipolar junction transistor).
- It is very rugged and has very large safe operating areas similar to Power MOSFETs.
- It has high overload current capability.
- It is easy to drive (like Power MOSFETs) consequently it is possible to drive it directly by means of popular linear IC.

quently it is possible to drive it directly by means of popular linear IC.

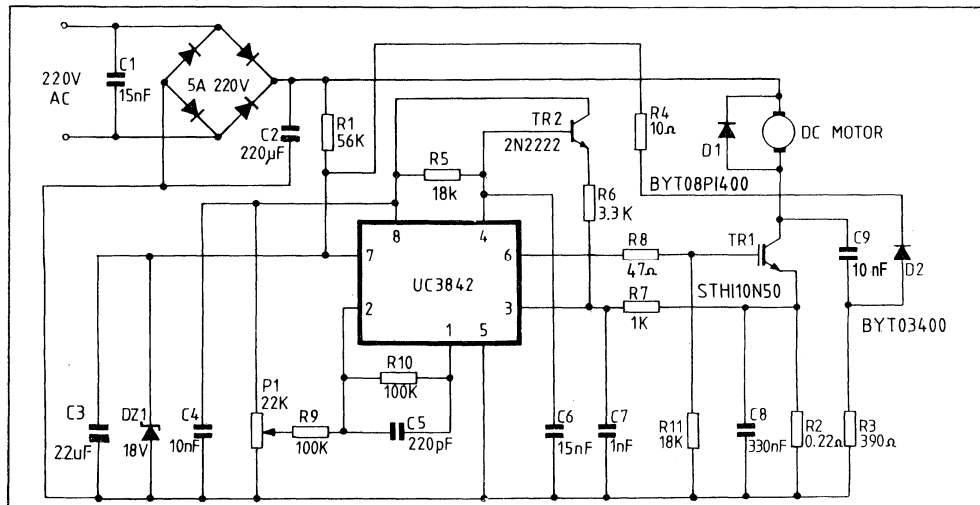
These characteristics are very suitable for motor drive applications in general and make HIMOS the new way of power switching in this area. An additional factor is that a HIMOS device has a smaller chip area than Power MOSFETs, or bipolar transistors with the same ratings ($V_{(BR) DSS}$ and $I_{DS max}$).

CIRCUIT DESCRIPTION

This DC motor drive circuit has a single switch topology and works in current mode; an STH10N50 HIMOS is used as the power switch. The complete circuit schematic is shown in figure 1. Its main features are as follows:

- 300V, 4A DC permanent magnet step down motor drive
- Current mode PWM control
- Output current adjustable pulse by pulse from 0 to 4A
- 220 AC $\pm$ 10% supply voltage
- 6KHz switching frequency
- From 6% to 95% operating duty cycle

Figure 1: Circuit diagram of the HIMOS motor drive



The PWM controller IC used is STUC3842. It is a popular, economic eight pin IC widely used for off-line and DC to DC converters. STUC3842 provides the features necessary to implement fixed frequency current mode control scheme with a minimal external parts count.

Internally implemented circuits include under voltage lockout featuring start-up current less than 1mA, a precision reference, logic to insure latched operation, a PWM comparator which provides current limit control and a totem pole output stage. It can directly drive the gate of the 500V 10A HIMOS switch STH10N50. The choice of this IC and its current mode working matches the requirements of economy and simplicity of this application.

Fig. 2 - STH10N50 output characteristics
(I step = 6V)

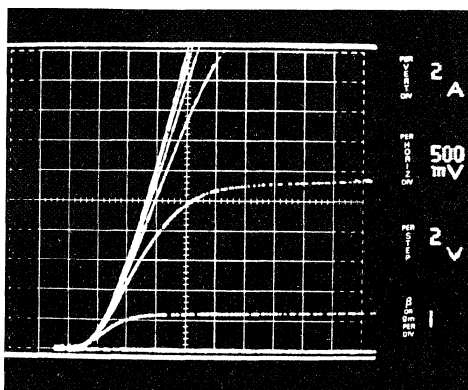
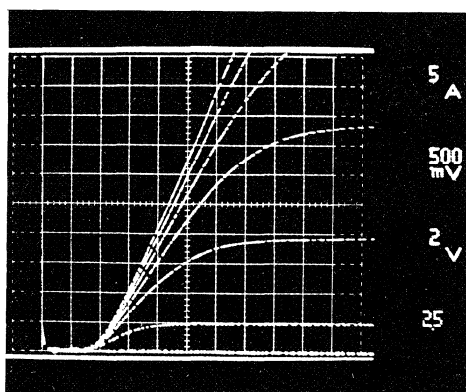


Fig. 3 - STH20N50 output characteristics
(I step = 6V)



The motor speed is controlled by the error voltage which is variable from 0V to +5V, and is applied to pin 2 of the IC by means of R9. This voltage sets a constant current level at which the IC interrupts, pulse by pulse, the current in the power switch: the PWM control is therefore a "current mode" type. The HIMOS switch used is STH10N50, for higher power motors STH20N50 can be used simply by changing resistors R2 and R6 and free-wheeling diode D1. Figures 2 and 3 show respectively the output characteristics of STH10N50 and STH20N50 devices.

An important part of the circuit is the snubber consisting of R3, C9, D2. This accomplishes two functions:

- it provides power for the UC3842 using the charge current of C9 during the STH10N50 turn-off; infact the IC requires about 20 mA DC as supply current and cannot be biased simply through resistor R1 which should be 10Kohm 10W. Instead, using this active snubber, R1 can be set to a value of 56Kohm 2W in order to apply the start up power to the UC3842.
- it reduces the energy dissipated in the power switch during turn-off; consequently a smaller heatsink can be used for STH10N50 giving additional cost reduction.

To insure a continuous power supply to the IC, using the active snubber C9, R3, D2, it is necessary that the capacitor C9 must be completely discharged before turn-off. Because C9 is discharged by means of R3 during the ON phase of the power switch, there is a limit to the minimum ON time which cannot be less than 8 μ s, consequently the minimum duty-cycle is 6%.

Considering a peak current $I_p = 4A$, a fall time $t_f = 1.5 \mu$ s and the minimum ON time of 8 μ s, the values of the snubber components are calculated as follows:

$$C9 = (I_p \cdot t_f) / 2V_{cc} = 10 \text{ nF}$$

$$R3 = T_{on}(\min) / 2 \cdot C9 = 400\text{ohm}$$

The power dissipated across R3 is:

$$P = 1/2 \cdot C9 \cdot V^2 \cdot f = 3W$$

The adoption of this snubber does not affect the efficiency of the circuit during normal operation because its power dissipation is very low and it has the additional benefit of using this energy to supply the IC so reducing the dissipation in the power switch. The extra cost is negligible with respect to the cost of a transformer for supplying the low voltage power to the IC.

The network of Tr2 and R6 adds a fraction of the ramp oscillator voltage to the "current sense" si-

gnal at pin 3 of the IC (via transistor Tr2 2N2222) to allow slope compensation. Consequently duty-cycles as high as 50% can be obtained.

Diodes D1 (BYT08PI400) and D2 (BYT03400) are fast recovery types and have been used in order to minimize stresses on the power switch.

MEASUREMENTS ON THE CIRCUIT

The DC motor drive was tested in several operating conditions. These were maximum and rated output current and in blocked rotor conditions.

The waveforms of the drain voltage, V_{DS} , drain current, I_D , and gate voltage, V_G , both with and without the snubber can be seen in figures 5 and 6 respectively.

Fig. 4 - STH10N50 turn-off with snubber $I_d = 1A/div$, $V_{ds} = 50V/div$, $V_g = 5V/div$

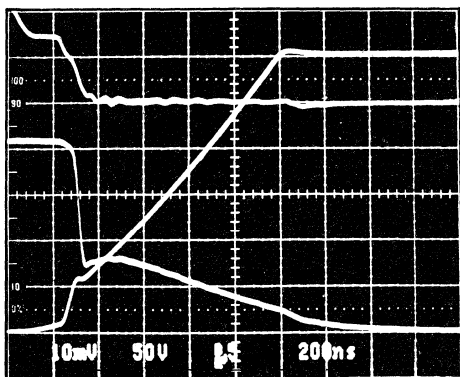
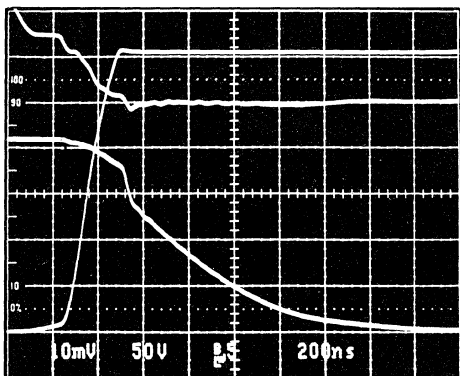


Fig. 5 - STH10N50 turn-off without snubber $I_d = 1A/div$, $V_{ds} = 50V/div$, $V_g = 5V/div$



Here you can see the typical behaviour of a HIMOS device at the turn-off when typical features of both Power MOSFET and BJT are involved. The storage phase of the turn-off is dependent on the MOS behaviour as the base collector junction of the PNP transistor is reversed biased: the gate voltage decreases to a point where the Miller effect begins to control the current in the drain and V_{DS} start to rise. The fall time phase can be divided into two parts: the first part is the MOS turn-off and is very fast, the second is slow and starts when the MOS channel is closed and the PNP transistor has an open base turn-off and is dominated by recombination of excess carriers. Therefore the first part of the time is controlled by the gate drive circuit, the second part is dependent on the PNP transistor life-time and gain.

Since the PNP gain increases as V_{DS} increase, the fall time consequently varies with V_{DS} . Therefore, when the snubber is used and the V_{DS} slope is dominated by the capacitance, the fall time region due to the MOS is more evident (figure 6).

Figure 6 shows the turn-on behaviour of the HIMOS: it very fast (t_{rise} 30ns) and, as with Power MOS devices, is a function of the impedance of the driver circuit and the applied gate voltage.

Fig. 6 - STH10N50 turn-on $I_d = 1A/div$, $V_{ds} = 50V/div$

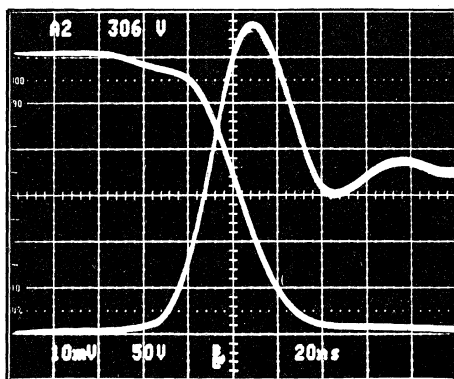
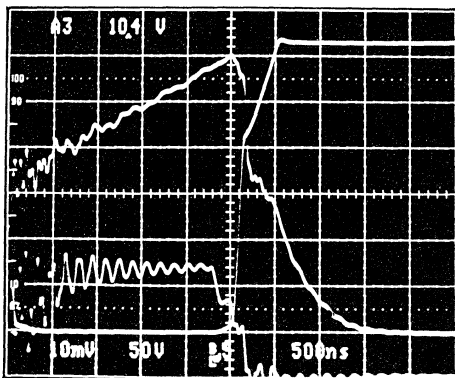


Figure 7 shows the behaviour in the case of a blocked rotor and with the current control set at the maximum 4A. This condition was simulated, as worst case, with an inductance of 300uH and a resistance of 1 Ω : the current does not exceed 6A. The over-current of 2A, with respect to the control current of 4A, is due to the delay introduced by the network

of R7, C7 of about $2\ \mu\text{s}$. This filter network is necessary to suppress the leading edge spikes on the IC current sense comparator input.

Fig. 7 - Blocked rotor' behaviour $I_d = 1\text{A/div}$,
 $V_{ds} = 50\text{V/div}$, $V_g = 5\text{V/div}$



The losses in the circuit, for the maximum rating of each component are approximately as follows: $P(R1) = 2\text{W}$, $P(R3) = 3\text{W}$, $P(R2) = 3\text{W}$, $P(D1) = 4\text{W}$, $P(Tr1) = 7\text{W}$.

CONCLUSION

A 300V 4A DC permanent magnet single quadrant motor drive was developed with objectives of maximum circuit simplicity and economy. Consequently a current mode PWM control with a popular IC was adopted and an STH10N50 HIMOS (an IGBT) was used.

The low drive energy requirement due to the high input impedance of the HIMOS allows substantial cost reduction in the control circuit. Conductivity modulation of the drain produces a low ON resistance, an essential feature to work with high peak currents in the switching element. The ruggedness, due to the excellent safe operating areas, is especially relevant for motor control applications.

The easy drive, high current handling and excellent ruggedness make HIMOS the new way of power switching in the motor control field.

DRIVERS AND IPS

SWITCH-MODE DRIVERS FOR SOLENOID DRIVING

This design guide describes the operation and applications of the L294 and L295 switch-mode solenoid drivers. Integrating control circuitry and power stage on the same chip, these devices replace complex discrete circuits, bringing space and cost savings.

Many applications, particularly in computer peripherals, require a high power, fast solenoid driver circuit. In the past these circuits have been realised with discrete components because the high powers required precluded the use of monolithic technology.

SGS-THOMSON Microelectronics has overcome this problem with a new high power bipolar technology that uses an innovative implanted isolation technique. This technology is used to fabricate two switchmode solenoid driver chips, the L294 and L295, which both incorporate high power output stages and control circuitry. Both circuits are designed for efficient switchmode operation and are mounted in Multiwatt[®] plastic package.

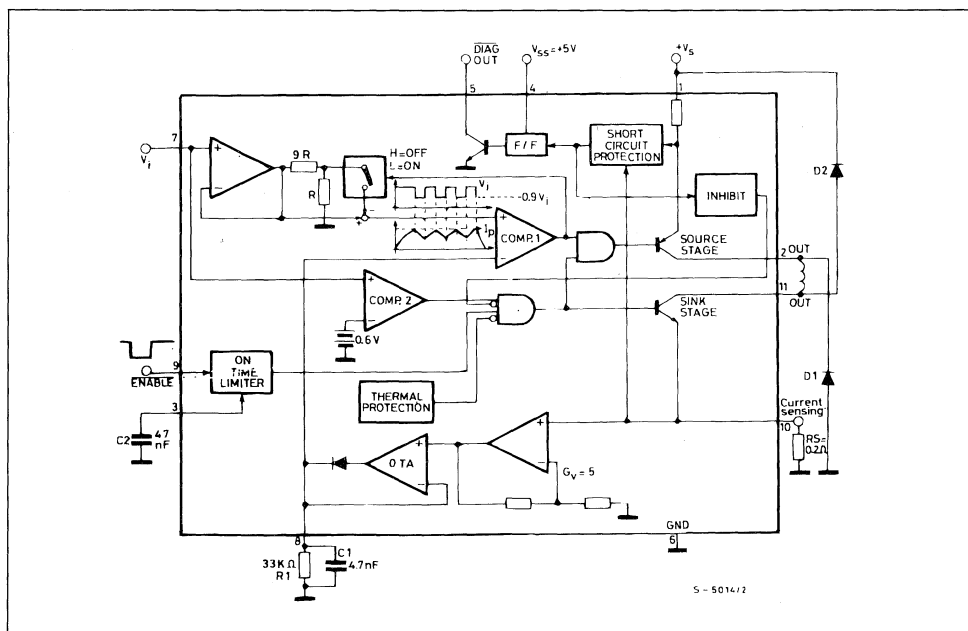
THE L294 SOLENOID DRIVER

The L294 is designed for solenoid driving applications where both very high speed and high current are essential; needle and hammer driving in printer mechanisms, for example. It delivers 4 A with supply voltages up to 46 V, handling effective powers up to 180 W.

Shown in figure 1, the L294 is controlled by a TTL - level logic input and the peak load current is programmed by a reference voltage applied to the pin labelled V_i .

Internal switchmode control circuitry regulates the solenoid current by turning the output stage on and off repeatedly to keep the load current between the

Figure 1 : Internal Block Diagram of the L294 Switchmode Solenoid Driver.



programmed peak value, I_p , and a lower limit of 0.9 I_p .

Other features of the L294 include thermal shut-down, output short circuit protection, overdriving protection and a latched diagnostic output. This output indicates fault conditions such as a short circuit solenoid.

CIRCUIT OPERATION

In most applications the L294 is used with a fixed reference voltage (V_i) and the solenoid is controlled by negative-going pulses on the ENABLE input. When the ENABLE input is active (low level), the output stage is enabled and the load current rises as shown in figure 2.

The load current is sensed by an external resistor (R_s) in the emitter of the sink stage. Through the op amp and transconductance amplifier (OTA), the sensed voltage charges an external RC network ($R1C1$) which determines the switching characteristics of the device.

Figure 2 : Output Current Waveforms of the L294. The Output Current is regulated by Switching between a Peak Value, I_p , and a lower Limit of 0.9 I_p .

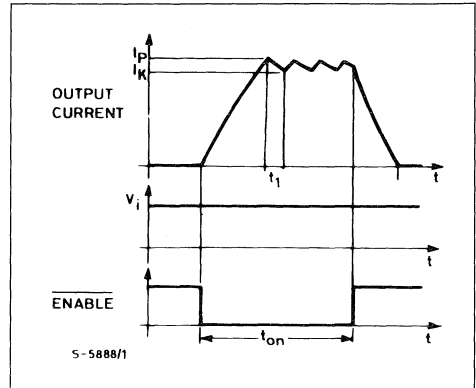
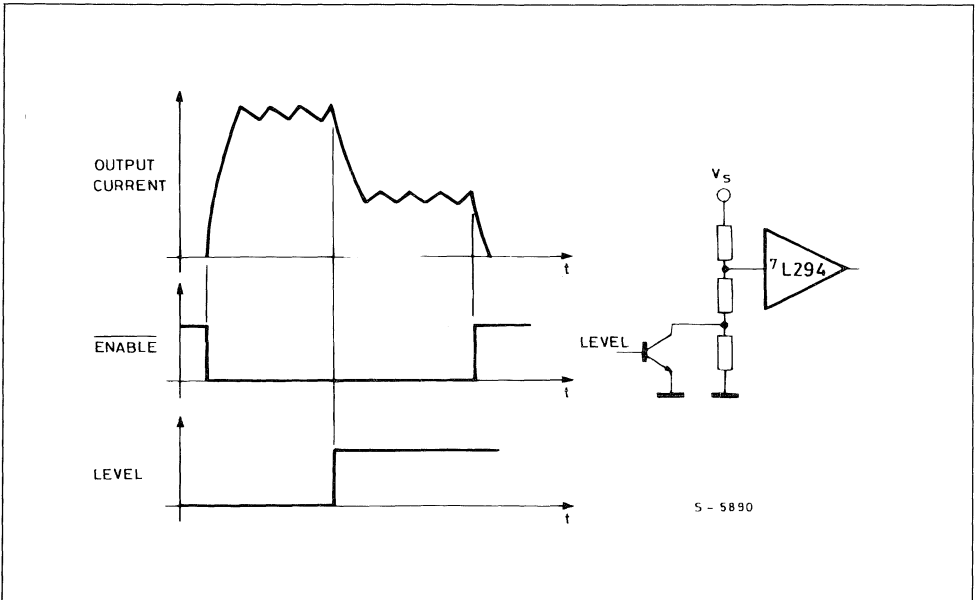


Figure 3 : Two Level Current Control can be implemented by switching V_i between two Values.



The voltage across this RC network is compared with the voltage V_i , which fixes the output peak current. When the current has reached the programmed peak value this comparator switches, turning off the output source stage and closing a switch which reduces the voltage on the non-inverting input to $0.9 V_i$. The load current now recirculates in D1. The voltage on pin 8 falls with a time constant determined by R1C1 or the load characteristics, whichever is the longest. In other word. R1C1 sets the minimum recirculation time constant.

When the voltage across R1C1 has fallen to the $0.9 V_i$ threshold the comparator switches on, turning the output stage back on and restoring the V_i comparison threshold.

The output source stage is switched in this way, regulating the load current, until the ENABLE input goes high again. At this point the output stage is disabled - both source and sink - and the load current recirculates through D1 and D2 to ensure a fast decay. By varying the voltage V_i the peak load current can be programmed to any value in the range 0.6 A to 4 A. This feature can be exploited to implement two-level current control if the fixed reference is replaced by a switched reference as shown in figure 3.

PROTECTION

To protect the load and the L294 from overdriving an on-time limiter inhibits the output stage independently of the ENABLE input if the duration of the input pulse exceeds a period set by the external capacitor C2 (figure 4). This circuit is reset by taking the ENABLE input high. The on-time limiter can be disabled by grounding pin 3.

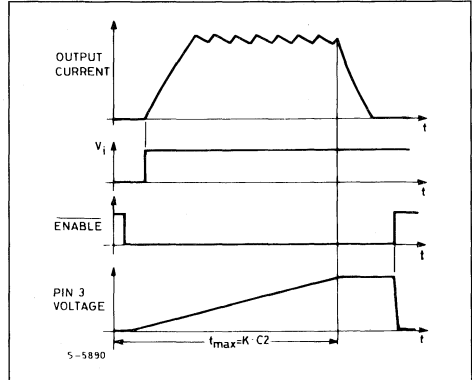
Protection against overheating is incorporated in the form of a thermal shutdown circuit which disables the output stage when the junction temperature exceeds 150°C . The circuit restarts when the temperature has fallen about 20°C .

The L294 is also protected against short circuits to ground, to supply and across the load. Triggered when the source stage current exceed 5 A or the sink stage current exceed $1 V/R_s$, the short circuit protection block inhibits the output stage and sets a flip flop which is supplied by a separate supply voltage V_{SS} . This flip flop is connected to the diagnostic output and signals that all is not well - a shorted solenoid, for example. The diagnostic flip flop is reset by removing the supply V_s .

A LED can be connected to the diagnostic output as shown in figure 5. If the diagnostic function is not re-

quired the V_{SS} supply can be omitted. The short circuit protection, however, still functions, even without V_{SS} .

Figure 4 : On-time Limiter Waveforms. After a Period defined by C2 the Output is disabled regardless of the State of ENABLE, protecting against overdriving.



USING THE L294

The basic application circuit for the L294 is shown in figure 5 ; a suggested layout is given in figure 6. The circuit is complete except for the source of V_i . In most cases this will be provided by a simple resistive divider dimensioned to set the desired peak current. With a 0.2Ω sense resistor as shown, the L294 has a transconductance of 1A/V for V_i above 600 mV. The device will not work with V_i less than 450 mV and operation is not guaranteed for V_i between 450 mV and 600 mV.

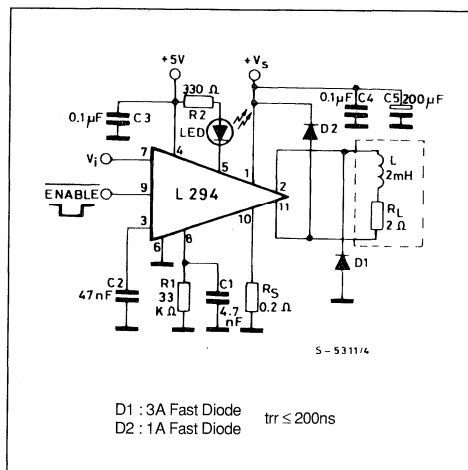
The on-time limiter delay - set by C2- is approximately $120\,000 \times C2$. Pin 3 must be grounded if the on-time limiter isn't used.

Switching frequency depends partly on the timing network R1C1 and partly on the load characteristics.

R1C1 determines the minimum value of t_1 (see figure 2), which is given by $t_1 \geq 0.1 \times R1C1$. C1 must be in the range 2.7 - 10 nF to ensure stability of the amplifier OTA. R1 must be at least 10 k Ω to give sufficient gain for OTA. The standard application circuit of figure 5 has a switching frequency of about 10 kHz.

The recirculation diodes should be fast types and rated at 3A (D1) and 1A (D2). If the full 4A capability of the L294 is not used these can be reduced.

Figure 5 : Standard Solenoid driving Application of the L294. Pin 7 must be connected to a Suitable Reference Voltage to set the Peak Current.



A high initial peak and low holding current can be obtained with the circuit shown in figure 7a. This example supplies a current peak for about 10 ms.

The peak current, I_{OEX} , (see figure 7a) is found from :

$$I_{OEX} = \frac{V_z}{5} \cdot \frac{R_2}{R_s} \cdot \frac{1}{R_1 + R_2}$$

V_z is the zener voltage. The zener and R5 can be omitted if a regulated 5 V supply is available for point A.

The holding current, I_{hold} , is found from :

$$I_{\text{hold}} = \frac{V_z}{5} \cdot \frac{(R_2 \parallel R_4)}{R_S} \cdot \frac{1}{R_1 + (R_2 \parallel R_4)}$$

The duration of the peak is determined by R3C1 and is increased by raising R3 or C1.

Typical component values are listed in the table below :

	I_{OEX} = 4 A I_{HOLD} = 1 A	I_{OEX} = 2.5 A I_{HOLD} = 0.5 A
R1	10 kΩ	10 kΩ
R2	47 kΩ	27 kΩ
R3	150 kΩ	150 kΩ
R4	2.7 kΩ	1.5 kΩ
R5	0.2 Ω (1 W)	0.27 Ω (0.5 W)
D1	3 A	1.5 A
D2	0.5 A	0.5 A
C1	0.2 μF	0.2 μF

Figure 6 : Suggested printed Circuit Board layout for the Application Circuit of figure 5.

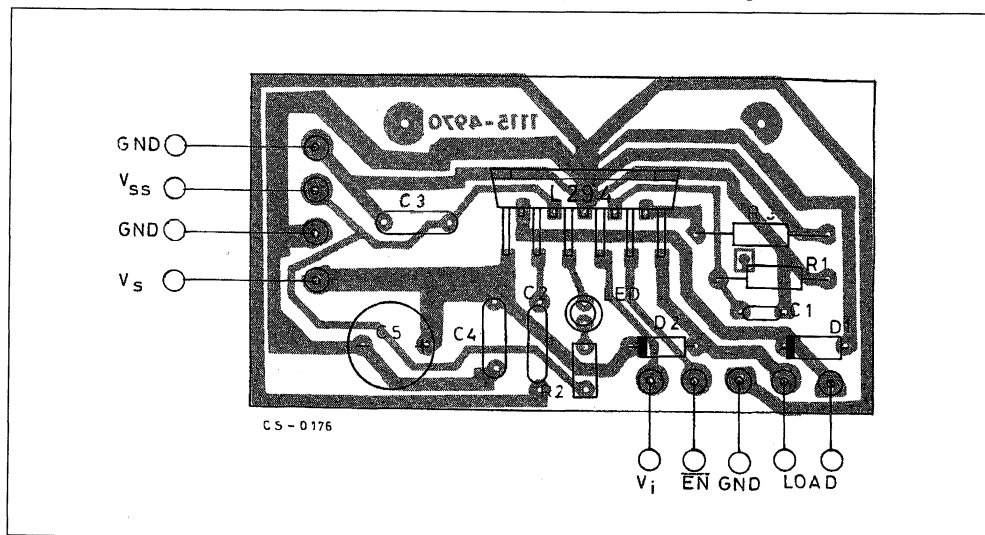


Figure 7a : Application Circuit for two Level Current Control. This Circuit generates a high Peak Current for a Period determined by R3C1 then a lower holding Current.

Figure 8 : Pin Functions of the L294.

N°	Function
1	Solenoid Supply Voltage V_s (12-46 V)
2	Output, Source Stage
3	On-time Limiter Time Constant. A capacitor to ground sets delay period ($120\,000 \times C_2$ seconds). On-time limiter is disabled by grounding this pin.
4	Supply Input (5 V) for Diagnostic Flip Flop.
5	Diagnostic Output, Open Collector. Signals intervention of latched short circuit protection. Reset by removing pin 1 supply.
6	Ground.
7	V_i Reference Input. Peak output current is proportional to V_i . Transconductance is 1 A/V for $R_S = 0.2\ \Omega$ and $V_i \geq 600\text{ mV}$.
8	Timing. A parallel RC network from this pin to ground sets the minimum recirculation time constant. The capacitor must be 2.7-10 nF to ensure stability. The resistor must be greater than 10 k Ω .
9	ENABLE. TTL-compatible logic input that controls the solenoid current. The solenoid is driven when this input is at a low level. The on-time limiter overrides enable.
10	Connection for Load Current Sense Resistor.
11	Output, Sink Stage

THE L295 DUAL SWITCHMODE DRIVER

The L295 is a dual switchmode solenoid driver which handles up to 2.5 A per channel at voltages up to 46 V - a total effective power handling of 220 W. Compared to the L294 it offers a more economical solution when 2.5 A is sufficient because there are two drivers per chip. Like the L294 it features switchmode regulation of the output current and thermal shutdown. Additionally it has a separate logic supply input so that the logic can be run at a lower voltage, reducing dissipation.

Intended for inductive load driving, the L295 is particularly suitable for solenoids and stepper motors. One L295 drives two solenoids and two L295s can drive the four phases at a unipolar stepper motor or the two phases of a bipolar stepper motor in bridge configuration.

Each channel of the L295 is controlled by a TTL-level digital input and the peak load current is programmed, independently for each channel, by a voltage reference input. A chip enable input is also provided to disable both channels together.

INSIDE THE L295

Internally the L295 (figure 9) bears little resemblance to the L294. Looking at channel one, when the V_{IN1} input goes high the output transistors Q1 and Q2 are switched on (the enable input EN is assumed to be active, i.e. low). The current in the load then rises exponentially, as shown in figure 10, until

the voltage across the external sense resistor R_{S1} reaches the current program reference voltage V_{ref1} .

The comparator COMP1 switches and sets the flip flop FF1 which turns off the source transistor Q1. The load current now recirculates through D2-Q2- R_{S1} and decays.

What happens next is determined by the oscillator components R and C on pin 9. If these components are present the flip flop is reset by the next clock pulse before the current decays very far. The output stage is therefore turned on again and the load current rises.

When it reaches the peak value COMP1 switches again, setting the flip flop and disabling the output stage. This process is repeated, regulating the load current until V_{IN1} goes low. The output stage is then disabled and the current falls off rapidly, recirculating through D1 and D2 (figure 10).

If the oscillator components are omitted and pin 9 grounded the current simply decays slowly until V_{IN1} goes low. The output stage is then disabled and the load current recirculates through D1 and D2. This case is illustrated by the waveforms of figure 11. Note that in this case the peak current level is controlled.

Unlike the L294, the switching frequency of the current regulation loop is determined by the oscillator components R and C (the L294 is also affected by the load). Typically, the switching frequency will be

10-30 kHz. Another difference between the two devices is that the L294 gives a constant ripple, the L295 does not.

TWO LEVEL CONTROL

Since the peak load current is programmed by the reference voltage (for each channel), two level cur-

rent control can be obtained by switching between two reference voltages. A high V_{ref} is selected initially to give a high initial current peak. Then, after a suitable interval, V_{ref} is reduced to give the lower holding current (figure 12). Two level current control is very useful for solenoids which require a high initial current peak for fast actuation.

Figure 9 : Internal Block Diagram of the L295 Dual Switchmode Driver.

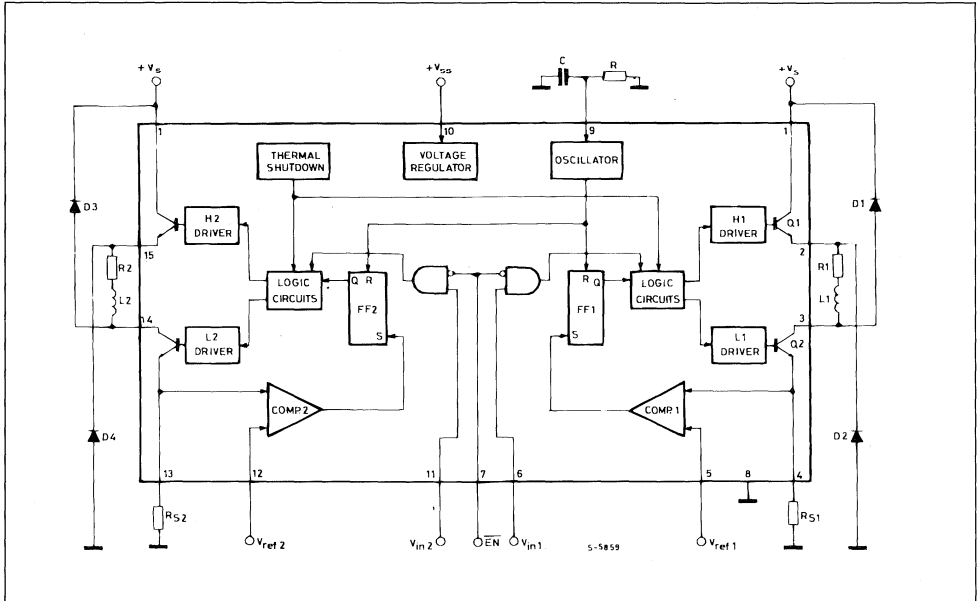


Figure 10 : Waveforms illustrating Normal Operation of the L295.

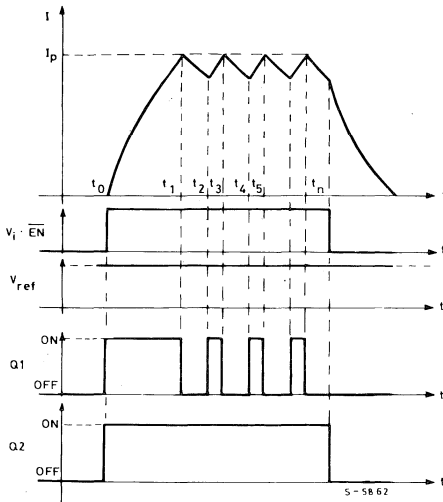


Figure 11 : When the Oscillator Components are omitted and Pin 9 grounded the L295 delivers a simple Current Peak to the Load.

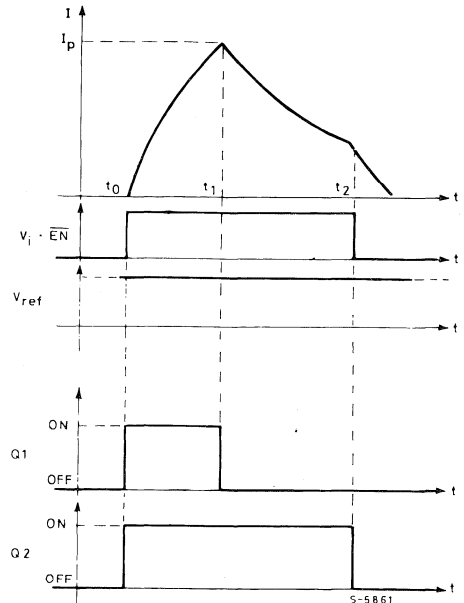
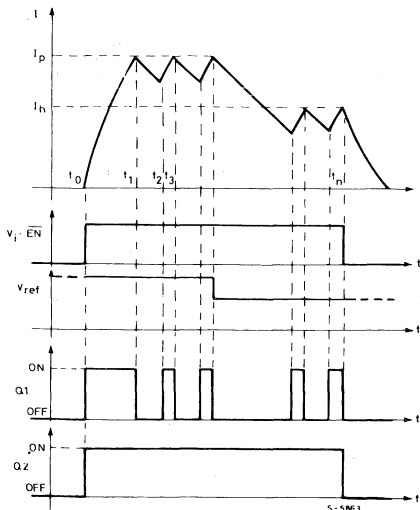


Figure 12 : Two Level Current Control is obtained by switching V_{ref} between two Values.



L295 APPLICATION HINTS

The basic application circuit of the L295 is shown in figure 14. A suitable layout is given in figure 15.

Suitable values for the oscillator components, R and C, can be found from the nomogram, figure 16. The value for the reference voltages depends on the desired peak current and is equal to $I_p R_s$; it must be in the range 0.2 V to 2 V.

If the V_{ref} inputs are left open circuit the L295 assumes an internal default value of 2.5 V giving a peak current of $2.5/R_s$ amperes.

The L295 can also be used to drive unipolar stepper motors. For a four phase motor two devices are used, connected as shown in figure 17. This circuit

provides switchmode regulation of the load current with a chopper rate of about 25 kHz. The enable inputs (EN, connected together) enable/disable the whole circuit and the channel inputs $V_{in1} \dots V_{in4}$ are driven by a suitable translator circuit. Phases 1 and 2 must not be energised together because they share the same sense resistor. The same applies to channels 3 and 4. However, 'two phase on' drive is still possible for bifilar motors where phases one and two represent one winding and 3 & 4 the other, and also for variable reluctance motors with phase 1 adjacent to phase 3 etc.

Two L295s could also be used to drive a bipolar stepper motor in systems where a translator already exists.

Figure 13 : Pin Functions of the L295.

N°	Function
1	Solenoid Supply Voltage, V_s (12-46 V).
2	Channel one Output, Source Stage.
3	Channel one Output, Sink Stage.
4	R_{S1} . Sense Resistor Connection, Channel one.
5	V_{ref1} . A voltage on this pin sets peak current of channel one. If this pin is left open or connected to V_{ss} a default V_{ref} of 2.5 V is assumed. An externally applied V_{ref} must be in the range 0.2 to 2 V.
6	V_{in1} . Logic Input for Channel one. Driver is active when V_{in1} is high and EN low.
7	$\overline{EN}$. Chip Enable (active low). When high both channels are disabled.
8	Ground.
9	Oscillator Timing Network. This pin is grounded to produce a single peak.
10	V_{ss} . Logic supply voltage, internally regulated. (4.75-10 V).
11	V_{in2} . Logic Input for Channel two. Driver is active when V_{in2} is high and EN low.
12	V_{ref2} . Voltage input, controls peak current of channel two. If left open or connected V_s an internal 2.5 V reference is assumed. An externally applied V_{ref} must be in the range 0.2 to 2 V.
13	R_{S2} . Sense Resistor Connection, Channel two.
14	Channel two Output, Sink Stage.
15	Channel two Output, Source Stage.

Figure 14 : Typical application Circuit of the L295. R1 L1 and R2 L2 are solenoids.

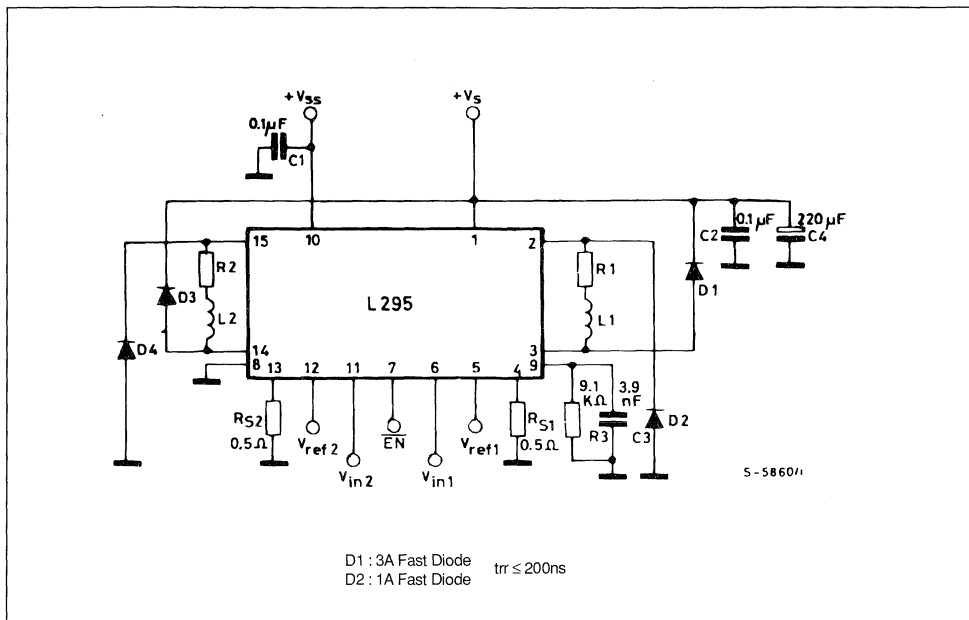


Figure 15 : Suggested printed Circuit Board layout for the Circuit of figure 14.

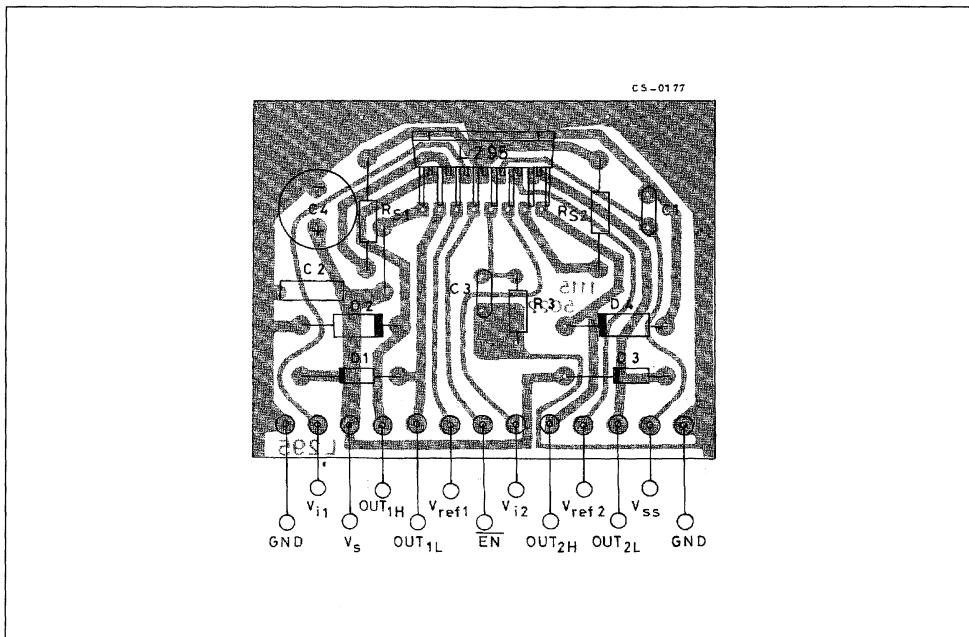


Figure 16 : Nomogram for the Selection of Values for the Oscillator components. RC.

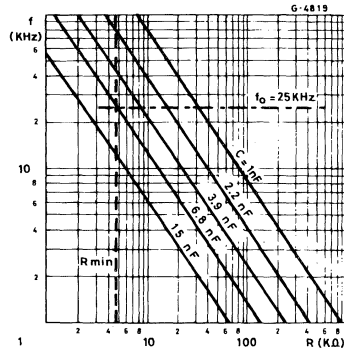
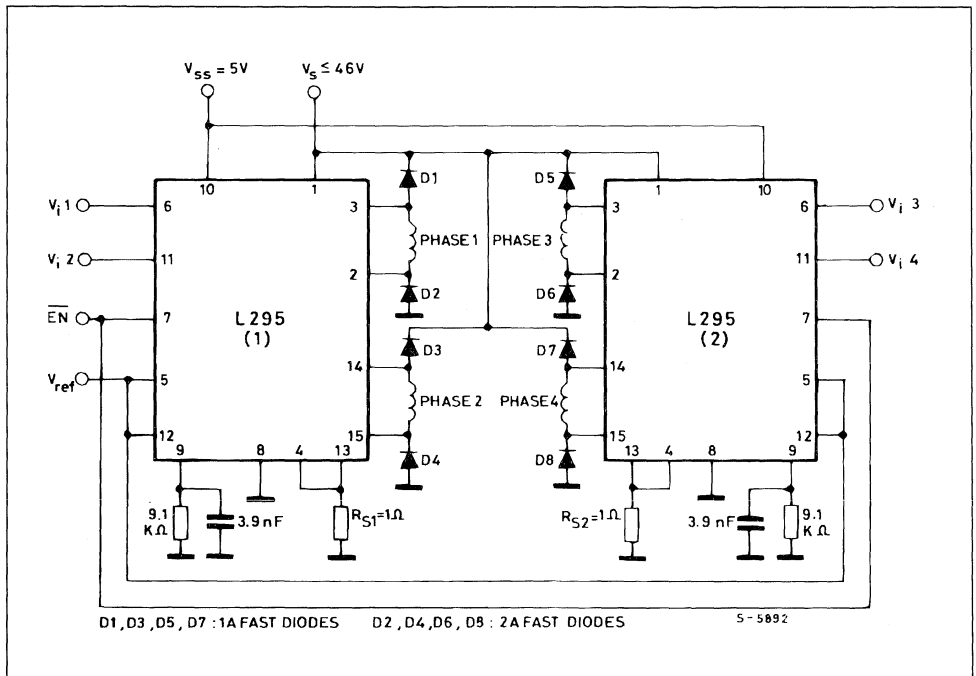


Figure 17 : Two L295s, connected as shown, can be used to drive a four Phase Unipolar Stepper Motor.



INTELLIGENT AUTOPROTECTED DRIVERS

by I.M.PETER and I.RATES

INTRODUCTION

In industrial applications, where digital control signals are provided by automation equipment, suitable **Drivers** are required to control various loads such as Relays, Lamps, Electrovalves, etc.

What are the essential main characteristics of these Drivers ?

- Primarily, they must be autoprotected, that is, they must be self-resistant to industry-originated disturbances, short-circuits, over-currents, accidental load and ground disconnection, and so on.
- Then, in case of fault occurrence, they must be capable of providing interactive dialogue with the central processor unit.
- And finally, they must meet the requirements of the standards currently in force and those of the forthcoming projects, imposing that one terminal of the load should be directly connected to ground (see figure 1).

The objective of this note is to discuss and illustrate how a family of autoprotected control has been developed from basic concepts and also to outline the likely future trends.

FUNDAMENTALS

The control signal is applied to a comparator, the output of which drives a current source. This current source in turn drives the power transistor T1. A transistor T2 driven by the voltage drop across shunt R_{sc} is configured to provide feed-back to power transistor T1. As soon as the voltage drop across this shunt exceeds 0.7V, T1 T2 configuration will act as a current limiting-unit so that $I_{limit} = 0.8/R_{sc}$. This is how the device is protected against short-circuits.

Another internal unit monitors the junction temperature which varies as a function of dissipated power (i.e. $V_{CC} \times I_{CC}$) and cooling conditions. As soon as this temperature exceeds $+175^{\circ}\text{C}$ (upper threshold), the protection unit is activated and will sink the generator current I_B thereby turning the device off. In the off condition, the device will cool down, and when the junction temperature falls below $+140^{\circ}\text{C}$ (lower threshold), the thermal protection unit is deactivated and the device is restored to its normal operating mode. However, if the overload conditions persist, the system will operate in low frequency relaxation mode with a frequency ranging from 1Hz to a few Hz according to the nature of the overload. Whatever the operating conditions :

- The current is limited at a programmable level.
- The junction temperature limit is never exceeded.

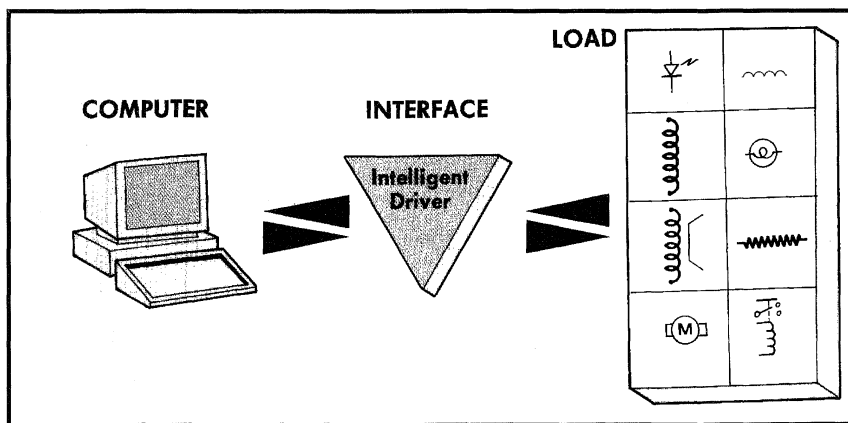


Figure 1 : There are two possible configurations of load/controller combination. Some standards and forthcoming projects will require one end of the load to be directly connected to ground.

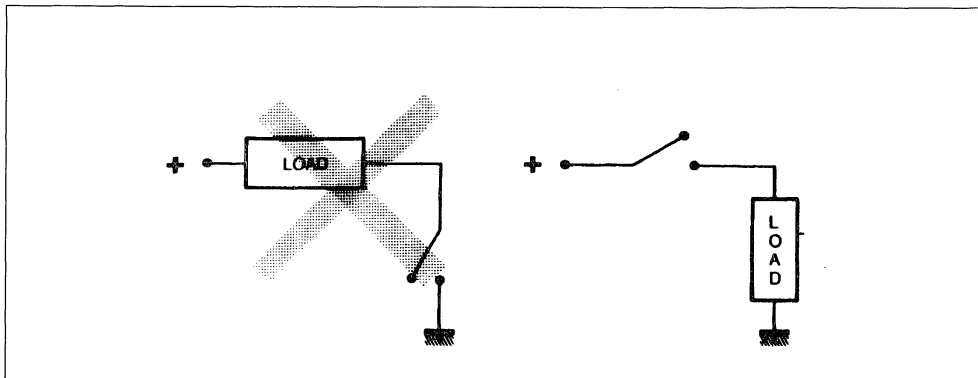
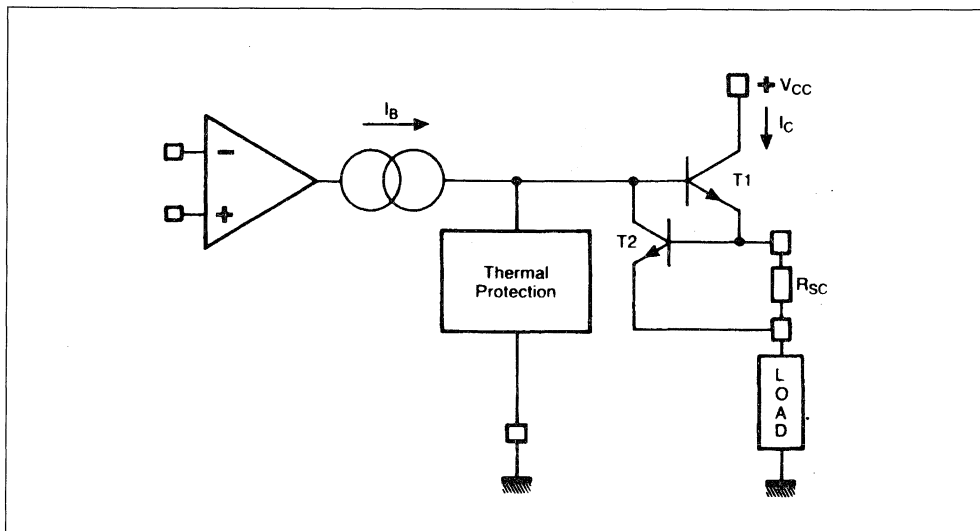


Figure 2 : Basic Functional Diagram of TDE 1647.



These features make the TDE 1647 which is the basic circuit of the family, a switch well-suited to applications implementing drives for lamps, inductive loads, blinkers and relays, etc.

It is worth mentioning that the current limit feature when used to limit the starting current, will in the case of incandescent bulbs, result in a considerable extension of their life duration.

INTERACTIVITY – A SECOND FAMILY OF CIRCUITS

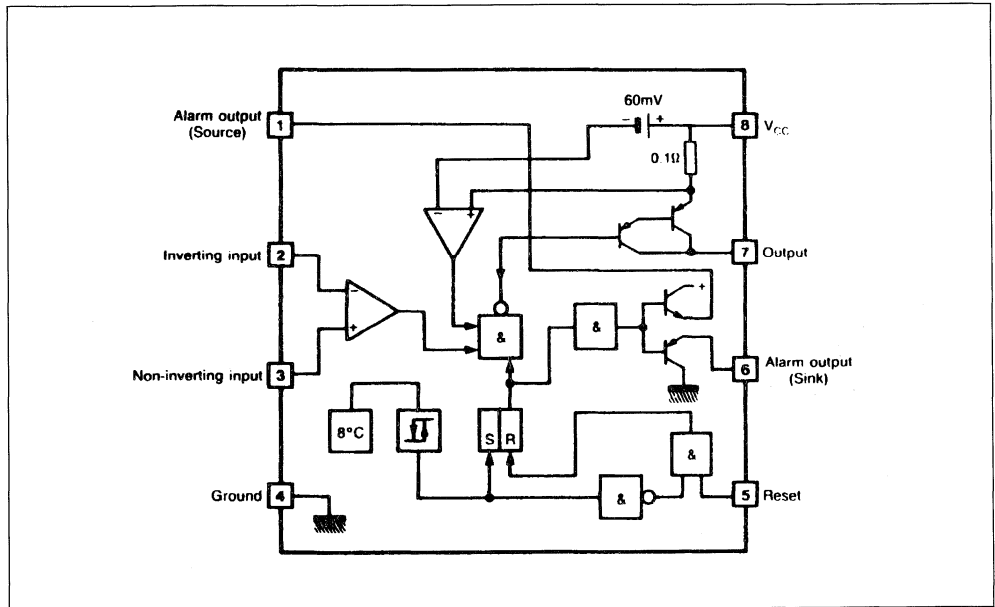
In many applications, the control system must receive the acknowledgement of the execution of an issued command, or receive information reflecting possible failures and disturbances. The TDE1798

has been designed to meet these requirements (see figure 3).

This autoprotected driver contains memory logic circuitry required to latch the device status and return the stored information to the processor.

This device is protected against thermal overloads exactly in exactly the same way as TDE1647 and in addition, if Reset input is held low, the driver output remains blocked after a thermal overload and this condition is indicated by a signal sent through the Alarm output pin. The Reset input is used to return the circuit to its normal mode of operation. In fact, if this input is maintained high, the device will operate in exactly the same way as TDE1647 that is, in case of continuous overloads, it will function in a low-frequency relaxation mode.

Figure 3 : TDE 1798 Autoprotected Control.



SHORT-CIRCUIT PROTECTION.

This device is protected against short-circuits by a current-limit feature operating exactly the same as the preceding device. Under overload conditions, the current is limited but the memory logic function is inactive.

POWER SUPPLY VOLTAGE LIMITS.

All of the devices of the entire family operate in a wide range of supply voltages : from + 6V to maximum voltage (between + 3V and + 6V, the protection logic is operational but the temperature detection circuit becomes inactive).

INDUCTIVE LOADS.

If a free wheel diode is connected across an inductive load, the voltage drop remains null while current decays slowly (figure 4). Two distinct solutions are possible to provide a rapid fall of this current :

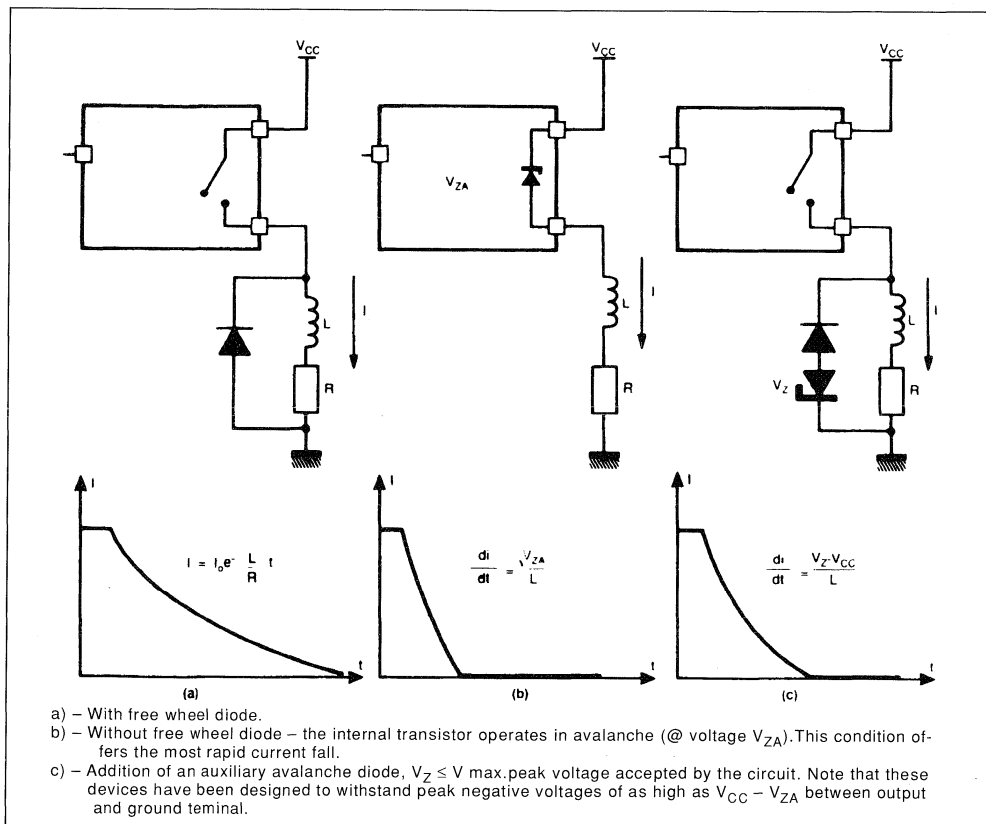
a)- Do not connect any additional device across the load. The output transistor of TDE1767/TDE1798 has been particularly designed to operate in avalanche mode and to clamp at voltage V_{ZA} . This outstanding feature eliminates the need of additional components in the case of inductive loads and automatically provides a rapid fall of load current.

As far as the users are concerned, this is an interesting feature. However, care must be taken not to exceed the operating limit of this transistor ; that is, energy dissipated in the transistor ($\frac{1}{2} L I^2$) should be less than 100mJ.

b)- In the case where energy stored in the load is very large, a Zener diode may be used to absorb this energy.

In case (b), the device and its internal logic circuits are protected against negative voltage peaks appearing between output and ground (figure 4).

Figure 4 : Current Decay in an Inductive Load.

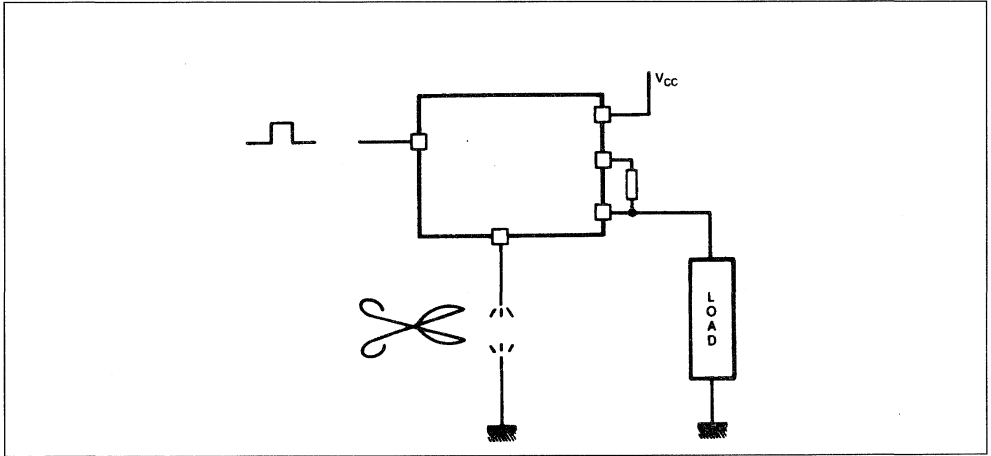


GROUND DISCONNECTION.

Besides the protection against disconnection of the power circuitry, these devices are also protected against accidental disconnection of ground return path. This is an outstanding security feature and the

TDE1798 was particularly developed to meet VDE422, the European standard which requires an instantaneous disabling of the output circuitry in case of accidental disconnection of ground (figure 5).

Figure 5 : The autoprotected control meet European security standard requirements. Output is automatically disabled in case of accidental disconnection of ground path.

**ANOTHER PROGRAMMABLE CIRCUIT.**

TDE1767 is another version of this circuit which in combination with an external resistor, implements a programmable short-circuit detection feature.

HIGHER POWER – OPTIMUM SECURITY

The control discussed so far are specified for output currents of 0.3A to 0.5A. TDF1778 & TDF1779 are dual autoprotected control capable of handling up to 2 x 2A. These monolithic devices contain 2 individual drivers which share a common monitoring logic circuitry (figure 6).

Protection features offered by these circuits are :

- A thermal protection feature similar to circuits mentioned earlier.

- Signalling Logic, Fault Memory and the availability of a Reset input (similar to preceding circuit).

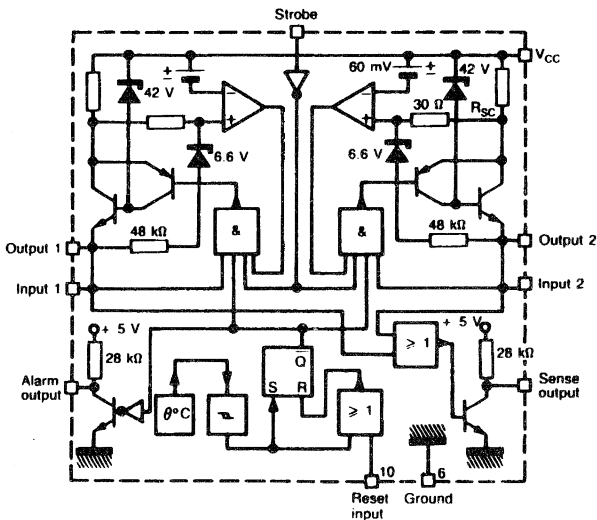
- Short-circuit protection. If the device is operated with current of the order of 2A, safe operating

area of the transistor must be taken into account. Figure 7 illustrates the characteristics of the integrated protection unit. The fault memory feature is inactive when device is in current limit mode.

The output transistor of these circuits is not protected in avalanche. However, in the case of TDF1778, a 42V Zener diode inserted between the positive supply and the base of the output transistor, will transform it to an avalanche protected transistor.

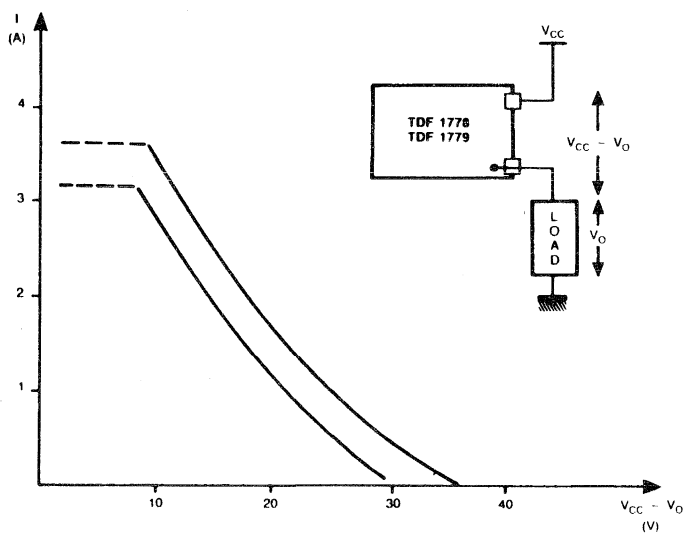
An additional feature, detection of load disconnection, is also offered by these circuits. A high-value resistor (not shown in the figure 6) is connected between the power supply terminal and the outputs. As long as the load remains connected to the output and the input is blocked, the output potential is practically null. If the load is disconnected, this potential will rise and correspondingly, a signal is sent to the central unit through the Sense Output terminal.

Figure 6 : TDF1778 Autoprotected Control.



Dual output : 2 x 2A. Fault memory. Thermal and short-circuit protection. Detection of and protection against ground and load disconnection.

Figure 7.



Current protection limit. For TDF1778 and TDF1779 devices, this varies as a function of $V_{CC} - V_O$ voltage appearing across the controller. This limit corresponds to the safe operating area.

APPLICATIONS

Main characteristics of this family of AUTOPROTECTED CONTROL are :

- Particularly suited to 24V to 48V - 0.3A to 4A systems.
 - Operation from + 6V to maximum voltage.
 - Can be used in parallel configuration.
- Protection against :
 - Over-currents.
 - Excessive heating.
 - Accidental ground disconnection.
 - Interactive dialogue with central processor unit (ALARM & RESET) terminals available on certain series.
 - Detection of load disconnection (TDF1778 & TDF1779).
 - Protection of output transistor by avalanche (some families).
 - μ P and TTL compatible inputs.

Figure 8 illustrates some conventional industrial automation applications built around these devices.

Power handling capability of these devices can be readily enhanced by the addition of an external power transistor as shown in figure 9. Further to these conventional applications, autoprotected control are also well suited for the implementation of choppers (figure 10) and more complex circuits (Bridge, Half bridge...).

FUTURE EVOLUTION

Two trends for these circuits :

- Enhancement of power handling capability.
- Reduction of losses - A new circuit offering considerable reduction of voltage drop and thus the losses, is forecast to be available in 1986. One of the consequences will be improving the circuit density in the equipment, thus achieving size reduction.

CONCLUSION

This new family of devices opens a new era of controllers which are :

- On one hand stand-alone, i.e. self-protected against external disturbances. If operated in this mode, in case of fault occurrence, the device itself will make the appropriate decision without the intervention of the central processor unit.
- On the other hand, capable of interactive dialogue, which means they are readily associated to processors and monitored by digital systems.

Figure 8 : Some Typical Applications of Autoprotected Controllers.

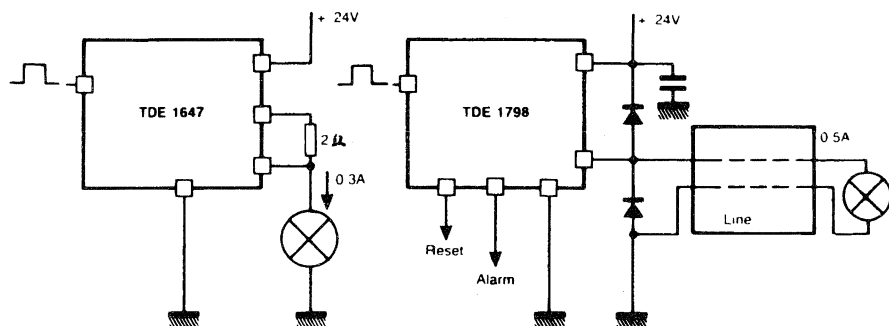
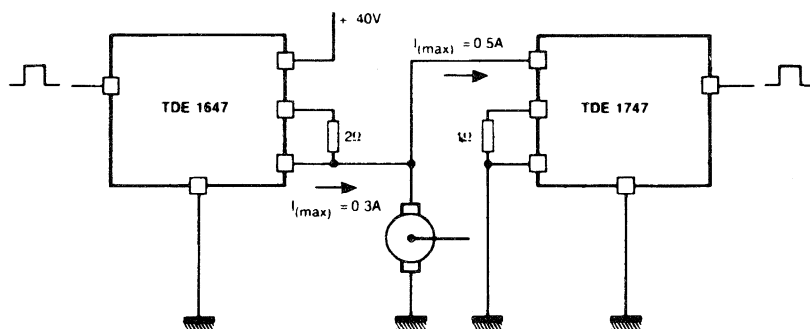
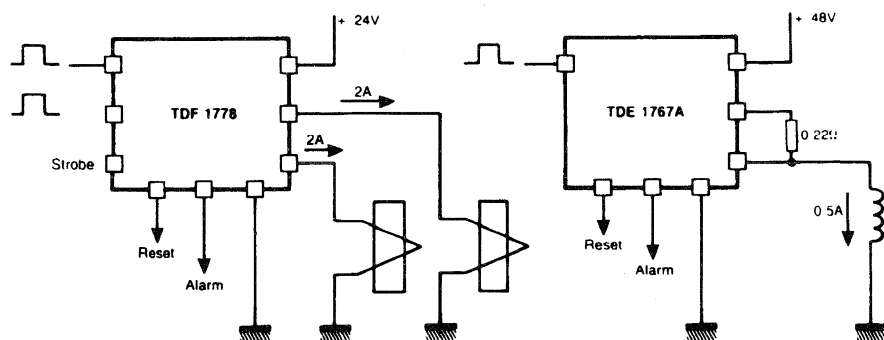
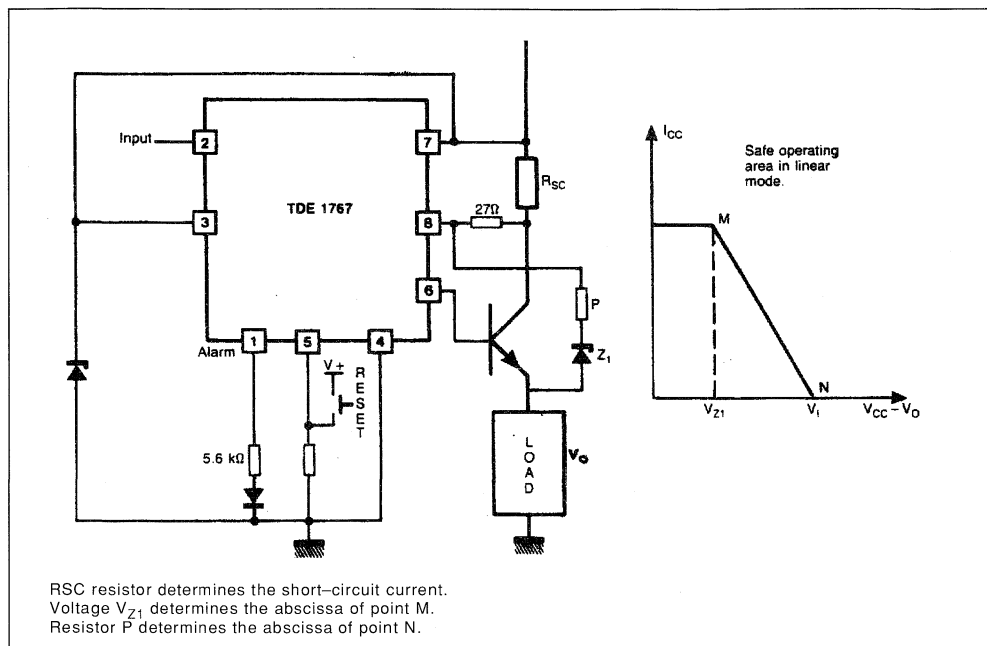
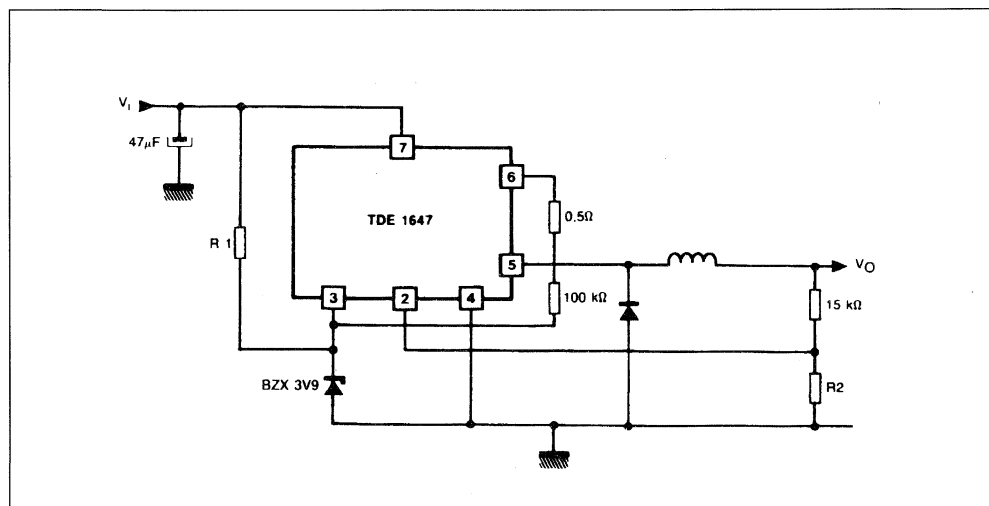
**Lamp driver****Small motor controller (constant torque breaking)****Electrovalve driver****Relay driver**

Figure 9 : TDE1767 Power Boosting.



VI (V)	R1 (KΩ)	R2 (KΩ)	VO (V)
+ 12	62	1.5	+ 5
+ 18	91	3.5	+ 12

Figure 10 : Voltage Step-Down Chopper.



INTERFACES DEDICATED TO PROCESSES CONTROL

By J.M. BOURGEOIS & L. PERIER

Controlling tasks are very common in many areas, for example the control functions associated with buildings, the factory automation control, the production and control of energy, the chemical industries...

These tasks are generally managed by process controllers or industrial micro computers linked to a supervisor and sometimes a dedicated computer. At the control level, sensors and actuators are the means of controlling the physical processes, and are monitored and driven by the process controller interfaces.

- 90% of system failures are due to the wiring or the sensors/actuators. Wiring may be reduced by the use of a field BUS and the distributed interfaces.
- Considering the remaining 10% of failures, 90% of them are due to the input/output interfaces.

Thus, if the reliability of the interfaces and the diagnostic functions are improved, the availability of the system increases (working time/working time + stopping time). A good means to achieve that is to use integrated self protected interfaces allowing a tele-diagnostic from the controller. The devices have integrated on the same silicon chip the safety and diagnostic functions and the power switch.

A better availability is achieved by mixing integrated interface with field BUS, decreasing the first 80% of errors, and the installation cost of the system.

A FAMILY OF INTEGRATED INTERFACES

The family of new circuits are dedicated to drive any type of inductive and resistive loads.

Their main characteristics are :

- * No indeterminate states up on power on.
- * Short circuit protection with the positive supply and ground by current limitation.
- * Over heating protection.
- * Protected against overloads.
- * Alarm output with delay.
- * Open ground protection.
- * Output voltage can be lower than ground for fast inductive load demagnetisation.
- * Differential input for universal logic compatibility.
- * Output paralleling capability.

Generally, hybrid or discrete circuits are used for these interface functions in process controller. Using integrated devices is cost effective and provides a better thermal protection because of the integration of the temperature sensor. As consequence, overload protection is totally reliable. Integrated interfaces are available in high side and low side configuration, for a range of current from 0.5A to 2A. They operate with a supply voltage range of + 8V to + 32V, a typical block diagram of one of these devices, the UAB/UAF 1780, is shown in Figure 1.

APPLICATION CIRCUIT OF THE UAB/UAF 1780

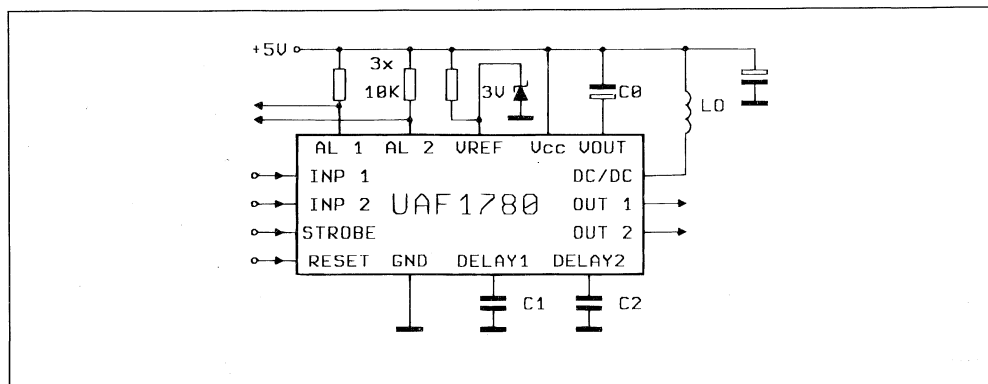
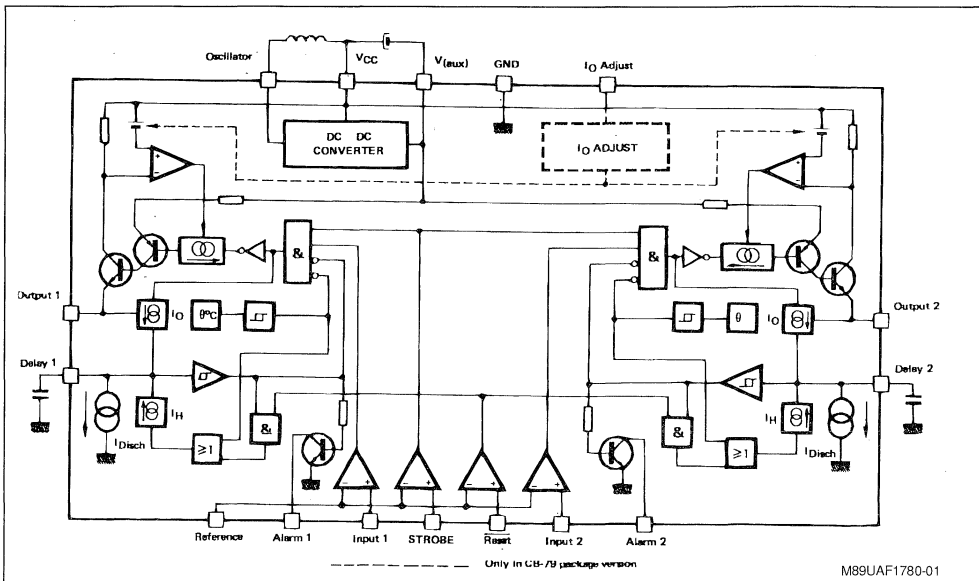


Figure 1 : UAF 1780 Structure.



APPLICATIONS

A local peripheral was designed for use by a micro computer or process controllers. The circuit uses four UAB/UAF 1780 which are dual integrated interfaces delivering up to 1A without heatsink and more than 2A with. The interfaces are driven and monitored by a Z86E11 micro controller whose UART allows the communication link with a serial field BUS.

Figure 2 shows the block diagram of the system.

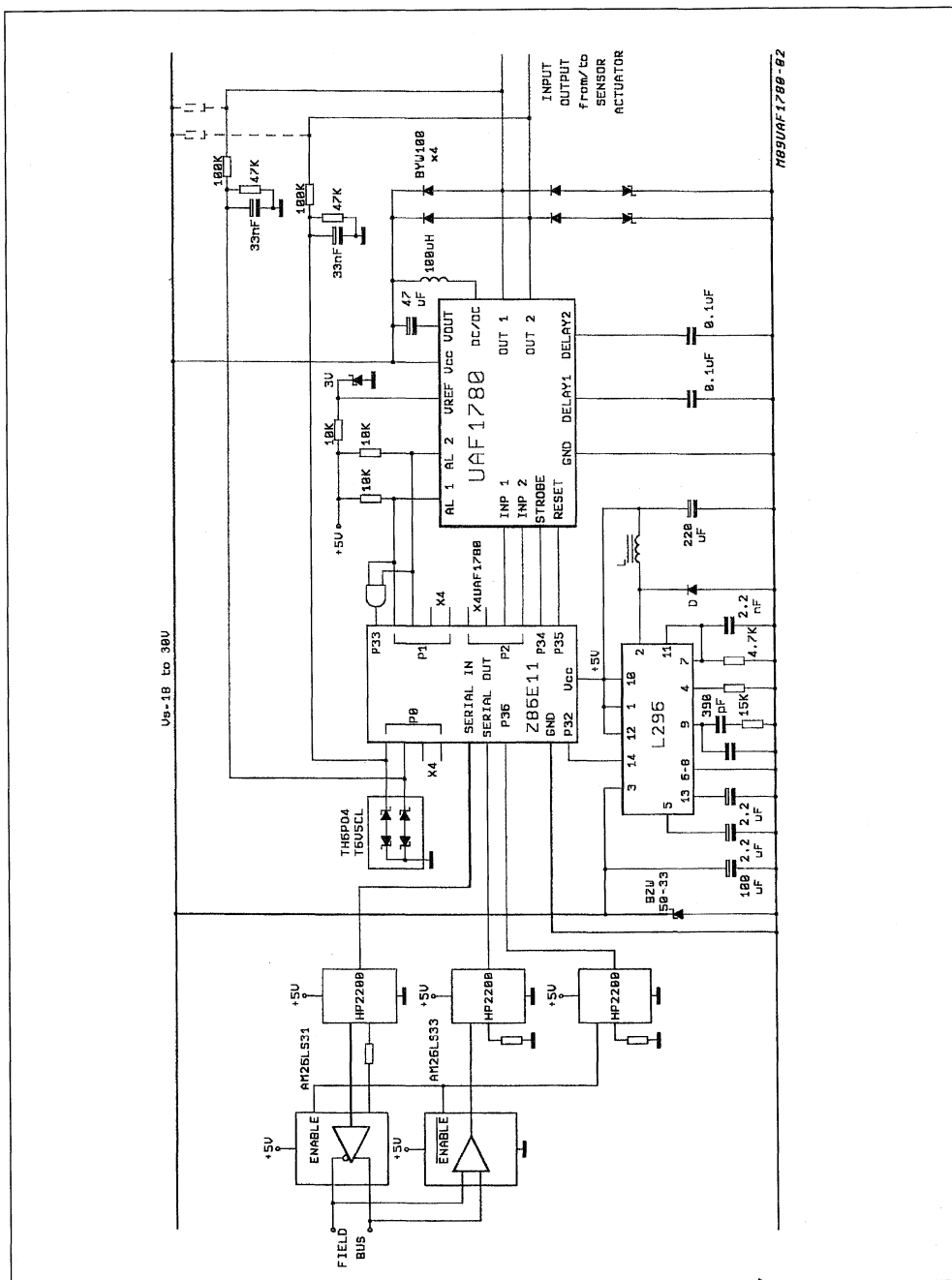
The configuration of the output of the integrated interface allows each output to be used as an input (via P_0) if desired. Only one of the four UAF 1780 is showed on the figure.

- In output configuration, the interface controls and monitors the load. The feedback signal to the port P_0 means that the state of the output can be monitored increasing the diagnostic capability
- In input configuration, the interface is off and the signals are read via the P_0 port.

List of items :

- * UAB/UAF 1780 : Intelligent full protected power switch
- * Z86E11 : 8 bits microcontroller
- * TRANSIL TH6P04T6V5CL : Octal protection zener in DIL package
- * L296 : High current switching regulator with reset output
- * AM26LS31 : High speed differential line driver
- * AM26LS33 : Differential line receiver
- * TRANSIL BZW5033 : Transcient voltage suppressors 5Kw/1msec
- * BYW100/100 : High efficiency ultra fast diodes $V_{RRM} = 100V$ $t_{rr} = 25/60nsec$ $V_f = 0.85V$

Figure 2 : Block Diagram of the Peripheral.



MAIN CHARACTERISTICS OF THIS PERIPHERAL

a) Inductive load demagnetisation :

The ability of the integrated interfaces output to sustain negative voltage up to 30V, provide a very fast demagnetization of inductive loads.

The size of the Zener diode depends on its voltage, the load current and the commutation frequency.

b) Noise and spike immunity.

The interfaces are supplied directly from the local 24V line. Because they withstand voltage spikes of up to 60V for 10ms, a transil is an effective protection for supply disturbances.

The outputs are protected by diodes connected to the ground and to supply to ensure the interface outputs are not subjected to parasitic voltage spikes.

c) Interrupt priority register.

—The first priority is given to the switching regulator L296 which warns the micro controller when there is an interruption in the supply volt-

age. This regulator provides simultaneously two auxiliary supplies one of which is isolated and used for the field BUS interface AM26LS31.

—The second priority is used for the communication with the host computer via the UART.

—The third priority is used to monitor the default signal of the UAF1780 interfaces.

d) Field BUS interface :

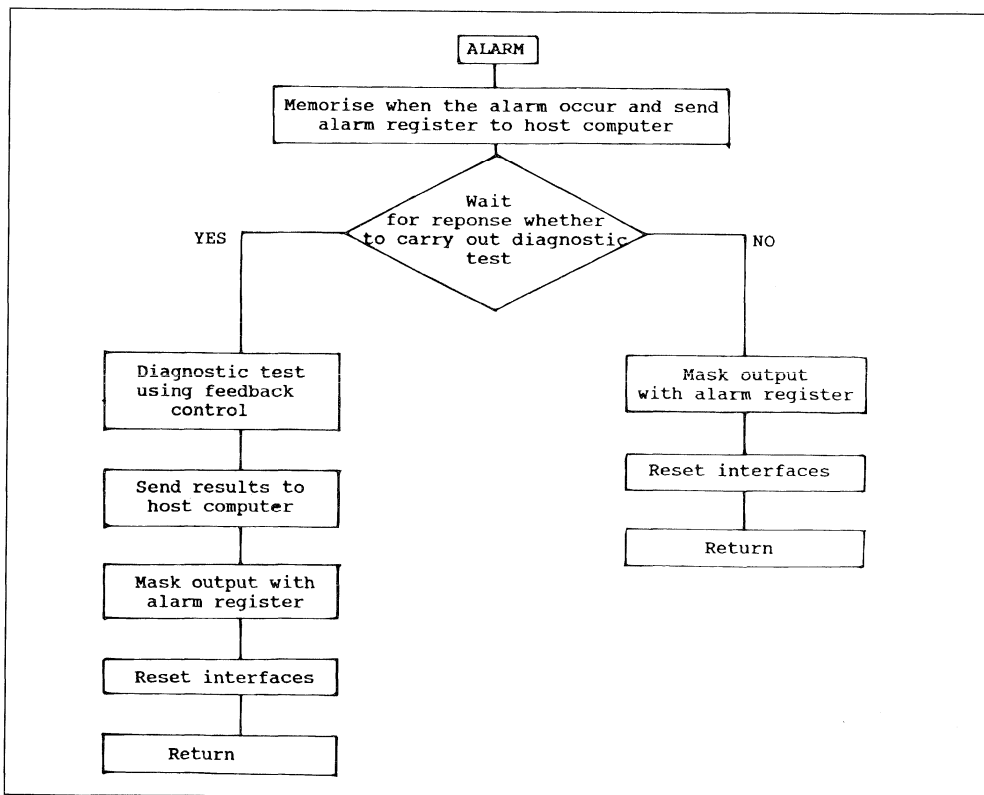
The galvanic isolation of this peripheral requires only three opto couplers because of the multiplexing of the INPUT/OUTPUT and alarm signal.

e) Efficiency :

The high efficiency of these integrated interfaces is due to an integrated DC/DC converter which reduces the on state voltage of the output Darlington stage.

DIAGNOSTIC CONTROL

When alarm output is enabled, the following processus is started.

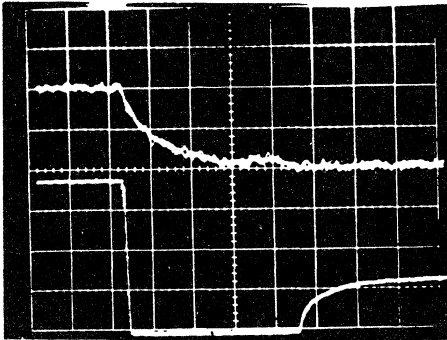


INTERFACE BEHAVIOUR

a) Inductive load.

Figure 3 shows the turn-off commutation with an inductive load, the demagnetisation zener diode used was 10V. This diode provides a current path for the load demagnetisation and a protection against negative spikes induced from in the wiring.

Figure 3 : I load : 0.4 A/div
V out : 10 V/div.

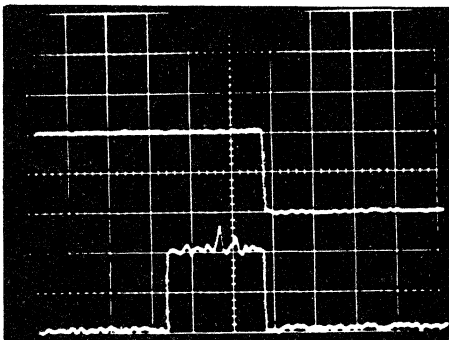


t : 20 msec/div.

b) Short circuit behavior :

Figure 4 shows the output current and the alarm signal in case of short circuit. The current is internally limited for a preset delay, after which a low level is applied on the alarm output and the current switched off. This device can be reactivated by the reset input.

Figure 4 : V alarm : 2 V/div
I load : 2 A/div.



t : 1 msec/div.

c) Over heating detection :

Figure 5 shows the output current and alarm signal in case of over heating detection. When the silicon chip reaches 150°C, the current is switched off and the alarm output activated. If the reset input is low, the switch restarts after the thermal hysteresis cycle and a preset delay. If the reset is high, the switch will remain off and the alarm low.

CONCLUSIONS

This family of integrated full protected interfaces provides more reliability in process control. Due to the alarm output, the real time diagnostic function can easily be multiplexed with a low cost micro controller.

The set of devices used for this application is optimized and provides a high immunity against all disturbances from the line voltage, the wiring and the loads.

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HIGH SIDE MONOLITHIC SWITCH IN MULTIPOWER-BCD TECHNOLOGY

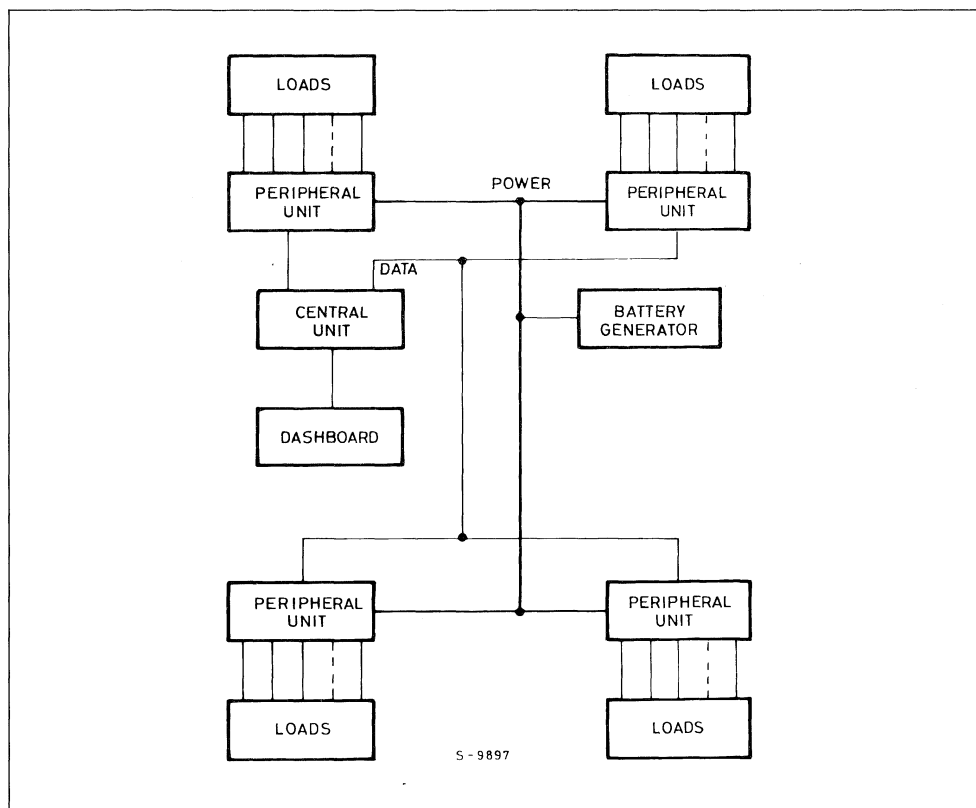
by C.Cini, C. Diazzi, D. Rossi, S. Storti

Recent advances in integrated circuit technology have allowed the realization of a new mixed process integrating isolated DMOS power transistors in combination with bipolar and CMOS signal structures on the same chip. Called Multipower-BCD, this technology has been used to realize a monolithic self-protected high-side switch mainly intended for automotive applications. Driven by TTL, CMOS input logic it can supply resistive or inductive loads up to 6A DC allowing a current peak of 25A with an $R_{DS(on)} = 0.1\Omega$. Fault conditions are signaled on a diagnostic output pin.

ELECTRONIC POWER SWITCHES IN THE CAR

The increase of the number of the electrical components in the car (today more than 50) and the increase in assembly costs shall soon make economical multiplexed power supply and control systems. These systems consist of a single line for power supply and a multiplexed signal network for control; in this way it is not necessary to have a wire for every load, but only a common power line and a common signal line for all the loads (fig. 1).

Figure 1 : Example of a Multiplexed System.



The control system is made, for example, with a central unit near the dashboard, for the user interface, a serial data transmission line and some peripheral units near the loads (fig. 2).

The multiplexed system not only makes it possible to reduce weight and overall dimensions of the cable harness, now critical in some places (e.g. the junction between the vehicle body and the doors), but, also makes it possible to have a bidirectional signal between peripheral units and the central unit without any extra line, this is useful for fault detection and, in a future, for data transmission to make a more complex informatic system.

Today the key problem, from the system engineering point of view, is data transmission whereas for

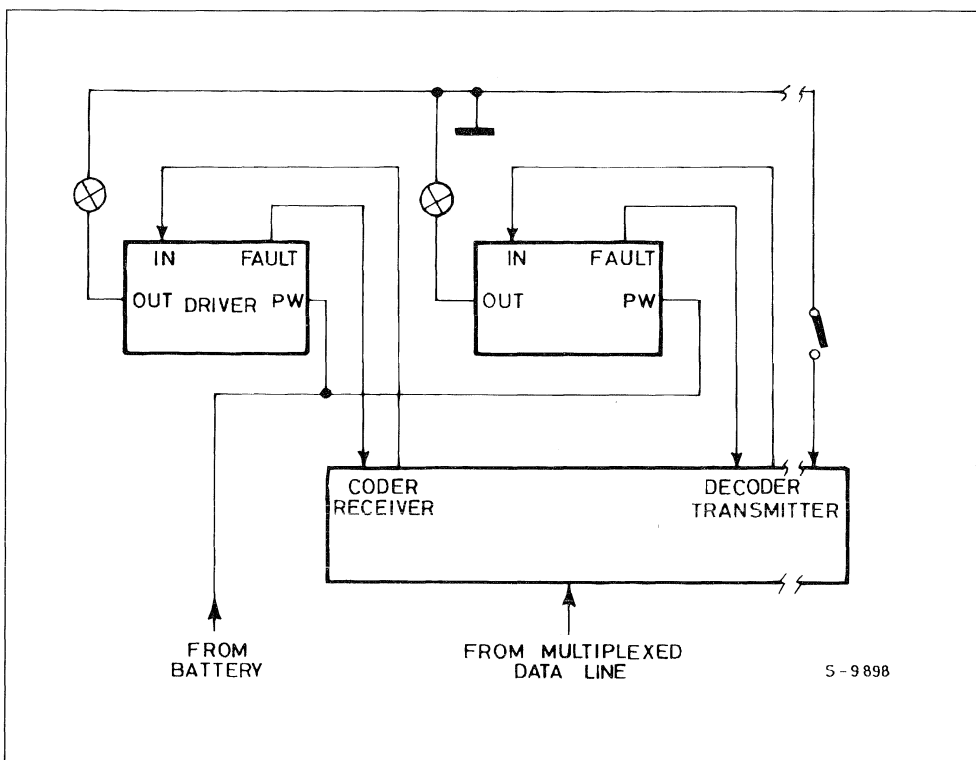
semiconductor technology the key problem is the electronic power switches.

The electronic switch, in addition to its main function, must be able :

- 1) to withstand a very high peak current (20A) with total battery voltage ($\approx 14V$) applied.
- 2) to protect itself, the power network and the load against overvoltages (load dump $\approx 60V$) and overload (protection with fuses is impractical),
- 3) to make some fault detections e.g. detect short circuit or open load condition.

For this reasons a simple electromechanic or electronic switch standing alone is not sufficient, a more complex circuit is necessary and for this the monolithic solution is the most effective.

Figure 2 : Block Diagram of a Peripheral Unit.



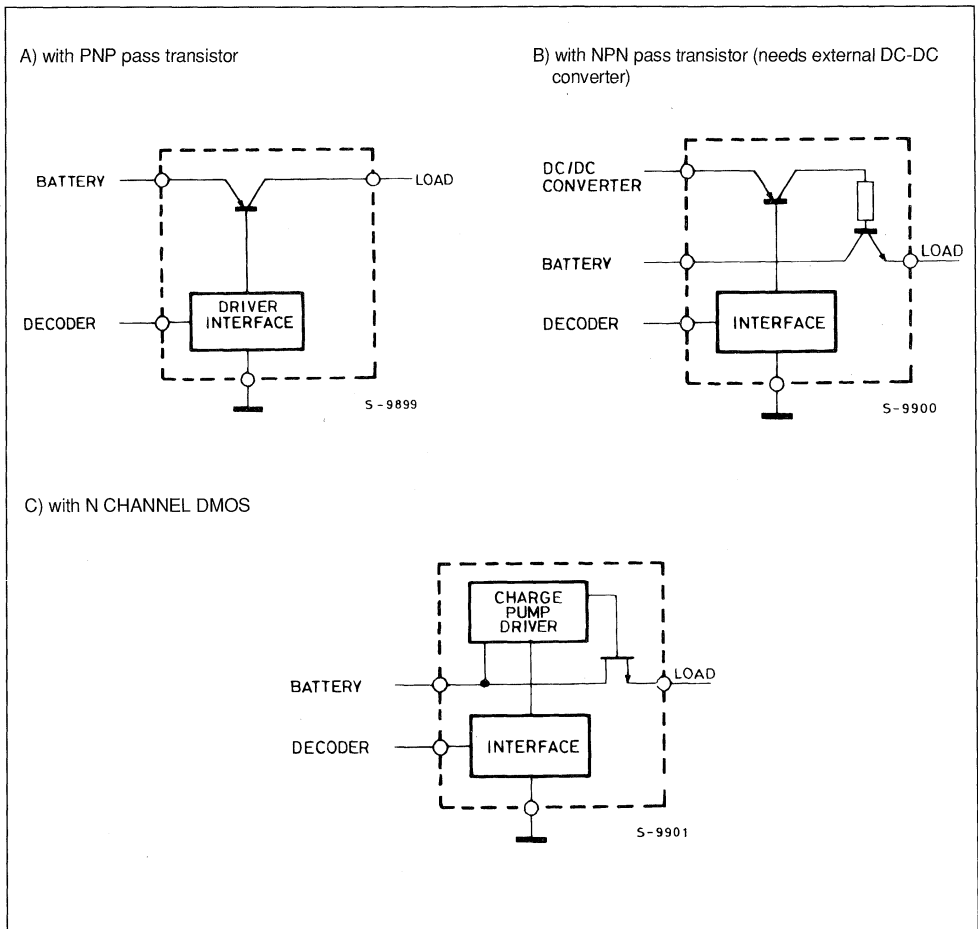
HIGH SIDE DRIVER

The problem of electrochemical corrosion is of primary importance in automotive systems because the electrical components are in an adverse environment (temperature, humidity, salt), for this reason the series switch is connected between the load and the positive power source. Therefore when the electrical component is not powered (that is for the greatest part of the lifetime of the car) it is at the lowest potential and electrochemical corrosion does not take place.

For this connection, components such as power PNP bipolar transistor or Power P-channel MOS would be integrated with low level signal circuitry

(fig. 3a), but this kind of element is less efficient and more difficult to realize than their complementary one. NPN bipolar transistors or N-channel MOS, if directly driven by the supply voltage, are not a good solution because the minimum voltage drop on the switch is V_{BE} or V_T (threshold voltage); the best solution is to have a driving voltage for the power transistor, higher than the positive supply. Nevertheless a power junction NPN transistor (fig. 3b) needs a certain amount of base current ($\beta = 10-60$ to have deep saturation) that could be obtained with a DC-DC converter; if centralized it complicates the power supply distribution network, if decentralized it complicates the peripheral unit always critical for size, reliability and cost.

Figure 3 : Possible High Side Drivers.



On the other side a POWER MOS N-channel (fig. 3c), being a voltage driven device, requires for the driving only a capacitive charge pump which can be fully integrated on the switch chip.

Bipolar transistors moreover need driving power and principally, are limited in maximum peak power by second breakdown.

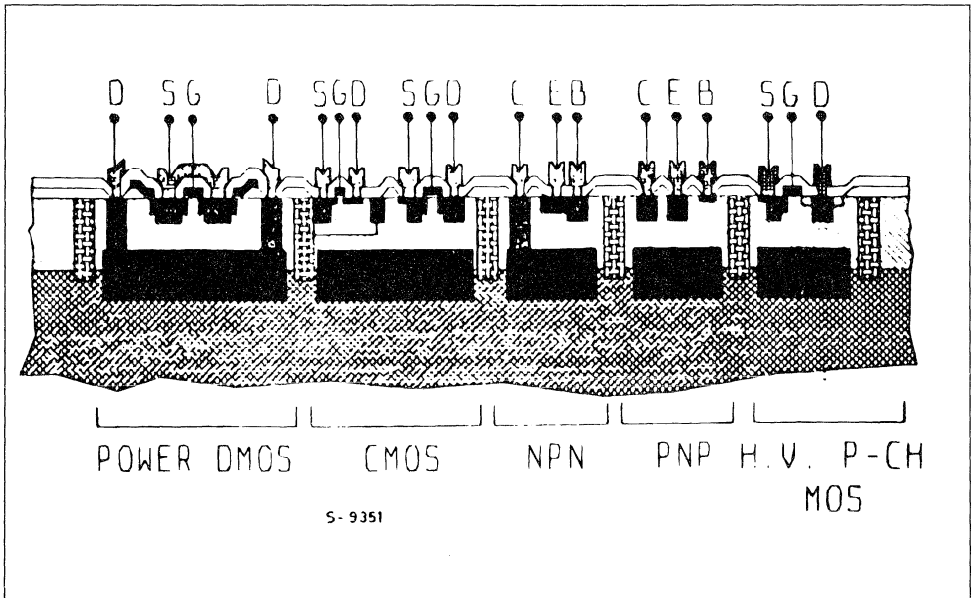
THE PROCESS TECHNOLOGY

For the realization of the device a mixed Bipolar-CMOS-DMOS process has been utilized. This process integrates the following components (tab.1) (Fig. 4) :

Table 1 : Devices in Multipower-BCD Technology.

VERTICAL D-MOS	$BV_{DSS} > 60V$	$V_{TH} = 3V$	$f_T = 1GHz$
P-CHANNEL DRAIN EXTENSION	$BV_{DSS} > 75V$	$V_{TH} = 1.9V$	$f_T = 200MHz$
C-MOS N-CHANNEL	$BV_{DSS} > 15V$	$V_{TH} = 0.9V$	
C-MOS P-CHANNEL	$BV_{DSS} > 15V$	$V_{TH} = 1.9V$	
BIPOLAR PNP	$V_{CEO} > 20V$	$\beta = 30$	$f_T = 10MHz$
BIPOLAR NPN1	$V_{CEO} > 20V$	$\beta = 30$	$f_T = 300MHz$
BIPOLAR NPN2	$V_{CEO} > 20V$	$\beta = 250$	$f_T = 1GHz$
BIPOLAR NPN3	$V_{CEO} > 20V$	$\beta = 250$	$f_T = 140MHz$

Figure 4 : A Schematic Cross Section of Bipolar, CMOS and DMOS Structures.



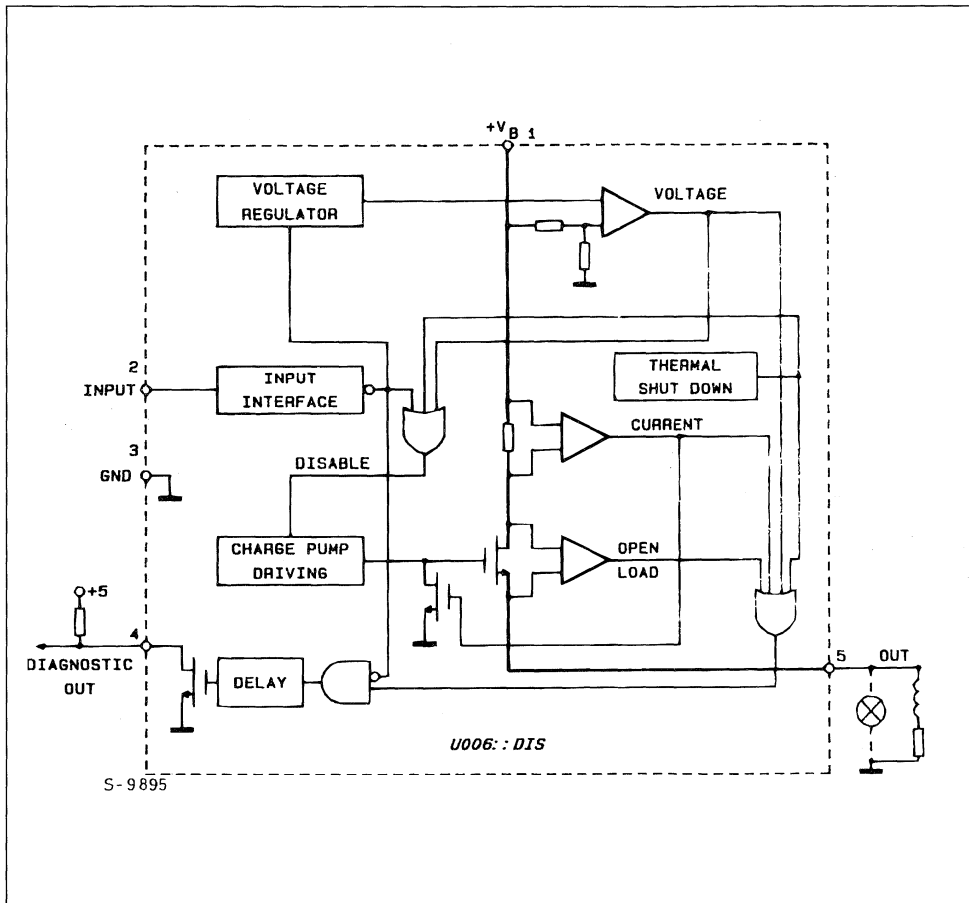
- N-CHANNEL POWER DMOS able to withstand $V_{DS} = 60V$ for the series element.
- BIPOLAR NPN AND PNP TRANSISTORS mainly employed in analog circuitry where low offset and high gain are needed e.g. voltage comparators and references, operational amplifiers.
- CMOS TRANSISTORS to realize a dense logic network with stand by currents practically negligible.
- PASSIVE COMPONENTS as resistors with a great variety of sheet resistivity ($30+8500\Omega/\square$)

to optimize both very high and very low resistive circuitry and gate oxide capacitors (e.g. to realize charge pump capacitors).

THE CIRCUIT

The circuit (fig. 5) is made by a power DMOS series element, a driving circuit with a charge pump, an input logic interface and some protection and fault detection circuits.

Figure 5 : Block Diagram of High Side Switch L9801.



THE POWER DMOS

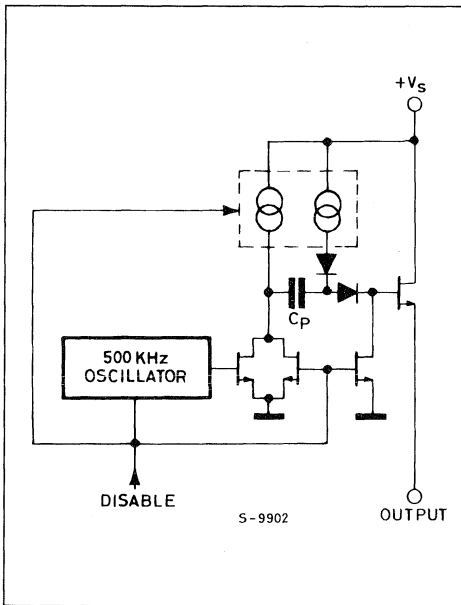
The power DMOS transistor is an array to 10,000 elementary DMOS cells that occupies an area of about 19,000 mils² and has a $R_{DS(on)} = 80\text{m}\Omega$ with $V_{GS} = 10\text{V}$. The low value of $R_{DS(on)}$ is required both to increase the power transferred to the load and to minimize the power dissipated in the device. In fact the switch must be operative also at very high ambient temperature (125°C) as required in automotive applications. For example to drive a 5A (60W) load, the drop on the switch is 400 mV and the dissipated power is 2W ($R_{th\text{-}j\text{-}case} 1.25^\circ\text{C/W}$).

THE CHARGE PUMP

The charge pump is a capacitive voltage doubler (fig. 6) starting from power supply (car. battery), driven by a 500 KHz oscillator.

The pump capacitor is an integrated 80 pF capacitor, the storage capacitor is the gate capacitance of the power itself ($\sim 500\text{ pF}$).

Figure 6 : Charge Pump.



INPUT INTERFACE

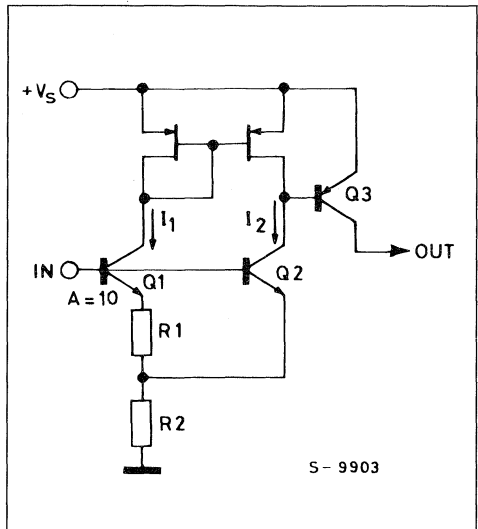
Considering the very wide operating temperature range ($T_j = 40$ to $+150^\circ\text{C}$) it is not possible to obtain the logic threshold from the conduction threshold of any elementary device, because of its temperature coefficient, respecting TTL input levels.

Nevertheless a solution with a voltage reference and comparator is not suitable because it needs a bias current flowing also when the device is in the OFF state.

This point is of great importance because the switches are directly connected to the car battery without the interposition of the ignition switch, thus also a little current ($> 50\mu\text{A}$) multiplied for the number of the switches (e.g. 50), causes an appreciable discharge current always flowing.

For this reason a threshold circuit has been designed derived from a well known voltage reference (fig. 7).

Figure 7 : Input Interface.



Fixed a threshold value $V_{IN} = V_{IN}^*$ for this value must be, by design $I_1 = I_2 = I_0^*$.

$$\text{if } \alpha = \text{area ratio} \quad \alpha = \frac{A_{Q1}}{A_{Q2}}$$

$$\text{must be} \quad I_1 = \frac{\Delta V_{BE}}{R_1}$$

$$(I_1 + I_2) R_2 + V_{BE}(Q2) = V_{IN}$$

$$\text{that is } V_{IN}^* = 2 \frac{R_2}{R_1} \frac{KT}{q} \ln \alpha + V_{BE} Q2$$

Reasoning around the threshold point it can be noted that the transconductance of Q2 is greater than the transconductance in Q1 branch (Q1 series R1).

For this

$$\begin{array}{lll} \text{if } V_{IN} > V_{IN}^* & I_2 > I_1 & Q3 \text{ ON} \\ \text{if } V_{IN} < V_{IN}^* & I_2 < I_1 & Q3 \text{ OFF} \end{array}$$

The choice of the values is made imposing :

- 1) $V_{IN}^* \equiv V_{BG} \equiv 1.250V$ band-gap voltage of silicon.

In this case V_{IN}^* is practically stable in temperature and centered respect TTL input levels ($V_{LMAX} = 0.8V$, $V_{HMIN} = 2V$).

The idle current I_{ABS} in the worst case, that is when $V_{IN} = V_{LMAX} = 0.8V$, $T_j = 150^\circ C$, it must be $I_{ABS} = I_1 + I_2 < 50\mu A$.

The proposed circuit has also a third working region : when $V_{IN} < V_{BE}$ $I_{ABS} = 0$ Q3 OFF

Observed that the TTL OUTPUT low level is V_{LMAX} 0.4V with practical driving circuits the idle current of this interface is zero : only at very high junction temperature ($V_{BE} < 400mV$) or with noise margin = V_{BE} 0.4V) this performance cannot be warranted.

The output of this circuit is useful to switch off not only the power DMOS, but also all the other circuits so that the idle current only the one of the input interface.

PROTECTION AGAINST OVERVOLTAGES

When the supply reaches the maximum operative voltage (18V) the device is turned OFF, protecting itself and the load ; moreover local zener clamps are provided in some critical points to avoid that V_{GS} of any MOS transistor could reach dangerous values even during 60V load-dump transistor.

PROTECTION AGAINST OVERLOAD

If the design of this device the peculiar inrush current of incandescent lamps must be considered, in fact.

- 1) When the tungsten wire is cold its resistance is about one tenth of the nominal steady state value (e.g. about 300mΩ for a 12V/50W lamp).
- 2) The decay time constant for the turn on extra-current of an incandescent lamp supplied with an ideal voltage source is on the order of some milliseconds.
- 3) A lamp powered with a constant current slightly higher than its steady state value has a turn on time on the order of 100msec. This time comparable with human reaction time is too much long for all flash-signalling devices.

The design choice has been to put a 20A current limit (that is $I_{max} = 5 I_{nom}$ for a 50W/12V rated lamp). This is a compromise between lamp turn on time

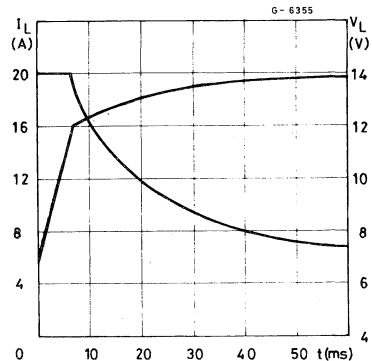
(40msec) and electric and thermal dimensioning of the device (fig. 8).

If the high current condition persists (e.g. load short circuit) and the junction temperature rises above $155^\circ C$ a thermal protection circuit turns off the device preventing any damage.

It must be noted that the power DMOS has no second breakdown, for this reason current limiting and thermal shutdown are sufficient to protect the device against any overload.

Some thermal hysteresis is provided to avoid a potentially critical condition (both current and voltage present during thermal shut down) for the POWER MOS.

Figure 8 : Lamp Current (I_L) and Voltage (V_L) vs. Time with 20A Current Limitation and 12V/50W Lamp.



FAULT DETECTION

When the device is driven and one of the protections (over temperature, overvoltage, overload) is present a fault detection open drain output turns-on. This output is active also when the drop on the POWER MOS is less than 80mV (that is $I_{load} < 1A$) detecting the open load (disconnected or burned-out).

When the device is off the fault detection circuits are not active and output transistor is turned off to allow a minimum quiescent current.

MOTOR AND INDUCTIVE DRIVING

This device can drive unipolar DC motors and solenoids as well, in fact it can recirculate an inductive current when the output voltage goes more than a threshold lower than ground. The possibility to have a high start-up current is useful also for DC motors.

CONCLUSION - FUTURE DEVELOPMENTS

A process allowing the integration of power DMOS, CMOS and BIPOLAR transistor makes possible the construction of a monolithic switch comprehending also protection and fault detection functions.

The power DMOS approach allows also the possibility to make a large range of power switches with different ON resistance and current capability only scaling proportionally the power area.

Moreover the CMOS structures can be utilized to make also the coder/decoder circuit to interface directly the transmission line.

Those features and the possibility to integrate more than one power element on the same chip makes possible, in a near future, the integration of the whole peripheral unit.

DRIVE CIRCUIT FOR AN ELECTRIC FUEL CUT-OFF VALVE

INTRODUCTION

The circuit described in this application note has been designed to drive the solenoid of an electric valve. The solenoid has the following characteristics:

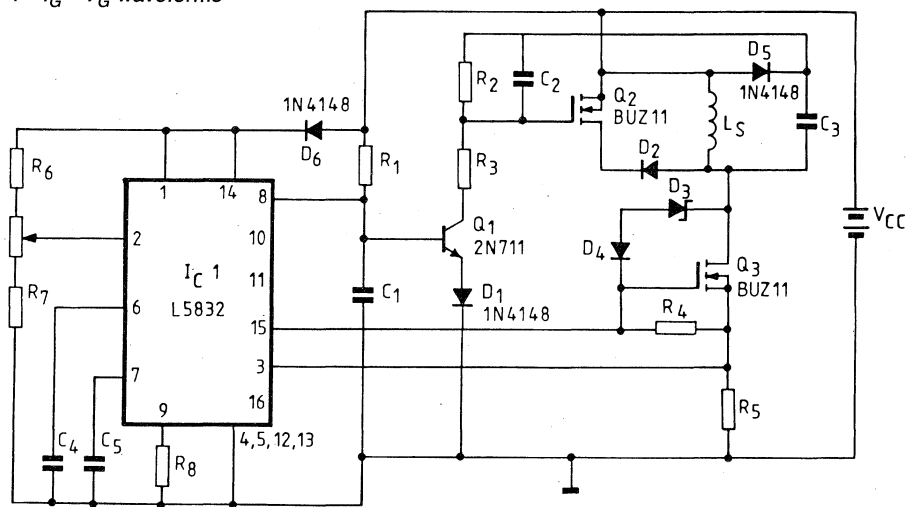
L_S	=	2mH @ 1 KHz
R_S	=	0.62 Ω
I_{pull}	=	38A per 100msec
I_{hold}	=	5A

CIRCUIT DESCRIPTION

The problem this circuit, figure 1, sets out to resolve is to produce an initial current peak of 38A for 100 milliseconds followed by a continuous reduced holding current of 5A.

This design note uses the features of the L5832 together with two external power transistors, both the peak and the holding current level are regulated by the switchmode circuitry of the L5832. The

Fig. 1 - $I_G - V_G$ waveforms



SU-1473

COMPONENT LIST (See Fig. 1)

C1	4.7nF	D3	$V_Z = 24V, 1W$	R5	0.01 Ω
C2	15nF	I_{C1}	L5832	R6	15K Ω 1/2W
C3	1 μ F	P1	100 Ω	R7	56 Ω 1/2W
C4	8 μ F	R1	470 Ω 1/2W	R8	1.2K Ω 1/2W
C5	27nF	R2	100 Ω 1/2W	Q1	2N1711
D1-D2-D5-D6	1N4148	R3	68 Ω 1/2W	Q2-Q3	BUZ11 or STVHD90
D2	BYV52PI-50	R4	470 Ω 1/2W		

Fig. 3 - Simplified driving of Q2

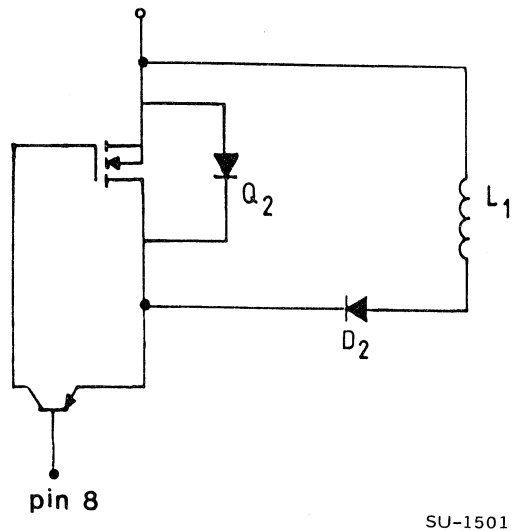


Figure 4

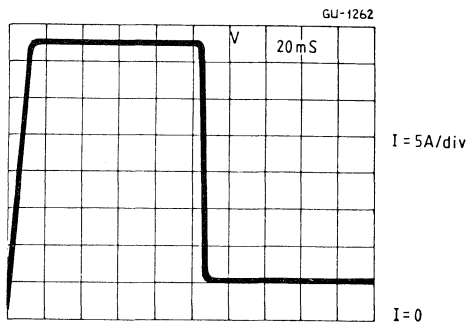
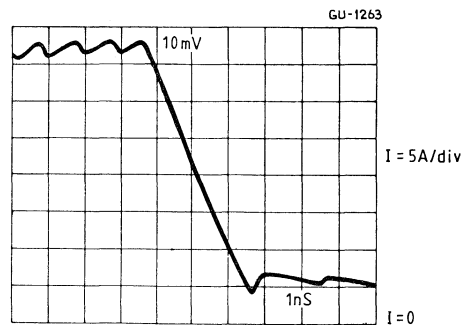


Figure 5



The power lost in power devices is:

At 38 Amp (I_{pull})

$$P_{Q2} = 2 \times 38 = 76W$$

$$P_{D2} = 0.8 \times 38 = 30.4W$$

$$P_{Q3} = 2 \times 38 = 76W$$

}

per 100msec.

At 5Amp (I_{hold})

$$P_{Q2} = 1.2 \times 5 = 6W$$

$$P_{D2} = 0.8 \times 5 = 4W$$

$$P_{Q3} = 0.4 \times 5 = 2W$$

FROM RELAYS TO INTELLIGENT POWER SWITCHES

by L. WUIDART

INTRODUCTION

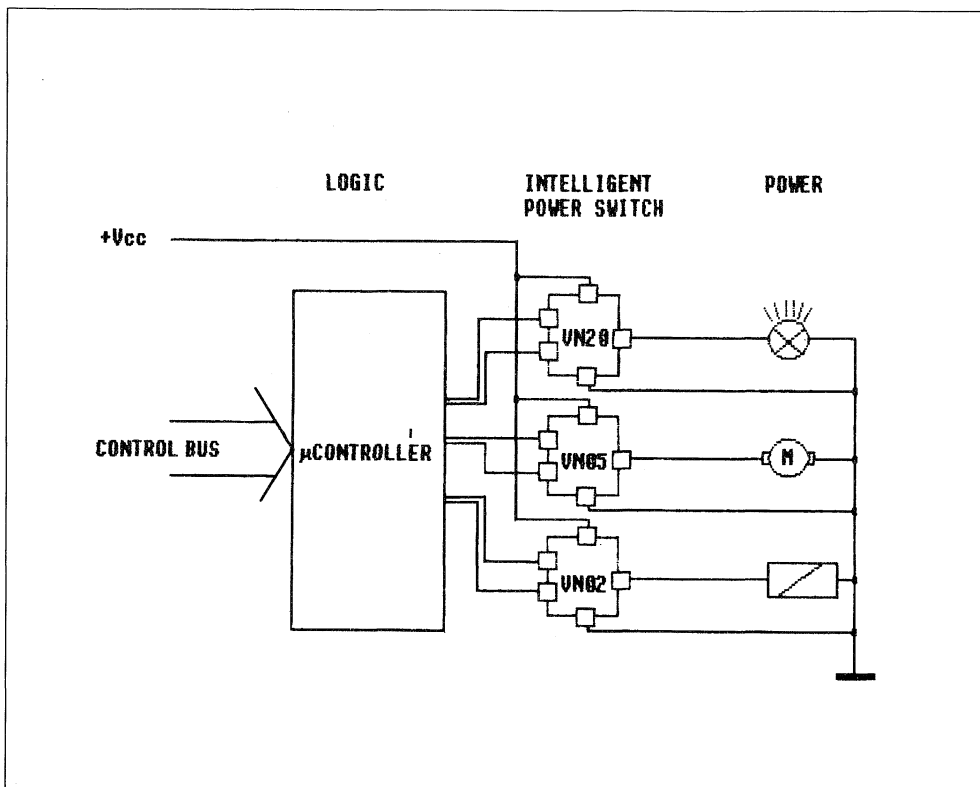
The advent of new "smart power" technologies on the electronics scene provides the electronics industry with an integrated power transistor and its control and protection functions on a single silicon chip [1] [2].

These Intelligent Power Switches, IPS, reduce the

number of discrete electronic devices required in circuits by direct interfacing between the control logic and the power load to be driven [5] [6], figure 1.

Besides control of electrical loads, Intelligent Power Switches can : protect themselves, detect abnormal operating conditions (openload, short circuits...) and send back information on load state to a microcontroller.

Figure 1 : IPS Interfaces Between Control Logic and Power Load.



INTERNAL STRUCTURE

The integrated power switch is a vertical N-channel, DMOS transistor (VDMOS). Its current capability (I_D) is related to its on-resistance (R_{on}). A family of

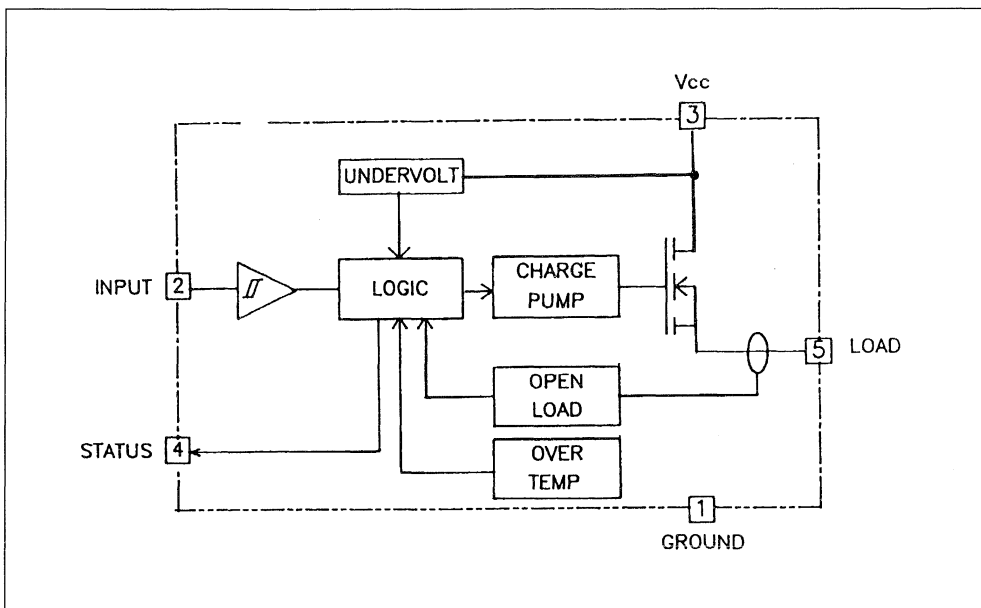
"highside" relays (see figure 2) with the same functional blocks have been built with currents ranging from 2 to 30Amps, see figure 3.

Figure 2 : "High Side" Relay Family Current Capability ($T_c = 25^\circ\text{C}$ and $V_{CC} = 13.5\text{V}_{DC}$).

Device	V_{DSS} [V]	I_D [A]	R_{on} [mOhm]
VN02	60	2	500
VN05	60	5	200
VN20	60	20	50
VN30	60	30	30

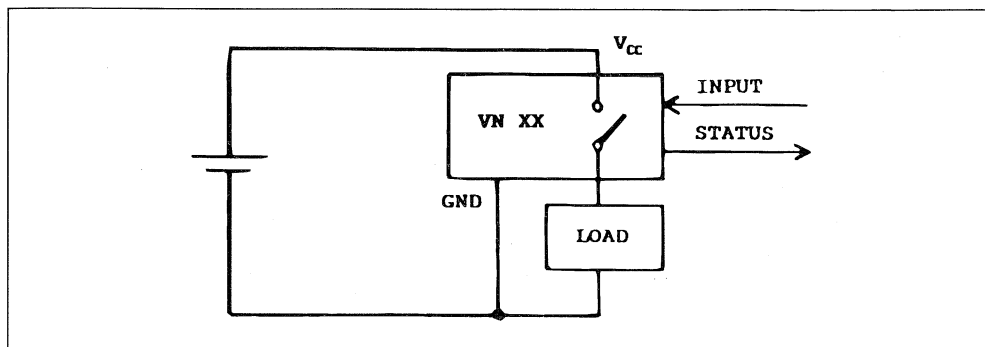
An obvious advantage of these switches over simple relays is that they can be driven by a CMOS/TTL compatible signal referenced to ground. They also feature built-in over temperature protection, over current limiting, under voltage and

load disconnection detection. Additionally, they indicate these abnormal operating conditions on the output status by switching the output status flag low. The maximum breakdown voltage of this family of VIPower devices is $60\text{V}(V_{DSS})$.

Figure 3 : VN02 VIPower Family Block Diagram.**"High Side" CONFIGURATION**

For safe practice, it must not be possible to activate the load by accidentally shorting the load to the frame of the equipment or body of the car. For this reason,

loads must be ground connected - figure 4. Consequently, the VN02 family power switches have to be placed between the positive line and the load.

Figure 4 : High Side Configuration.

SELF PROTECTION AND DIAGNOSIS

OVERTEMPERATURE PROTECTION

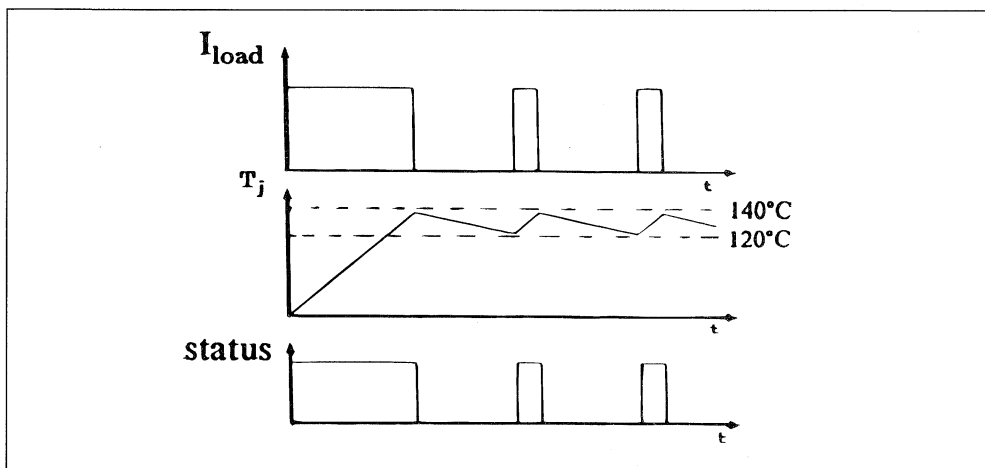
These IPS have to work within a temperature range of - 40°C to 105°C in order to comply with the demands of both industrial and automotive applications. [3] [4].

To avoid destruction from excessive dissipation under abnormal operation, the over temperature protection turns the integrated power transistor off

at a typical junction temperature of 140°C. When the temperature comes down again to 120°C, the power switch is turned back on.

When the VN02 family are permanently overloaded, they maintain a junction temperature between 120°C and 140°C by a succession of ON/OFF states (figure 5).

The "status" output indicates a fault condition when the temperature protection is operating.

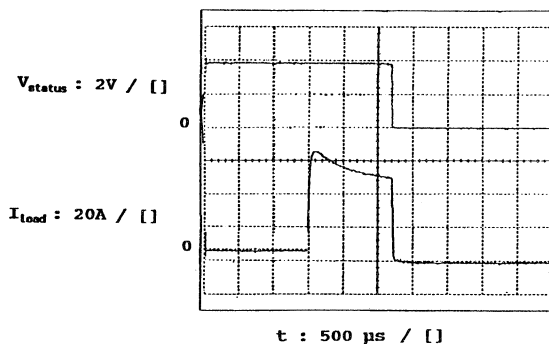
Figure 5 : VN20 Temperature Protection in Operation.

SHORT-CIRCUIT PROTECTION

Short-circuit and intermittent overloads are self-limited to the Intrinsic saturation current (I_{lim}) of the integrated power VDMOS transistor.

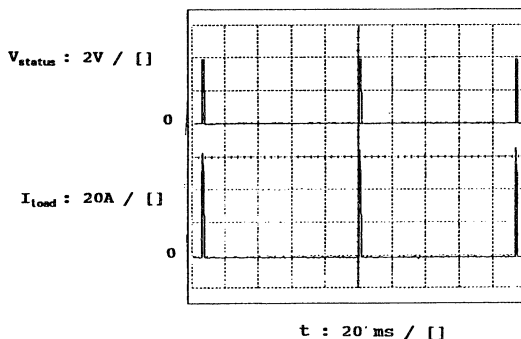
If a short circuit is permanent, the power switch simultaneously withstands the supply voltage (V_{cc}) and

the saturation current (I_{lim}) - photograph 1. Under these conditions the IPS heats up very quickly. As soon as the temperature protection turns the switch off. When the switch cools down to 120°C it turns on again.

Photo 1 : Current during Short Circuit in an VN20.

During a permanent short-circuit, these devices are alternately ON then OFF with a frequency determined by their ability to dissipate heat.

This is typically between 5 and 10Hz - see photograph 2.

Photo 2 : Thermal Cycling during Permanent Short Circuit Conditions for an VN20.

The VN20 family can also detect an open load. This may occur as a result of lamp filament failure, or during accidental disconnection, i.e. intermittent connections. The "status" output indicates an open load when the load current drops to a tenth of its nominal value.

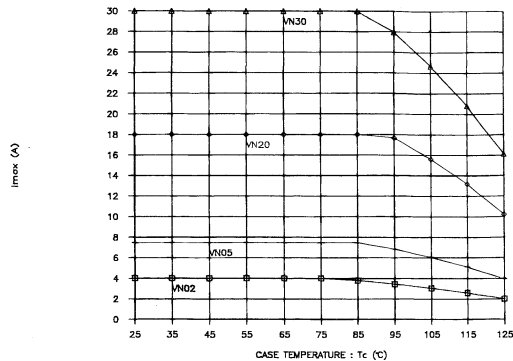
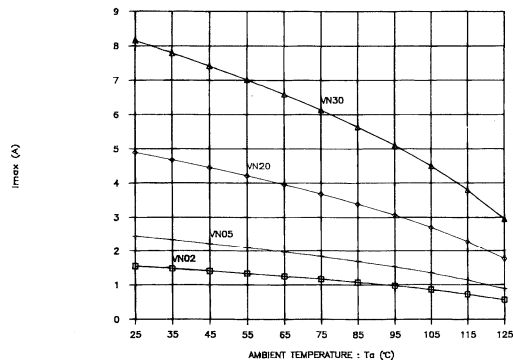
UNDER VOLTAGE LOCKOUT

This IPS failly can withstand large supply voltage variations from 6.5V to 60V.

ENVIRONMENT

OPERATING TEMPERATURE

The ambient operating temperature in certain equipment can rise above 85°C. The maximum DC current without thermal shutdown (I_{max}) is mainly related to the case temperature (T_c) and consequently to the ambient temperature and its ability to dissipate heat, see figures 6a and 6b.

Figure 6a : Maximum DC Current (I_{max}) versus Case Temperature (T_C).**Figure 6b :** Maximum DC Current without Heatsink versus Ambient Temperature.

TRANSIENTS AND PROTECTION

Transients are mainly due to other switches operating on the same supply line. They are mostly positive or negative over voltage transients with respect to the supply line.

For automotive applications ISO TR7637 [7] defines the main wave-form parameters of these transients giving enough information for them to be simulated.

THE "LOAD DUMP"

This is a high energy transient due to battery disconnection whilst the alternator is generating.

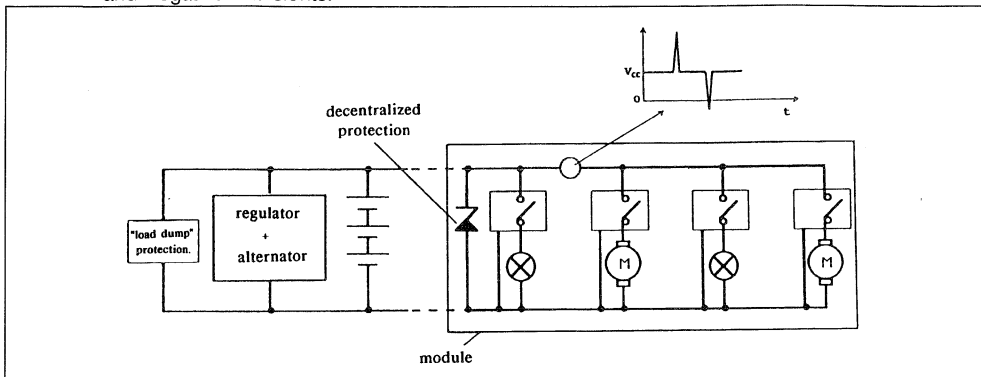
A protection diode especially dedicated to clamp this

load dump can be put close to the alternator and its regulator [3]. The breakdown voltage (V_{BR}) of this clamping diode must be at least twice the battery voltage ($V_{BR} > 26V$) to allow jump starting with 2 batteries in series - a condition + encountered in the automotive industry.

THE "REMAINING TRANSIENTS"

Each VN02 family member is internally protected against reverse current through the ground connection. Consequently, one single clamping diode between V_{CC} and ground is sufficient to protect a module of several IPS devices against positive and negative transients - figure 7.

Figure 7 : Clamping Diode Protecting a Module of Several of the VN02 Series Devices against Positive and Negative Transients.



These decentralized protection diodes cannot withstand the "load dump" transient. Their breakdown voltage (V_{BR}) must be greater than the clamping voltage of the "load dump" protection. The protection hierarchy must therefore be :

$26V < V_{BR} \text{ (load dump diode)} < V_{CL} \text{ (load dump diode)} < V_{BR} \text{ (decentralized diode)}$.

LINE INDUCTANCES

The parasitic wiring inductances generate supply line disturbances.

These parasitic "line inductances" are in the order of $1\mu H$ per metre of automotive wiring harness.

TURING ON

At the turn on of an IPS, the local supply voltage (V_{local}) can drop several volts because of line induct-

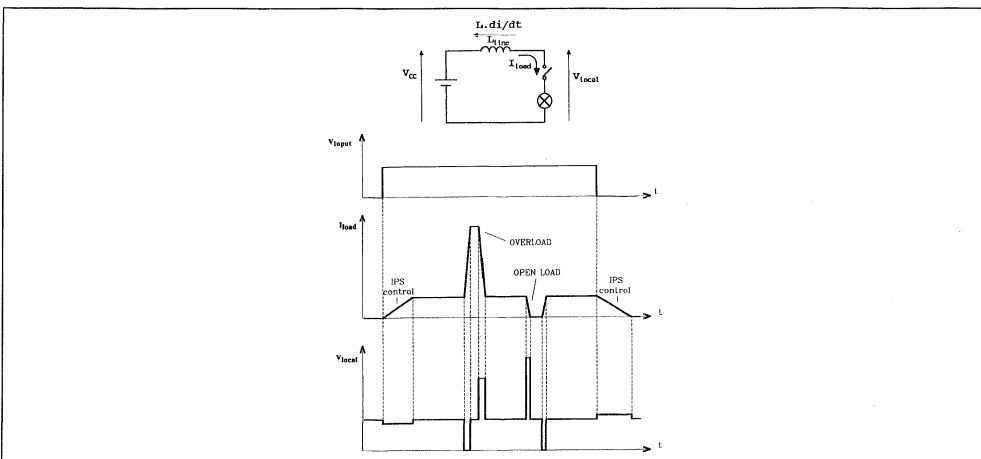
ance. This inductive voltage drop could cause the IPS to turn off again due to the under voltage lock-out, especially if the supply voltage was low. This in turn could produce oscillations which disturb the IPS control.

In order to avoid these oscillations, each VN02 family member internally limits di/dt during switching, figure 8, enabling a line inductance of about $20\mu H$ for a $24V_{DC}$ supply voltage or $8\mu H$ for $13V_{DC}$.

$$L_{line}(\mu H) \leq \frac{V_{cc}(V) - 6,5}{0,8 (a/\mu s)}$$

A small resistive load, less than 1Ω , represent the worst case voltage drop, since any inductive load, even small, will slow down the rate of rise of the current.

Figure 8 : Control of the Switching di/dt by the VN20 with Intermittent Load Variations.



ON STATE

During the on-state, intermittent load variations can occur due to bad connections or open loads. These intermittent current variations cause, through line inductance, over voltages which can exceed 100V.

One single clamping diode is sufficient (cf : transients and protection) to protect a module of several IPS devices against these over voltages, figure 8.

BEHAVIOUR WITH DIFFERENT TYPES OF LOADS

RESISTIVE LOADS

The automotive bulbs are a very typical example of

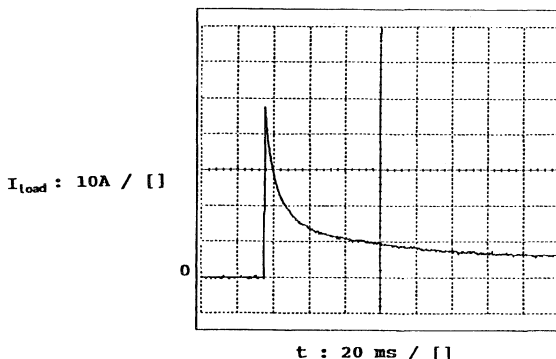
resistive load. The inrush current (I_{inrush}) of a cold bulb can be up to 10 times its nominal value at operating temperature. The VN02 family conducts the full inrush current, exactly as you would expect in a conventional switch. For this reason, there is no additional visible delay in the initial illumination of the lamp.

A voltage drop of less than 300mV (nominal current) can be obtained with a VN02 family device whose saturation current is generally greater than the bulb's inrush current, figure 9.

Figure 9 : Bulbs with Corresponding VIPower IPS. Currents and Voltages at 25°C and $V_{cc} = 13.5V$.

Bulb (W)	I_{inrush} (A)	$I_{nominal}$	VNxx	Drop Voltage (mV)	I_{lim} (A)
5	6	0.4	VN02	125	14
21	24	1.8	VN05	260	28
60	58	5.6	VN20	260	80

Photograph 3 : Inrush Current of a 60W/H4 Automotive Bulb with VN20.



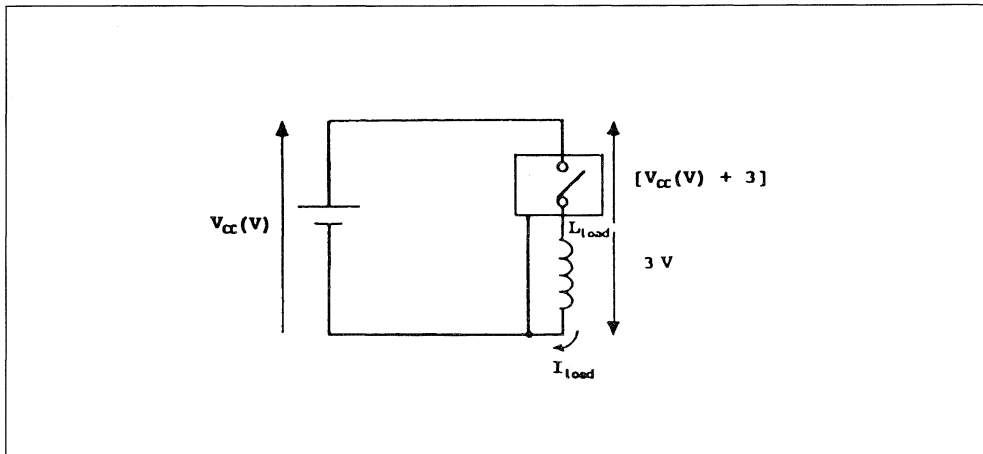
INDUCTIVE LOAD

All relay, valve and injector coils are inductive loads. At turn off, a magnetized inductive load generates a negative potential on the IPS output pin. The internal function of the VN02 family ensures the de-

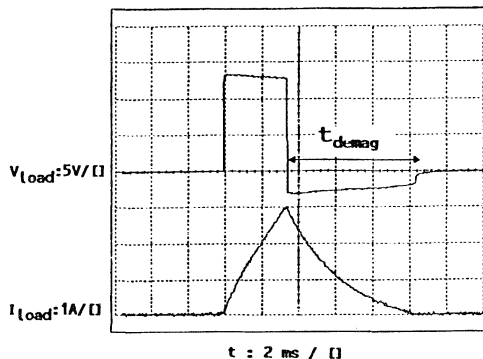
magnetization of these inductive loads with a typical voltage (V_{demag}) of - 3V.

As soon as the IPS turns off, the load current and the increased supply voltage ($V_{\text{cc}} + 3\text{V}$) are simultaneously applied to the switch terminal, figure 10 and photograph 4.

Figure 10 : Inductive Load Demagnetization Turn-off for the VN02 Family.



Photograph 4 : 15mH Inductive Load Demagnetization at Turn-off with 13V_{DC} Supply Voltage for a VN20.



During repetitive operation, the inductive load demagnetization causes power dissipation P_{demag} in the chip, increasing the silicon temperature up to thermal shutdown.

$$P_{\text{demag}} = 0.5 L_{\text{load}} \cdot [I_{\text{load}}]^2 \cdot \frac{[V_{\text{cc}} + V_{\text{demag}}]}{V_{\text{demag}}} \cdot f$$

f = the switching frequency.

For each member of the VN02 family, we have :

$$P_{\text{demag}} \approx C \cdot L_{\text{load}} \cdot [I_{\text{load}}]^2 \cdot f$$

where $C = 2,8$ for $V_{CC} = 13$

and $C = 4,5$ for $V_{CC} = 24V$.

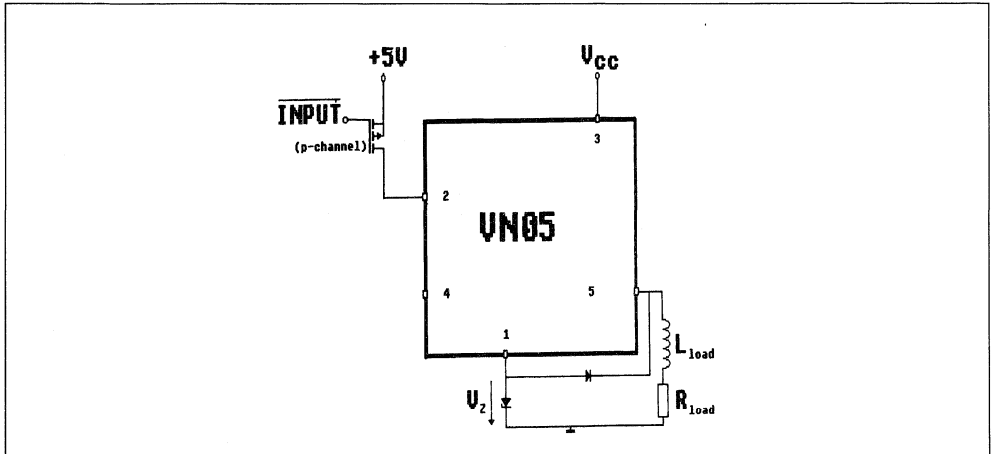
An external freewheeling diode prevents the demagnetization energy from being dissipated through the IPS. However, this increases the demagnetization time considerably.

$$t_{\text{demag}} (\text{with diode}) \approx \frac{3}{V_F} \cdot t_{\text{demag}} (\text{without diode})$$

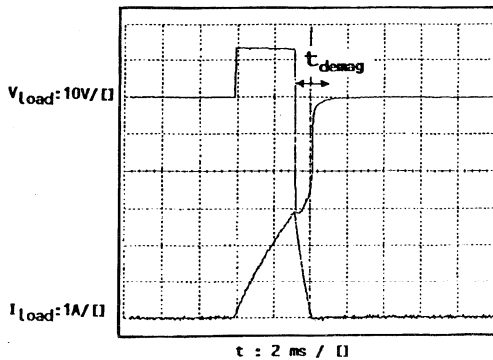
V_F = the freewheeling diode threshold.

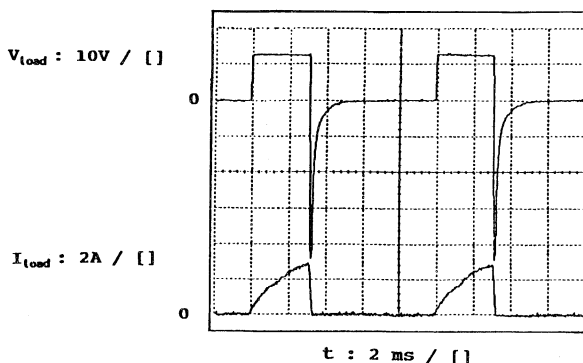
An alternative method using one of the VN02 family devices and several discrete devices is shown in figure 11. This enables fast demagnetization at a higher voltage. This voltage can be set with a zener diode, V_Z . This greatly reduces the power dissipation in the IPS, see photograph 5a and 5b.

Figure 11 : Fast Demagnetization Diagram of an Inductive Load, Valid for all the VN02 Family.
(conditions : $V_Z + V_{CC} < V_{DSS}$).



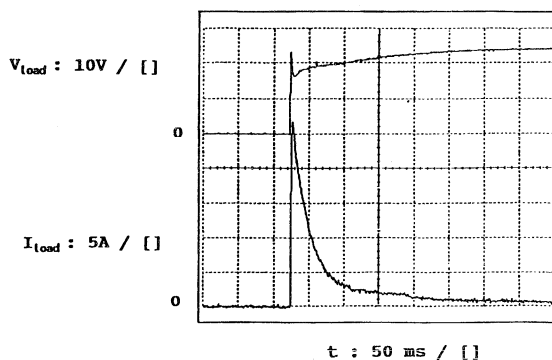
Photograph 5a : 30V Fast Demagnetization of a 15mH Inductive Load with a VN05. ($V_{CC} = 13V_{DC}$).



Photograph 5b : 40V Demagnetization of 4 Paralleled Injector Coils with VN05. ($V_{CC} = 13V_{DC}$).**MOTORS**

DC Motors are mainly used in industrial ($V_{CC} = 24V$), and automotive ($V_{CC} = 12V$) applications such as : pump motors, cooling fan motors, stepper motors, etc...

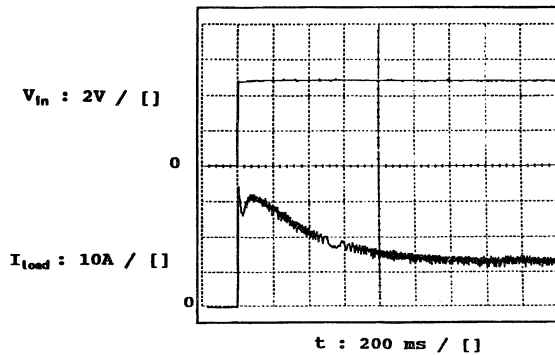
DC Motor inrush currents are also very important. The inrush current of a 50W/24 V_{DC} stepper motor can be as high as 25A ! - photograph 6.

Photograph 6 : Inrush Current for a 50W/24 V_{DC} Stepper Motor Using VN05.

A 150W cooling motor fan draws up to 30A at start-up, - photograph 7.

As is the case for bulbs, (cf : resistive load), the VN02 family will start a motor without limiting it's inrush current.

Photograph 7 : Inrush Current for a 150W/12V_{DC} Cooling Motor Fan Using VN05.



CONCLUSION

The VN02 family are an attractive alternative to conventional electromechanical relays, as much in industrial as in automotive or consumer applications.

Solid state monolithic devices wipe out several drawbacks associated with electromechanical relays.

- The number of switching cycles is unlimited.
- Their package is basically PCB washable.
- They switch high currents without using prohibited materials such as cadmium.

- They are space saving.

More than simple solid state relays, these devices are self protected and provide load status information. The whole of the VIPower VN02 family, VN02/05/20/30, are very easy to use since you can control up to 100A with simply a TTL/CMOS compatible signal.

The use of these new Intelligent Power Switches reduces the number of discrete components whilst greatly increasing system reliability.

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AN ISOLATED INTEGRATED DRIVER FOR POWER MOSFETS USING THE VB300 VIPOWER I.C.

by R. Letor

The VB300 is a monolithic ac to dc converter primarily designed to drive capacitive input power devices, n-channel Power MOSFETS and HIMOS (IGBT). Two integrated capacitors provide input to output isolation of 370V dc. The device is supplied in an 8 pin minidip package.

The device has been designed primarily for telecommunication applications where together

with two Power MOSFETS it forms a noise free solid state relay capable of switching ac or dc loads, see fig. 1. The VB300 has been designed specifically for its low distortion feature — essential in telecommunication equipment. The current capability of such a solid state relay depends solely on the Power MOSFETS used in the design.

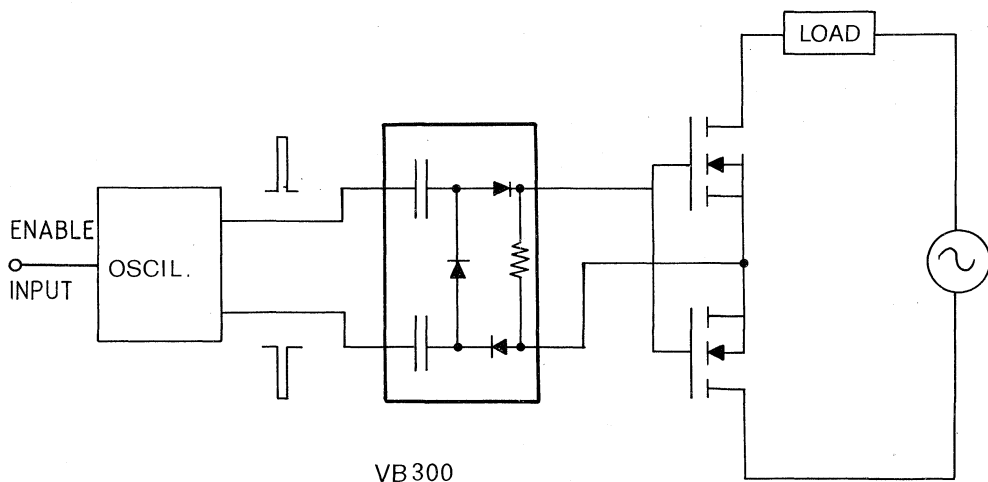


Figure 1. VB300 typical application

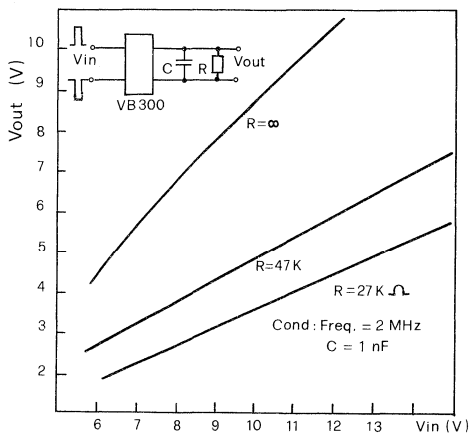


Figure 2. Transfer characteristic as a function of R_o

The transfer characteristics are illustrated in figure 2 while figure 3 and 4 show the dc output voltage versus input pulse amplitude and input signal frequency. The input gate capacitance of the Power MOSFETS used will affect the switching speed achieved by the VB300, ($Q=it$). This can be varied by choice of input signal amplitude and frequency and the use of an external gate source resistor network. Figure 2 shows how the output voltage varies as a function of the load resistance, R_o .

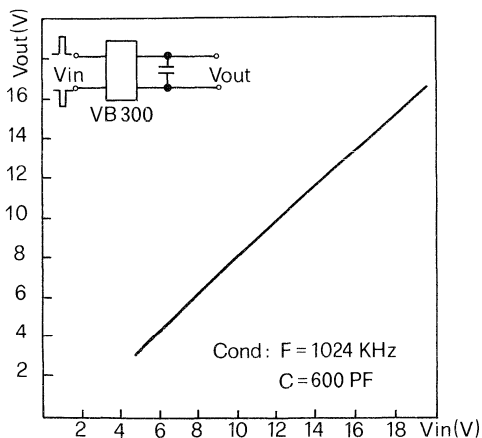


Figure 3. DC output voltage vs input pulse amplitude

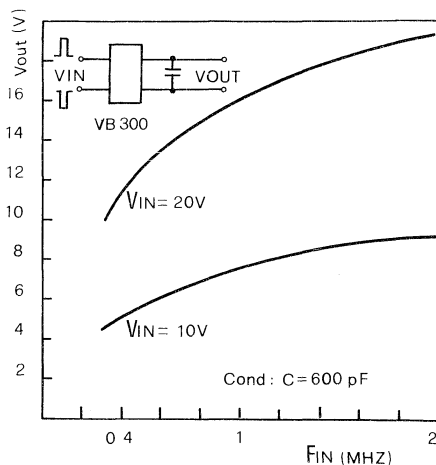


Figure 4. DC output voltage vs input signal frequency

The VB300 is not limited to solid state relay applications. It can be used in a variety of other situations. For example it could be used in automotive actuator circuits as a high side driver, figure 5. Figure 6 shows in outline how it could be used to provide feedback for regulating a

switched mode power supply. Here the VB300 forms part of a network, dc / ac / dc converter, where the input dc voltage is proportional to the output dc voltage. The oscillator is a HCMOS oscillator with an ac output amplitude proportional to its dc supply voltage.

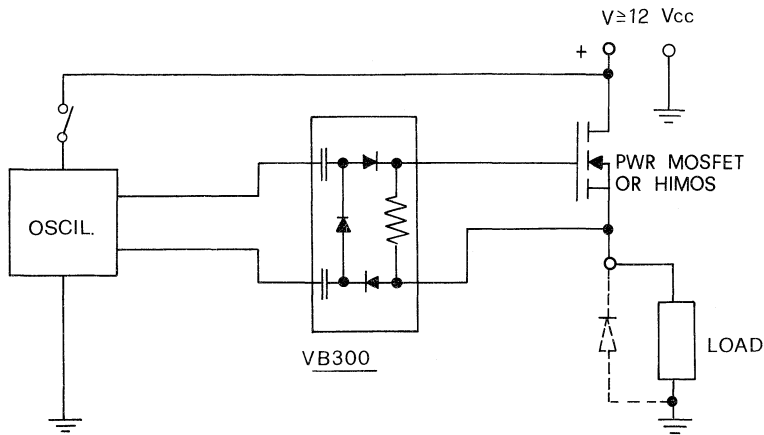


Figure 5. Typical automotive actuator circuit using VB300

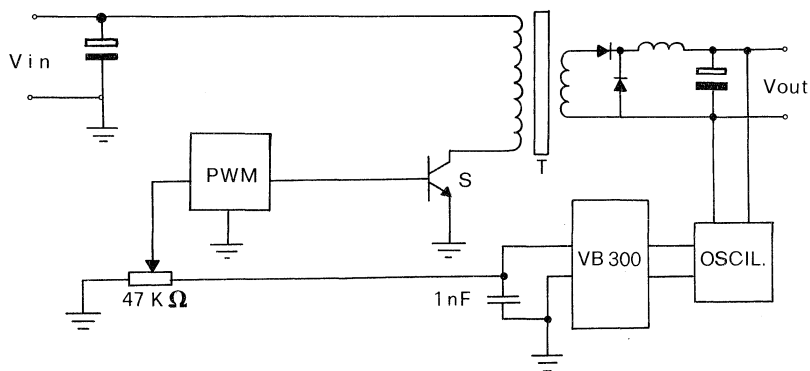
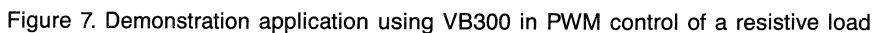


Figure 6. Feedback in an SMPS using VB300

allows the circuit to float around the 110V level. In actual use the circuit should be mounted in insulated housing. Fast turn-off (100 μ sec) of the Power MOSFETS is obtained by connecting a 27Kohm resistor between the gate and the source. A capacitive divider circuit is used to provide the supply voltage for the PWM controller.



FULLY PROTECTED HIGH VOLTAGE INTERFACE FOR ELECTRONIC IGNITION

By S. PALARA ; M. PAPARO ; R. PELLICANO

INTRODUCTION

It is well known that an electronic car ignition system must be able to generate and supply the high energy discharge to the spark plugs, firing the petrol/air mixture at a precise point in each piston cycle. This job is performed by means of an high energy coil, its driver stage and the most suitable controller ; an example is shown in fig. 1.

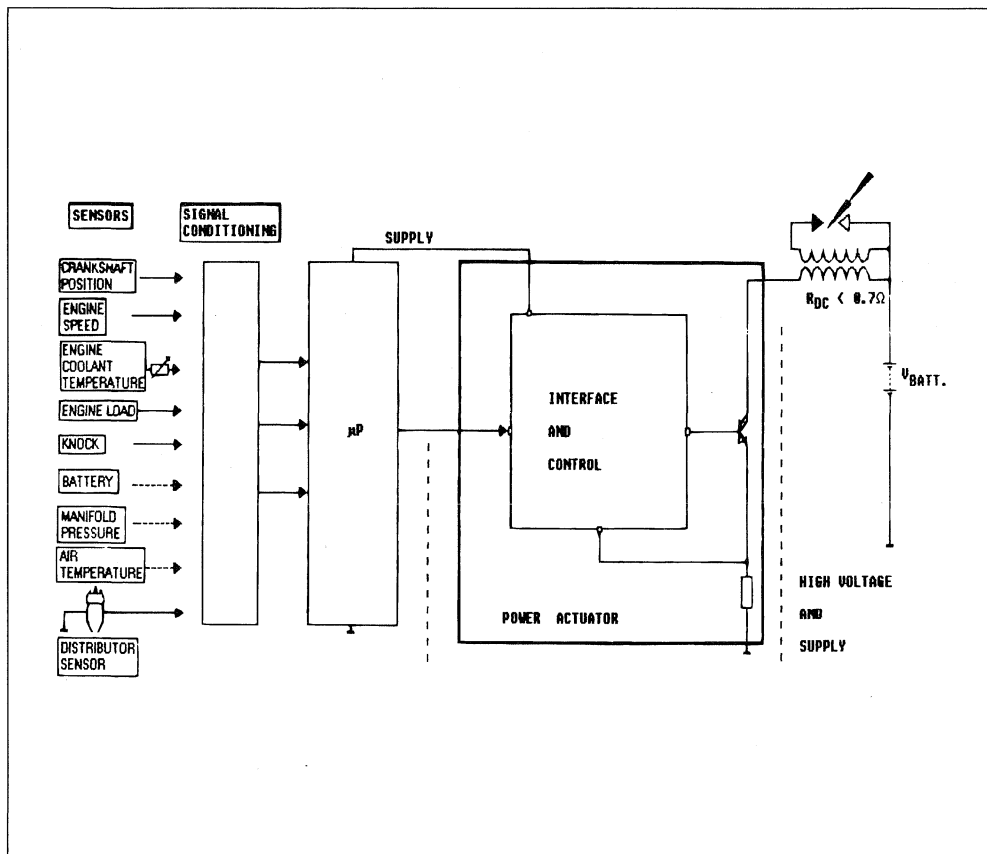
In the most recent car ignition systems the coil current loading signal is controlled by a microproces-

sor that can also optimize the ignition timing. This ensures the correct spark at every speed for all environmental conditions.

The engine efficiency is so optimized ensuring the minimum toxic exhaust gas emission.

The high voltage necessary to generate the spark is obtained by charging the primary winding of the ignition coil with a controlled energy, i.e. a controlled current.

Figure 1 : Car Ignition System.



At the firing point this current is suddenly interrupted transferring the stored energy to the secondary winding and produces output voltage in excess of 20KV and therefore the spark.

The fig. 1 power actuator must also limit the current to a max of 10A and the voltage on the primary to a maximum of about 400V.

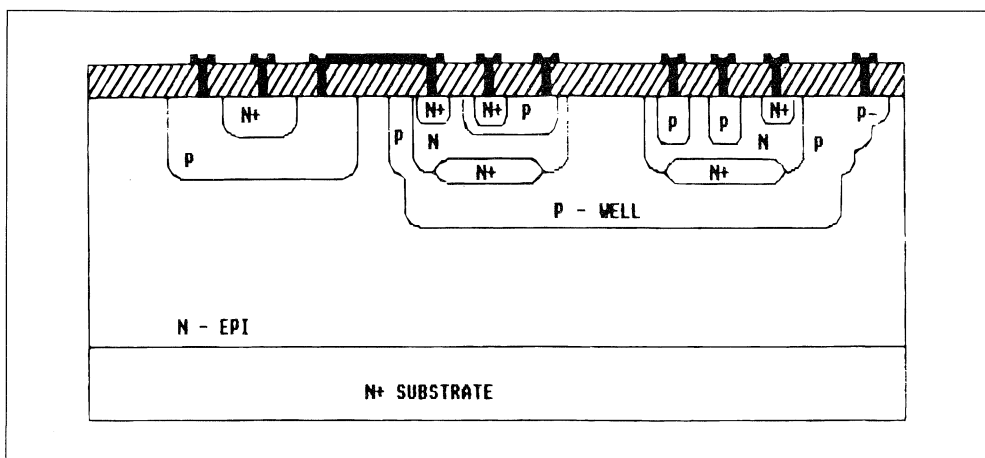
The voltage clamp avoids any damage to the power actuator : if the spark plug, for example, is disconnected, the energy stored in the coil is transferred back to the power actuator.

The device described in this paper realizes these power actuator functions with a very innovative integrated single chip solution.

THE VIPOWER M1 TECHNOLOGY

The VIPower M1 structure shown in fig. 2 combines a vertical current flow NPN power transistor and a

Figure 2 : VIPower Technology Vertical Structure.



low voltage junction isolated I.C. on the same silicon substrate.

This is realized inside a diffused p-type well that takes the place of a reverse-biased p-substrate of conventional ICs and must be connected to the most negative supply.

As in a standard discrete BJT, the first epitaxial layer thickness and resistivity set the V_{ce0} and the ruggedness of the high voltage device, the second epi growth fixes the features of the low voltage components (up to 100V V_{CBO}).

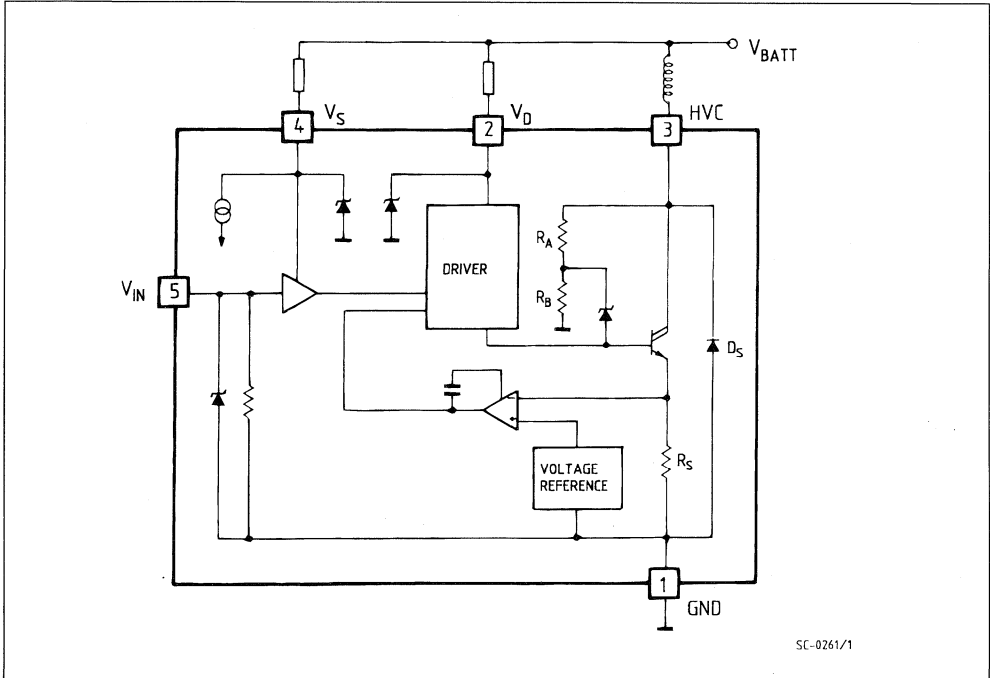
The maximum voltage the power device can withstand is nevertheless also dependent on the maximum field strength at the silicon surface and on the n^+/p -well parasitic diode breakdown voltage.

The high voltage termination of the integrated circuit is achieved by a p-diffused resistor in spiral form connected between the substrate (power darlington collector) and ground.

DEVICE CHARACTERISTICS

The device realizes the ignition, power actuator subsystem of fig. 1.

Figure 3 : Device Block Diagram.



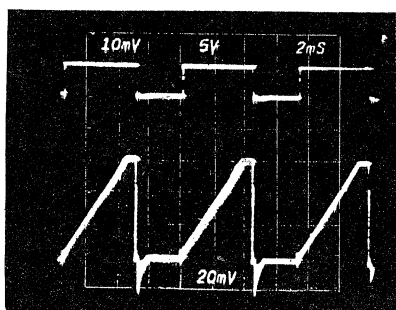
A TTL/CMOS compatible input signal coming from a logic interface, like a microprocessor, determines the turn on of the power darlington integrated in the chip. The darlington collector current charges the coil linearly as long as a set level is reached, typically $6A \pm 3\%$, sensed by an internal aluminium emitter

resistance.

The voltage drop on this resistor is compared with an internally generated threshold ($\sim 200mV$) and limits the current, thus controlling the Darlington base current until the input signal causes the output Darlington to switch off.

Photo 1 shows the coil current behaviour together with the corresponding input signal.

Photo 1 : Collector Current and Corresponding Input Signal.



Input signal (5V/div)

Coll. current (2A/div)

The current loop is made by compensated operational amplifier ensuring enough precision of the set value and hence of the stored energy without requiring external components.

The regulation stability is in fact mandatory in the car ignition system to avoid spurious sparks on the secondary coil winding.

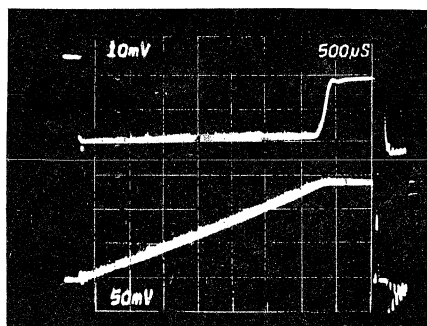
During the current limiting phase, the Darlington collector voltage reaches the battery voltage minus the voltage drop on the coil (due to the primary resistance). It causes high power dissipation in the power actuator which the microprocessor minimizes by delaying the output Darlington switch on.

The overvoltage on the power Darlington collector during the transition from the coil charging to the current limiting phase is low enough to avoid undesirable sparks.

At the input signal switch-off the power Darlington is immediately turned off and the energy stored in the coil is transferred from the primary to the secondary winding causing the spark.

The collector voltage of the power Darlington then rises very rapidly and is detected by the spiral resistor used as the high voltage termination for the chip.

Photo 2 : Collector Voltage During Coil Charging.

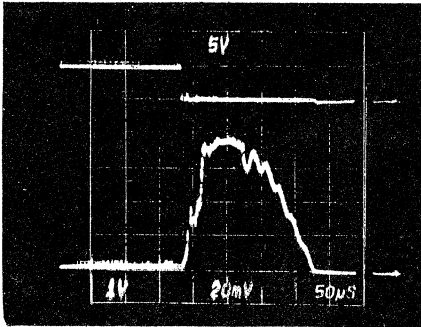


Coll. volt. (5V/div)

Coll. current (2A/div)

This resistor, used as a divider, is connected to a low voltage zener circuit that turns on the power Darlington, holding the collector voltage at a value determined in the chip ($\sim 400V \pm 10\%$) which is less than the Darlington V_{CEO} .

Photo 3 : Voltage Clamp.

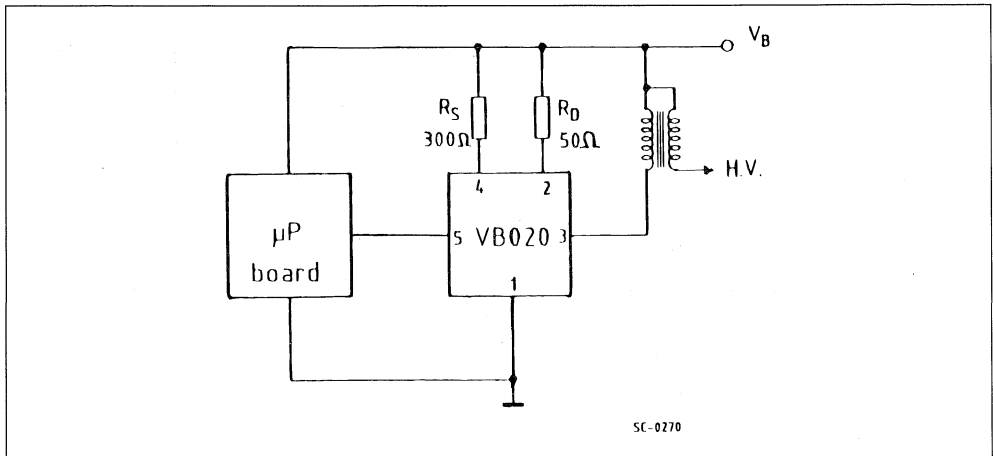


Input signal (5V/div)

Coll. volt. (100V/div)

Fig. 4 shows the application circuit for this device.

Figure 4 : Application Circuit .



Two separate pins for the supply : pin 4 and pin 2, are connected to the battery by means of two different resistors.

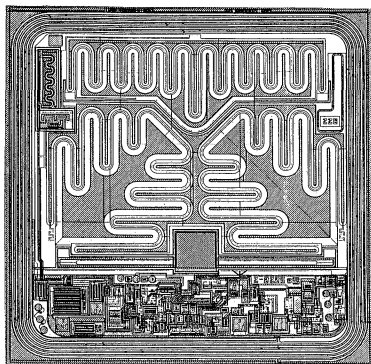
Pin 2 represents the supply of the driver with a current of up to 200mA.

Pin 4 is the supply for the rest of the circuit

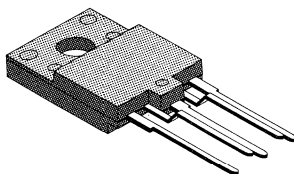
($I_{L1} \sim 3mA$).

A picture of the die is shown in photograph 4.

The device is assembled in a new fully insulated five-lead plastic power package, ISOWATT 5 and shown in figure 5.

Photo 4 : The Die.**Figure 5.**

ISOWATT 5

**CONCLUSION**

The ignition controller described in this paper completely substitutes the existing hybrid solution which requires additional components and manufacturing processes (i.e. insulating substrates, ink layers, active and special passive devices, laser trimming, en-

capsulation etc.). This single chip solution leads to an intrinsic increased compactness. The subsequent higher reliability is further enhanced by the known advantages of integration.

Additionally to that a cost reduction benefit through this approach is also achievable.

SWITCHING POWER SUPPLY

80W TO 400W MONOLITHIC BUCK REGULATORS INTEGRATED IN MULTIPOWER BCD TECHNOLOGY

By C. DIAZZI, G. GATTAVARI

Presented at the High Frequency Power Conversion Conference, San Diego, May 2-5th 1988

The paper describes recent developments in "intelligent" power integrated circuits realized in Bipolar, CMOS, DMOS (MULTIPOWER-BCD) mixed technology integrating both the control and power sections.

The new technology led to a new generation of monolithic switched mode power supplies in Buck configuration working at high switching frequency (up to 500KHz) and with output current in the range from 2A to 10A, at a supply voltage up to 55V.

Switched mode techniques led to the development of high efficiency circuits offering room saving and reduction in costs, mainly of heatsink and output LC filter.

For these applications a new technology, called MULTIPOWER-BCD, has been developed which

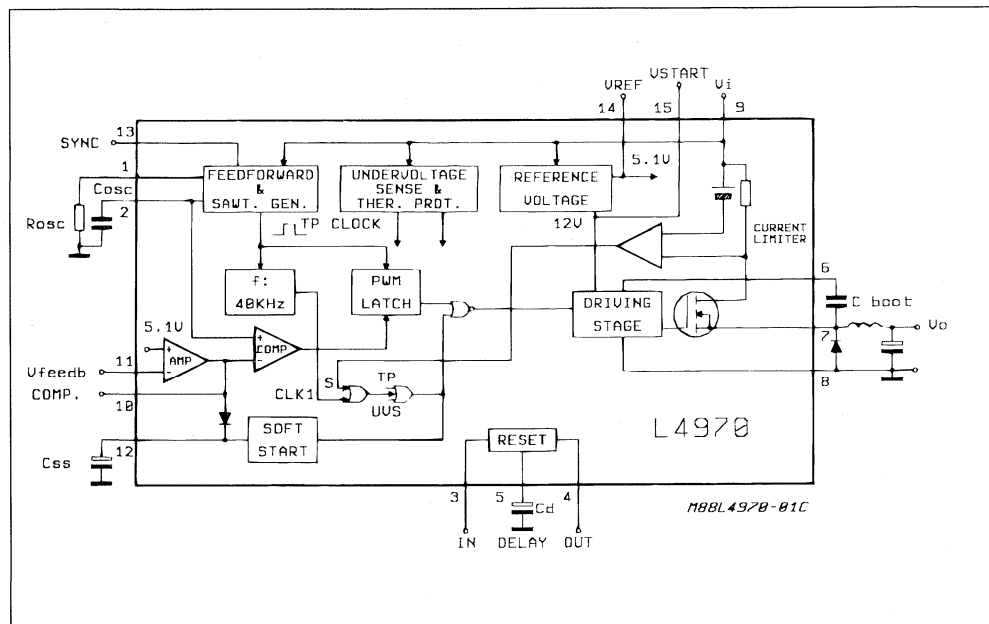
allows the integration on the same chip of isolated power DMOS elements, Bipolar transistors and CMOS logic.

The technology is particularly suitable for the problems arising in switching mode techniques field, due to the characteristics of high efficiency, fast switching speed, no secondary breakdown of the power DMOS element.

The great flexibility that we have at our disposal for the choice of the signal and driving sections components allows optimization and compactness of the system.

By MULTIPOWER-BCD it has been possible to implement the family L497X, a new series of fully integrated switching regulators suitable for DC-DC converters working in Buck configuration.

BLOCK DIAGRAM.



The complete family consists of five devices which differ each other only by the output current value (2A, 3.5A, 5A, 7A, 10A) they can deliver to the load.

The devices rated at 2A and 3.5A are assembled in Dual in Line package, Power Dip 16 + 2 + 2, while the others are assembled in Multiwatt 15 package. Each device integrates a DMOS output power stage, a control section, limiting current and supervisor functions like Reset and Power Fail signal for microprocessors applications.

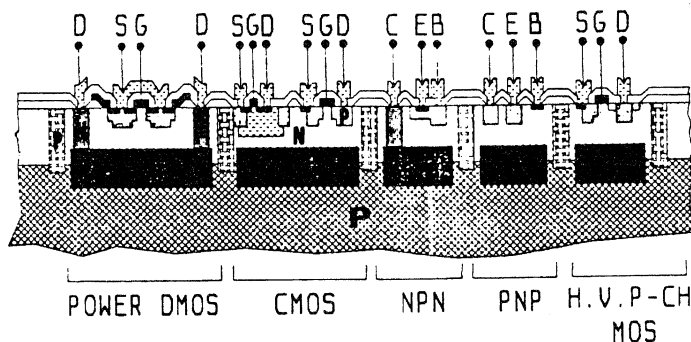
Output voltage can be adjusted starting from the internal reference voltage (5.1V) up to 40V, allowing a maximum output power of 80W for the 2A version and of 400W for the 10A version.

Maximum operating supply voltage is 55V.

THE TECHNOLOGY

The technology architecture is based on the vertical

Figure 1 : Technology Cross Section.



S-9351

DMOS silicon gate process that allows a channel length of 1.5μm ; using a junction isolation technique it has been possible to mix on the same chip Bipolar and CMOS transistors along with the DMOS power components.

Fig. 1 shows a cross section of the technology and table 1 lists the main electrical characteristics of the components.

TAB. 2 shows transistors density comparison between BCD and a standard Bipolar process capable to sustain the same voltage. The table shows that power bipolar component is cheaper in terms of silicon area than DMOS power component, but the disadvantage is largely compensated by the extremely simple circuitry required to drive the DMOS.

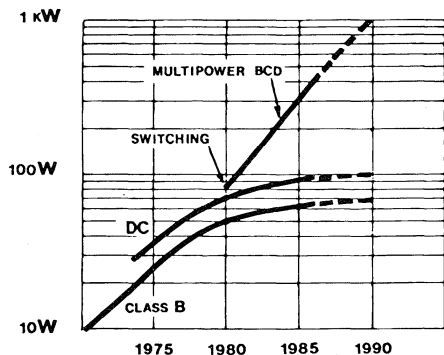
On the other side the table shows the compactness of signal components for BCD process that allows the implementation of complex control circuits.

Table 1 : Electrical Characteristics.

Vertical DMOS	$BV_{DSS} > 60V$	$V_{TH} = 3V$	$f_t = 1GHz$
P-Channel Drain Ext.	$BV_{DSS} > 75V$	$V_{TH} = 1.9V$	$f_t = 200MHz$
CMOS N-Channel	$BV_{DSS} > 15V$	$V_{TH} = 1V$	
CMOS P-Channel	$BV_{DSS} > 15V$	$V_{TH} = 1.9V$	
Bipolar PNP	$BV_{CEO} > 30V$	$\beta = 35$	$f_t = 10MHz$
Bipolar NPN1	$BV_{CEO} > 30V$	$\beta = 35$	$f_t = 300MHz$
Bipolar NPN2	$BV_{CEO} > 30V$	$\beta = 200$	$f_t = 150MHz$

Table 2 : Transistors Density.

	MultipowerBCD Process(60V)	Bipolar Process(50V)
Power DMOS (1A/1V)	1mm ²	
Power Bipolar (1A/1V)		0.7mm ²
Signal Bipolar	200Tr./mm ²	100Tr./mm ²
CMOS	700Tr./mm ²	

Figure 2 : Power Capability Progress of Power ICs.

The curves of fig. 2 show the progress in terms of power capability of power ICs as a function of years. In the 70's class B circuits and DC circuits allowed output power in the range of 70W.

In 1980 with the introduction of switching techniques in power IC's output power up to 200W were

reached ; with the introduction of BCD technology output power increased up to 400W.

THE DEVICES : FUNCTIONS AND BLOCK DIAGRAM

The family of L497X products finds its typical application in those systems which require stabilized supply voltage starting from a non stabilized supply of 60V.

Such applications are typically found in personal computer systems, printers, typewriters and so on where for safety of working people a maximum supply voltage of 48V is allowed on the secondary side of the transformer which supplies the system.

The devices are used in step down configuration (buck converter) and can regulate output voltage from 5.1V up to 40V.

The circuits contain the power stage, control sections and diagnostic and protection circuits that make the devices particularly indicated to supply microprocessor based systems.

By integrating the power and control functions on a single monolithic chip a very compact and low cost system has been realized.

Additional cost and volume savings can be obtained since the high switching frequency (200-500KHz) offers significant savings in LC filter.

See the block diagram of the device at the first page of this note.

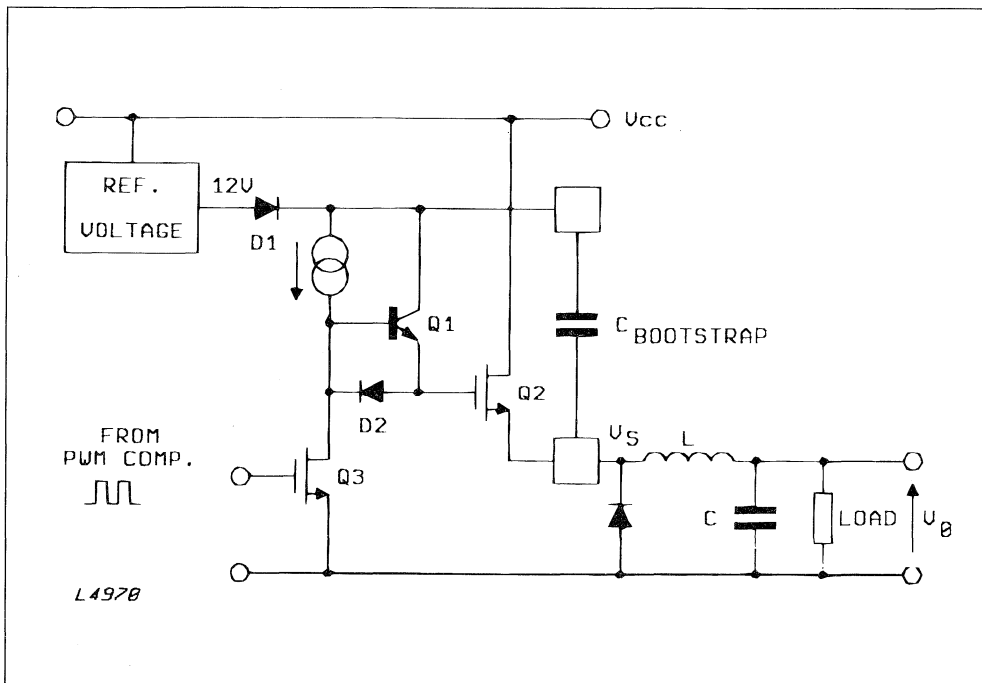
It includes a DMOS power stage with PWM control loop, soft start circuits, trimmed 5.1V voltage reference, under voltage lock out circuit, feedforward

function, pulse by pulse current protection, thermal protection for the power stage and a Power Fail-Reset circuit which generates a Reset signal for a microprocessor.

The family of devices is rated at five different maximum output current levels to the load : 2A, 3.5A, 5A, 7A, 10A.

The first two devices are assembled in Dual in Line power package which needs no heatsink and which shows a thermal resistance junction to pin of 11°C/W.

Figure 3.



The last three devices are assembled in Multiwatt package which shows a thermal resistance of 1°C/W (j-case).

THE POWER STAGE

A simplified schematic of the output stage along with the external filter components is shown in fig. 3.

Power stage and its associated driving circuits are

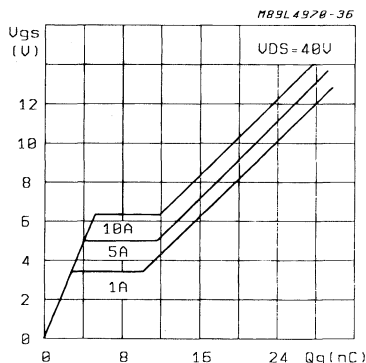
among the most critical components to achieve good performances at high switching frequency.

An external bootstrap capacitance, charged via diode D1 at 12V, is needed to provide the correct gate drive to the power DMOS N-channel transistor.

The driving circuit is able to deliver a current peak of 0.5A, during turn on and turn off phases, to the gate of power DMOS transistor.

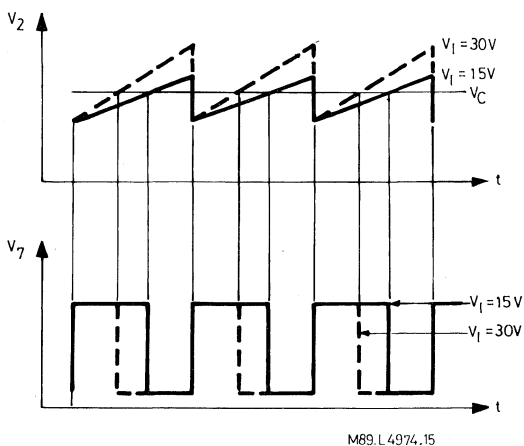
Table 3 : Power DMOS Electrical Characteristics.

$BV_{DSS} > 60V$	at $I_D = 1mA$		$V_{GS} = 0V$
$R_{DS(ON)} = 100m\Omega$	at $I_D = 10A$	$T_j = 25^\circ C$	$V_{GS} = 10V$
$R_{DS(ON)} = 150m\Omega$	at $I_D = 10A$	$T_j = 150^\circ C$	$V_{GS} = 10V$
$V_{TH} = 3V$	at $I_D = 1mA$		

Figure 4 : GATE-CHARGE Curves for the Power DMOS.

The described circuit shows commutation times of 50ns.

The five devices of L497X family differentiate each other only for the level of current protection, while

Figure 5 : Voltage-feed-forward Technique.

the control part is the same and power device area is the same to guarantee low power dissipation also for low current versions in Dual in Line package.

Table 3 shows electrical characteristics of the power DMOS implemented in the chip.

REGULATION LOOP

The regulation loop (block diagram) consists of a classical Pulse Width Modulation circuit and includes a sawtooth oscillator, error amplifier, voltage comparator and PWM latch.

A precision 5.1V voltage reference, trimmed on the chip to guarantee a tight 1% initial tolerance and 1% temperature range, is generated and constitutes the voltage reference for the loop. The error amplifier is a transconductance type with high impedance current output and the loop can be easily compensated by placing a resistor capacitor series network between amplifier output and ground (pole-zero compensation).

The soft start circuit incorporated in the device

allows the device to soft start the power stage after power up and after an inhibit state. The L497X devices feature a voltage feedforward technique, which is completely integrated and does not require any external component, that increases the slope of the sawtooth oscillator proportionally to the value of supply voltage V_{cc} .

As V_{cc} increases the output pulse width (transistor on time) decreases in such a manner as to provide a constant "volt-second" product to the inductance (fig. 5).

Freedom of V_o from V_{cc} minimizes error amplifier gain requirements while maintaining good output regulation.

The amplifier not compensated has a DC voltage gain $A_v = g_m \cdot R_o = 70\text{Db}$ with $g_m = 1.3\text{mA/V}$ and $R_o = 3.3\text{M}\Omega$, $C_o = 5\text{pF}$.

POWER FAIL-RESET CIRCUIT

L497X include a voltage sensing circuit that may be used to generate a power on power off reset signal for a microprocessor system.

The circuit senses the input supply voltage and the output generated voltage and will generate the re-

quired reset signal only when both the sensed voltages have reached the required value for correct system operation. The Reset signal is generated after a delay time programmable by an external capacitor on the delay pin.

Fig. 6 shows the circuit implementation of Reset circuit.

The supply voltage is sensed on an external pin, for programmability of the threshold, by a first comparator.

The second comparator has the reference threshold set at slightly less the ref. voltage for the regulation circuit and the other input connected internally at the feedback point on the error amplifier.

This allows to sense the output regulated voltage.

When both the supply voltage and the regulated voltage are in the correct range, transistor Q1 turns off and allows the current generator to charge the delay capacitor.

When the capacitor voltage reaches 5V the output Reset signal is generated. A latch assures that if a spike is present on the sensed voltage the delay capacitor discharges completely before initialization of a new Reset cycle.

Figure 6 : Power Fail / Reset Circuit.

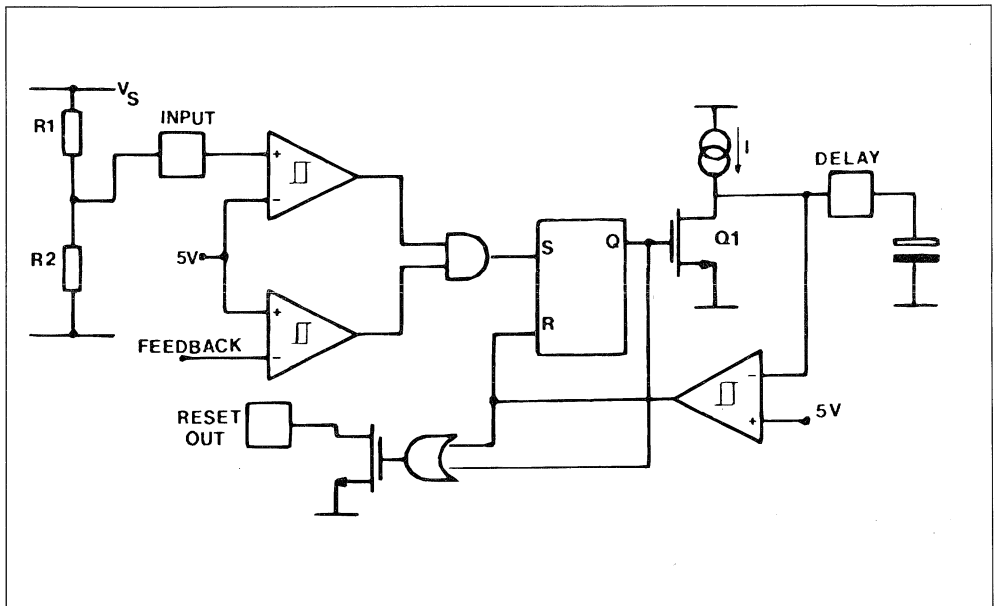
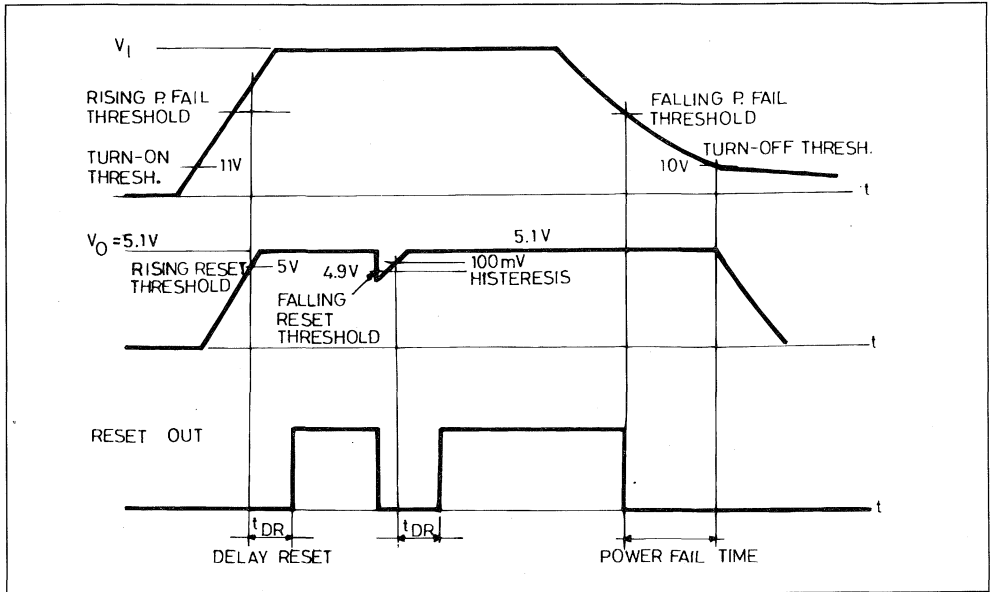


Figure 7 : Reset Waveforms.



The output gate assures immediate take of reset signal without waiting for complete discharge of delay capacitor.

Reset output is an open collector transistor capable of sinking 20mA at 200mV voltage.

Fig. 7 shows reset waveforms.

THERMAL CONSIDERATIONS

Power losses in the switched mode devices are given by three major contributions : DC losses of the power stage, switching losses of the power stage and quiescent losses of control circuit.

DC losses of the power stage are given by the following relationship :

$$P_{DC} = R_{DS(ON)} \cdot I^2 \cdot \delta \quad \delta = \text{Duty cycle} \quad (1)$$

Switching losses of the power stage are given by the following relationship assuming square waveform for DRAIN-SOURCE voltage and triangular waveform for DRAIN current (inductive load) :

$$P_{DS} = (1/2 V_{CC} \cdot I_D \cdot t_{rise} + 1/2 V_{CC} I_D \cdot t_f) \cdot f_{switch} \quad (2)$$

Quiescent current drawn from V_{CC} to supply driving and control circuits is $I_q = 12\text{mA}$. Power dissipation due to quiescent current is given by :

$$P_{DQ} = V_{CC} \cdot I_q \quad (3)$$

L497X family consists of 5 devices differentiating for the level of output current and for the package in which they are included.

TABLE 4 shows the current capability and type of package for the 5 devices :

Table 4.

Type	Current Limit (internally set)	Package	R_{thj-c}
L4972	$2.7A \pm 10\%$	D.I.P. 16 + 2 + 2	11°C/W
L4974	$4.5A \pm 10\%$	D.I.P. 16 + 2 + 2	11°C/W
L4975	$6.3A \pm 10\%$	Multiwatt 15	1°C/W
L4977	$8.8A \pm 10\%$	Multiwatt 15	1°C/W
L4970	$12A \pm 10\%$	Multiwatt 15	1°C/W

L4972 and L4974 are assembled in a Dual in Line package (power dip) with 4 pins mechanically connected to the copper frame of the package.

This allows to dissipate heat from the frame to external world by some dissipating copper area on the PC board, without heatsink on the package.

Fig. 8 shows Thermal Resistance junction to ambient as a function of copper dissipating area on the PC board.

As we can see from fig. 8 and 9 we have $R_{thj-pin} = 11^{\circ}\text{C/W}$, $R_{thj-a} = 35^{\circ}\text{C/W}$.

Thermal Resistance junction-case of Multiwatt package is 1°C/W for a dissipating silicon area of 30000mils^2 .

Figure 8 : Thermal Resistance j-pin (DIP).

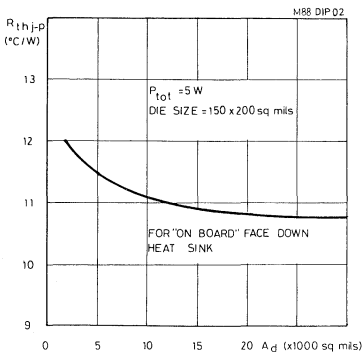


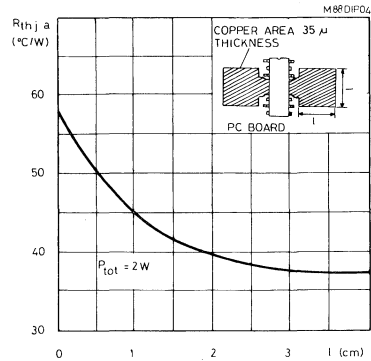
Table 5.

Type	P _o	P _{Dtot}	T _j (T _{amb} = 70°C)
L4972	80W (2A, 40V)	1.58W	125°C
L4974	70W (3.5A, 20V)	2.2W	147°C
L4975	200W (5A, 40V)	4.85W	140°C (R _{thj-a} = 14°C/W)
L4977	280W (7A, 40V)	8.23W	140°C (R _{thj-a} = 8.5°C/W)
L4970	400W (10A, 40V)	15W	140°C (R _{thj-a} = 5°C/W)

For chips in Multiwatt package it has been calculated the heatsink required to guarantee 140°C junction temperature.

For Power Dip package it has been calculated junction temperature knowing j-amb thermal resistance according to fig. 8 and 9.

Figure 9 : Thermal Resistance j-ambient (DIP).



According to formula (1) (2) (3) and to Thermal Resistance Data we can calculate power dissipation and junction temperature for the 5 applications.

Assuming $R_{DS(ON)} = 0.15\Omega$, $T_j = 150^{\circ}\text{C}$; $t_{rise} = t_{fall} = 50\text{ns}$;

$f_{switch} = 100\text{KHz}$; $V_{cc} = 50\text{V}$

we can consider the power dissipated in the following working conditions :

The data show that MULTIPOWER BCD technology has allowed, with its outstanding features, the implementation of a complete switched mode power supply able to deliver about 80W in Dual in Line package without heatsink and 400W in Multiwatt package.

APPLICATION CIRCUIT

Fig. 10 shows typical application circuit for 10A de-

vice and in the table are listed the typical electrical characteristics and performances achieved.

Figure 10 : Application Circuit.

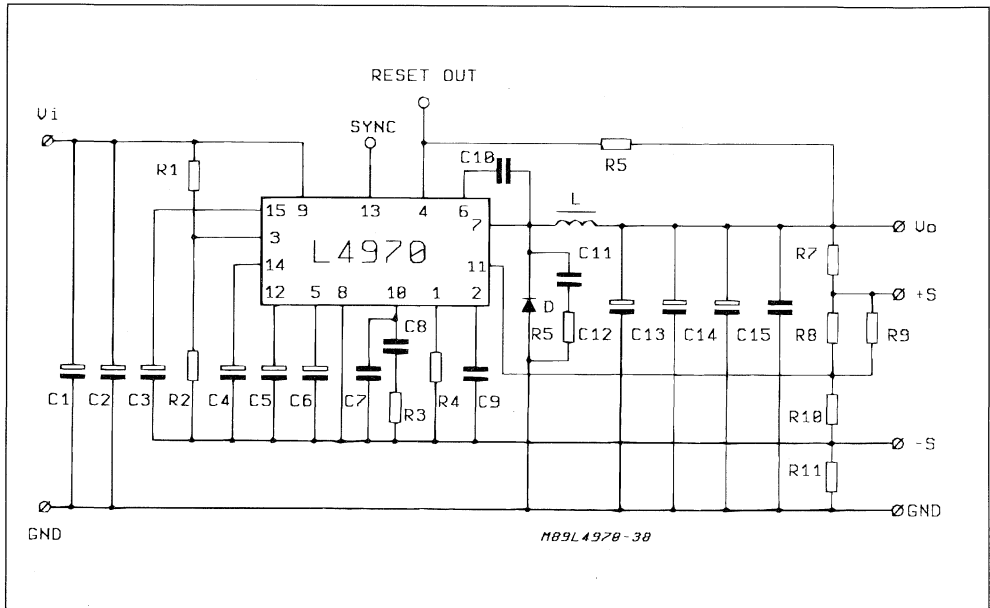
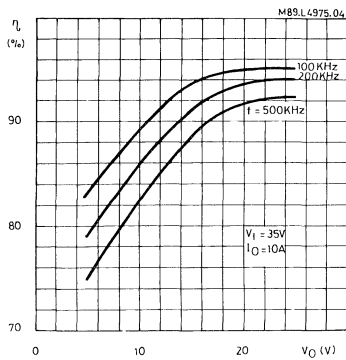


Table 6 : Electrical and System Characteristics.

Input Voltage	55V MAX
Output Current	10A (internally limited)
Reference Voltage	5.1V $\pm$ 10%
Temp. Stability of Ref. Volt.	0.2mV/°C
Line Regulation V _i = 12V-50V	70dB
Ripple Rejection f = 120Hz	60dB
Soft Start Time	20ms
Reset Delay Time	100ms
Switching Frequency	200kHz

Fig. 11 shows efficiency curves for 10A output current and fig.12 for 5A output current, as a

Figure 11.



function of output voltage and switching frequency.

Figure 12.

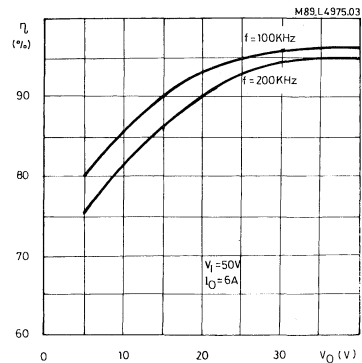
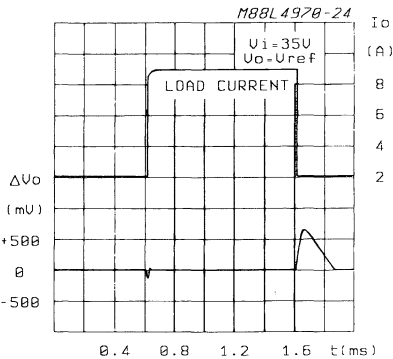


Fig. 13 shows a transient load condition from 2A to 8A and viceversa and the output voltage transient.

Figure 13 : Load Transient.



$L_o = 50\mu H$
 $C_o = 300\mu F$
 $V_o = 5.1V$
 $V_i = 35V$
 $f = 200KHz$

CONCLUSIONS

A family of integrated Buck regulators realized in MULTIPOWER BCD technology has been presented. The high efficiency characteristics of the devices implemented allows to deliver to the load 80W in a DIP package and 400W in a Multiwatt package working at high switching frequency ($> 100KHz$).

Future trends for MULTIPOWER BCD technology is the increase of breakdown voltage (250V, 500V) for the implementation of off-line systems.

ACKNOWLEDGMENTS

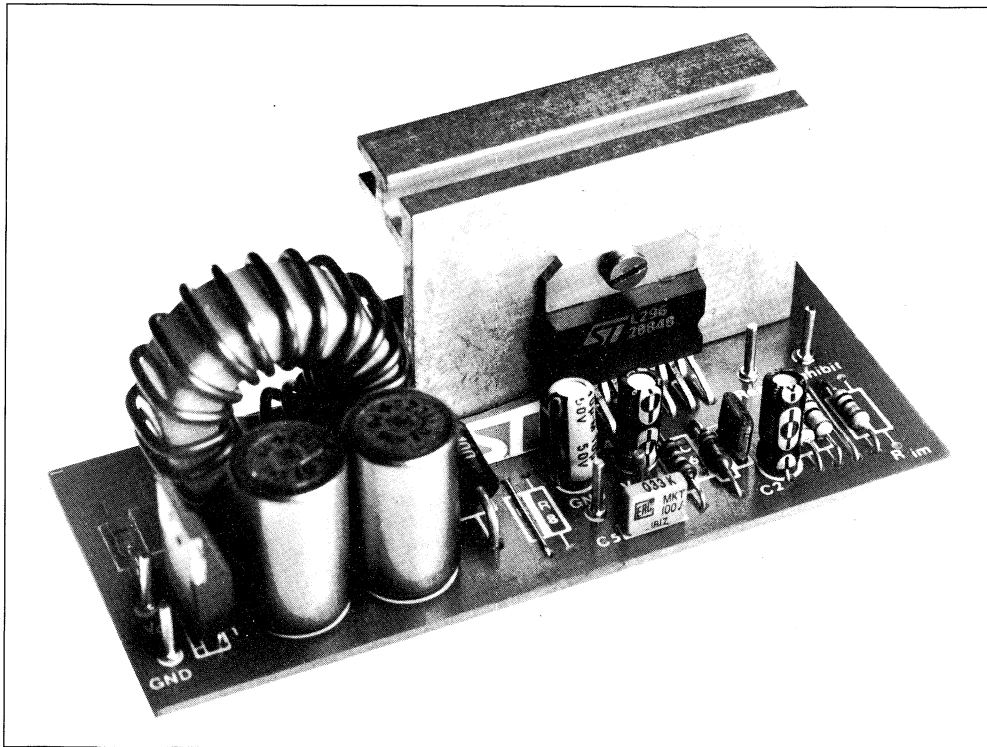
The authors wish to thank F. CONSIGLIERI, G. IZZO and L. PAGOTTO for the contribution given to prepare the material for the paper.

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DESIGNING WITH THE L296 MONOLITHIC POWER SWITCHING REGULATOR

A cost-effective replacement for costly hybrids, the L296 Power Switching Regulator delivers 4A at an output voltage of 5.1V to 40V and includes many popular supply features. This comprehensive application guide explains how the device operates and how it is used. Typical application circuits are also presented.



The SGS THOMSON L296 is the first monolithic switching regulator in plastic package which includes the power section. Moreover, the circuit includes all the functions which make it specially suited for microprocessor supply.

Before the introduction of L296, which realizes the step down configuration, this function was implemented with discrete power components driven by integrated PWM regulator circuits (giving a maximum output current of 300 to 400mA) or with hybrid circuits. Both of these solutions are characterized by a low efficiency of the power transistor. For this reason it is generally necessary to operate at frequen-

cies in the 20kHz to 40kHz range. Of the two alternatives discrete solutions are usually less expensive because they do not include as many functions as the L296.

With the new L296 regulator the driving problem of the power control stage has been eliminated. Besides a higher overall efficiency, it is therefore also possible to operate directly at frequencies as high as 100kHz. At 200kHz the device still operates (further reducing the cost of the L and C external components) when a reduction of a few percent in efficiency is acceptable.

The device delivers a maximum current of 4 A to the load, at an output voltage adjustable from 5.1 to 40V ; the maximum operating input voltage is 46V. The high voltage and the high current capabilities of the device are a result of the special technology used and the special care taken in designing the power transistor. Essential requirements for a good power transistor are high gain and high current levels, low saturation voltage and good second breakdown robustness. To achieve high gain at high current levels, the power transistor has to be designed to maximize the emitter's perimeter/area ratio.

In the L296 power transistor, realized with a high voltage (50V) process, current densities in the magnitude order of 10mA/Mil² are achieved.

In its most complete configuration, in which all the available functions are being used, a significant reduction of the external component count is achieved compared with discrete component solution.

The L296 is mounted in a MULTIWATT® plastic package with 15 pins, minimizing the cost per watt and allowing a low thermal resistance of 3° C/W between junction and package and of 35° C/W be-

tween junction and ambient. This thermal resistance (including the contact resistance) is comparable to that of the more costly metal TO-3 packages.

THE STEP-DOWN CONFIGURATION

Fig. 1 shows the simplified block diagram of the circuit realizing the step-down configuration. This circuit operates as follows : Q1 acts as a switch at the frequency f and the ON and OFF times are suitably controlled by the pulse width modulator circuit. When Q1 is saturated, energy is absorbed from the input which is transferred to the output through L. The emitter voltage of Q1, V_E , is $V_i - V_{sat}$ when Q is ON and $-V_F$ (with V_F the forward voltage across the D diode as indicated) when Q1 is OFF. During this second phase the current circulates again through L and D. Consequently a rectangular shaped voltage appears on the emitter of Q1 and this is then filtered by the L-C-D network and converted into a continuous mean value across the capacitor C and therefore across the load. The current through L consists of a continuous component, I_{LOAD} , and a triangular-shaped component super-imposed on it, ΔI_L , due to the voltage across L.

Figure 1 : The Basic Step-down Switching Regulator Configuration.

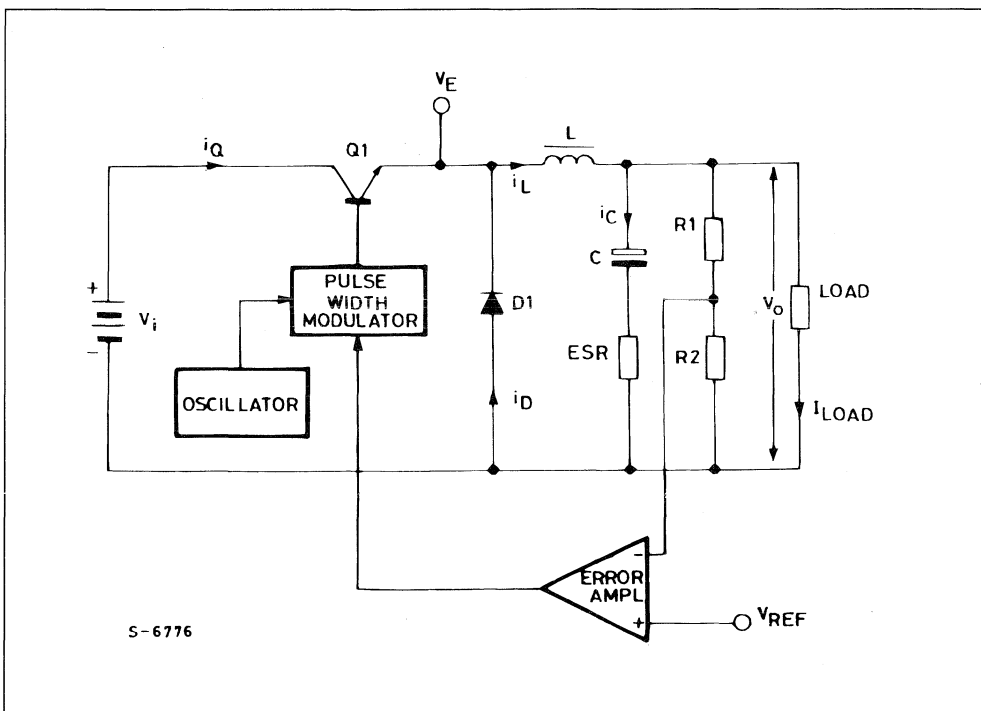
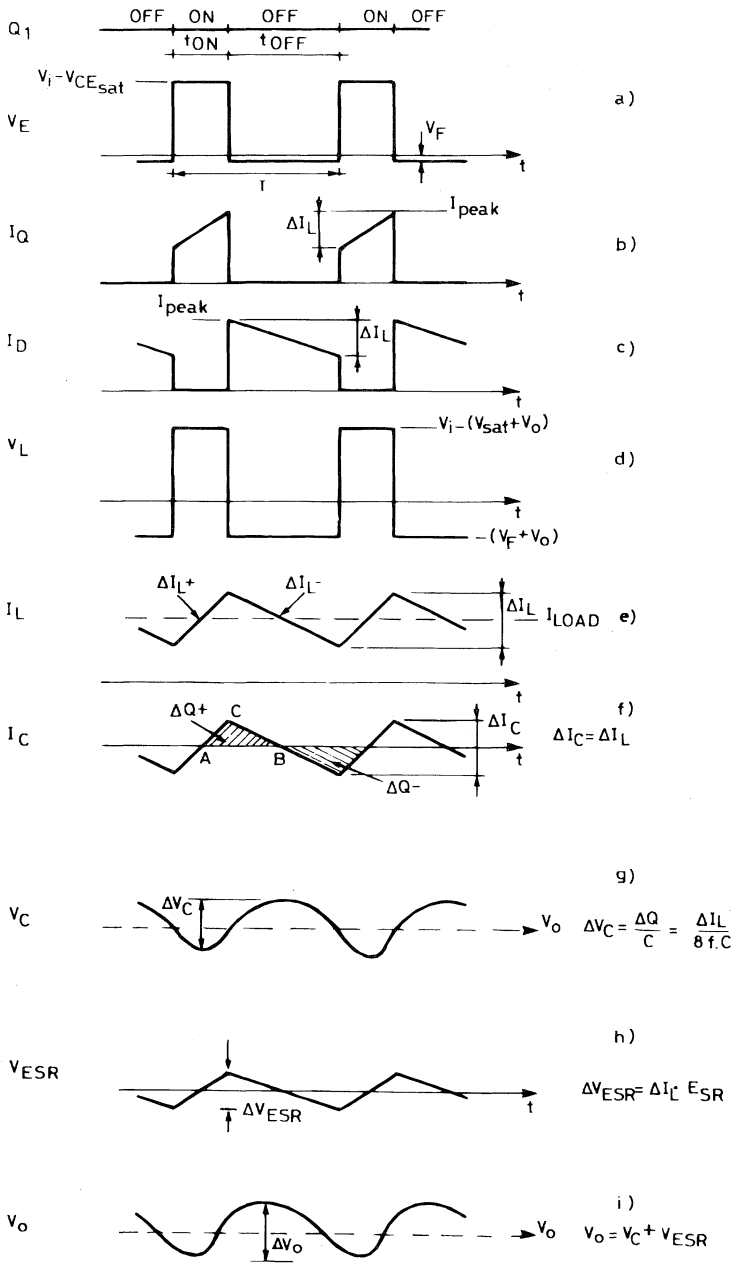


Figure 2 : Principal Circuit Waveforms of the figure 1 Circuit.

S-6788

Fig. 2 shows the behaviour of the most significant waveforms, in different points of the circuit, which help to understand better the operation of the power section of the switching regulator. For the sake of simplicity, the series resistance of the coil has been neglected. Fig. 2a shows the behaviour of the emitter voltage (which is practically the voltage across the recirculation diode), where the power saturation and the forward V_F drop across the diode are taken into account.

The ON and OFF times are established by the following expression :

$$V_o = (V_i - V_{sat}) \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

Fig. 2b shows the current across the switching transistor. The current shape is trapezoidal and the operation is in continuous mode. At this stage, the phenomena due to the catch diode, that we consider as dynamically ideal, are neglected. Fig. 2c shows the current circulating in the recirculation diode. The sum of the currents circulating in the power and in the diode is the current circulating in the coil as shown in fig. 2e. In balanced conditions the ΔI_L^+ current increase occurring during T_{ON} has to be equal to the ΔI_L^- decrease occurring during T_{OFF} . The mean value of I_L corresponds to the charge current.

The current ripple is given by the following formula :

$$\begin{aligned} \Delta I_L^+ = \Delta I_L^- &= \frac{(V_i - V_{sat}) - V_o}{L} T_{ON} = \\ &= \frac{V_o + V_F}{L} T_{OFF} \end{aligned}$$

It is a good rule to respect to $I_{oMIN} \geq I_L/2$ relationship, that implies good operation in continuous mode. When this is not done, the regulator starts operating in discontinuous mode. This operation is still safe but variations of the switching frequency may occur and the output regulation decreases.

Fig. 2d shows the behaviour of the voltage across coil L . In balanced conditions, the mean value of the voltage across the coil is zero. Fig. 2f shows the current flowing through the capacitor, which is the difference between I_L and I_{LOAD} .

In balanced conditions, the mean current is equal to zero, and $\Delta I_C = \Delta I_L$. The current I_C through the capacitor gives rise to the voltage ripple.

This ripple consists of two components : a capacitive component, ΔV_C , and a resistive component, ΔV_{ESR} , due to the ESR equivalent series resistance of the capacitor. Fig. 2g shows the capacitive com-

ponent ΔV_C of the voltage ripple, which is the integral of a triangular-shaped current as a function of time. Moreover, it should be observed that $v_C(t)$ is in quadrature with $i_C(t)$ and therefore with the voltage V_{ESR} . The quantity of charge ΔQ^+ supplied to the capacitor is given by the area enclosed by the ABC triangle in fig. 2f :

$$\Delta Q = \frac{1}{2} \cdot \frac{T}{2} \cdot \frac{\Delta I_L}{2}$$

which therefore gives :

$$\Delta V_C = \frac{Q}{C} = \frac{\Delta I_L}{8fc}$$

Fig. 2h shows the voltage ripple V_{ESR} due to the resistive component of the capacitor. This component is $V_{ESR}(t) = i_C(t) \cdot ESR$. Fig. 2i shows the overall ripple V_o , which is the sum of the two previous components. As the frequency increases ($> 20kHz$), which is required to reduce both the cost and the sizes of L and C , the V_{ESR} component becomes dominant. Often it is necessary to use capacitors with greater capacitance (or more capacitors connected in parallel) to limit the value of ESR within the required level.

We will now examine the stepdown configuration in more detail, referring to fig. 1 and taking the behaviour shown in fig. 2 into account.

Starting from the initial conditions, where $Q = ON$, $v_C = V_o$ and $i_L = i_D = 0$, using Kirckoff second principle we may write the following expression :

$V_i = v_L + v_C$ (V_{sat} is neglected against V_i).

$$V_i = L \frac{di_L}{dt} + v_C = L \frac{di_L}{dt} + V_o \quad (1)$$

which gives :

$$\frac{di_L}{dt} = \frac{(V_i - V_o)}{L} \quad (2)$$

The current through the inductance is given by :

$$I_L = \frac{(V_i - V_o)}{L} t \quad (3)$$

When V_i , V_o , and L are constant, I_L varies linearly with t . Therefore, it follows that :

$$\Delta I_L^+ = \frac{(V_i - V_o) T_{ON}}{L} \quad (4)$$

When Q is OFF the current through the coil has reached its maximum value, I_{peak} and because it cannot vary instantaneously, the voltage across the coil is inverted and the diode D becomes forward biased to allow the recirculation of the current through the load.

When Q switches OFF, the following situation is present :

$$v_C(t) = V_o, i_L(t) = i_D(t) = I_{peak}$$

And the equation associated to the following loop may be written :

$$V_F + L \frac{di_L}{dt} + v_C = 0 \quad (5)$$

where :

$$v_C = V_o$$

$$\frac{di_L}{dt} = -(V_F + V_o)/L \quad (6)$$

It follows therefore that :

$$i_L(t) = -\frac{V_F + V_o}{L} t \quad (7)$$

The negative sign may be interpreted with the fact that the current is now decreasing. Assuming that V_F may be neglected against V_o , during the OFF time the following behaviour occurs :

$$i_L = -\frac{V_o}{L} t \quad (8)$$

therefore :

$$\Delta i_L^- = \frac{V_o}{L} T_{OFF} \quad (9)$$

But, because

$$\Delta i_L^+ = \Delta i_L^- \quad \text{if follows that :}$$

$$\frac{(V_i - V_o) T_{ON}}{L} = \frac{V_o T_{OFF}}{L}$$

which allows us to calculate V_o :

$$V_o = V_i \frac{T_{ON}}{T_{ON} + T_{OFF}} = V_i \frac{T_{ON}}{T} \quad (10)$$

where T is the switching period.

Expression (10) links the output voltage V_o to the input voltage V_i and to the duty cycle. The relationship between the currents is the following :

$$I_{IDC} = I_{ODC} \cdot \frac{T_{ON}}{T}$$

EFFICIENCY

The system efficiency is expressed by the following formula :

$$\eta \% = \frac{P_o}{P_i} \cdot 100$$

$$\text{where } P_o = V_o I_o \quad (\text{with } I_o = I_{LOAD})$$

is the output power to the load and P_i is the input power absorbed by the system. P_i is given by P_o ,

plus all the other system losses. The expression of the efficiency becomes therefore the following :

$$\eta = \frac{P_o}{P_o + P_{sat} + P_D + P_L + P_q + P_{sw}} \quad (12)$$

DC LOSSES

P_{sat} : saturation losses of the power transistor Q.
These losses increase as V_i decreases.

$$P_{sat} = V_{sat} \cdot I_o \frac{T_{ON}}{T} = V_{sat} I_o \frac{V_o}{V_i} \quad (13)$$

$$\text{where } \frac{T_{ON}}{T} = \frac{V_o}{V_i} \quad \text{and } V_{sat} \text{ is the power}$$

transistor saturation at current I_o .

P_D : losses due to the recirculation diode. These losses increase as V_i increases, as in this case the ON time of the diode is greater.

$$P_D = V_F I_o \frac{V_i - V_o}{V_i} = V_F I_o \left(1 - \frac{V_o}{V_i}\right) \quad (14)$$

where V_F is the forward voltage of the recirculation diode at current I_o .

P_L : losses due to the series resistance R_S of the coil

$$P_L = R_S I_o^2 \quad (15)$$

P_q : losses due to the stand-by current and to the power driving current :

$$P_q = V_i I'_{3q} + V_i I''_{3q} \frac{T_{ON}}{T} \quad (16)$$

where being :

$$\frac{T_{ON}}{T} = \frac{V_o}{V_i} \quad \text{it follows that :}$$

$$P_q = V_i I'_{3q} + V_o I''_{3q} \quad \text{in which :}$$

$$I'_{3q} = I_{3q} \quad \text{at 0 \% duty cycle}$$

$$I''_{3q} = I_{3q}(100 \% \text{ d.c.}) - I_{3q}(0 \% \text{ d.c.})$$

SWITCHING LOSSES

P_{sw} : switching losses of the power transistor :

$$P_{sw} = V_i I_o \frac{t_r + t_f}{2T}$$

The switching losses of the recirculation diode are neglected (which are anyway negligible) as it is assumed that diode is used with recovery time much smaller than the rise time of the power transistor.

We can neglect losses in the coil (it is assumed that Δi_L is very small compared to I_o) and in the output capacitor, which is assumed to show a low ESR.

Calculation of the inductance value, L

Calculation T_{ON} and T_{OFF} through (4) and (9) respectively it follows that :

$$T_{ON} = \frac{\Delta I_L^+ \cdot L}{V_i - V_o} \quad T_{OFF} = \frac{\Delta I_L^- \cdot L}{V_o}$$

But because :

$$T_{ON} + T_{OFF} = T \quad \text{and} \quad \Delta I_L^+ = \Delta I_L^- = \Delta I_L$$

it follows that :

$$\frac{\Delta I_L \cdot L}{V_i - V_o} + \frac{\Delta I_L \cdot L}{V_o} = T$$

Calculating L, the previous relation becomes :

$$L = \frac{(V_i - V_o) V_o}{V_i \Delta I_L} T \quad (18)$$

Fixing the current ripple in the coil required by the design (for instance 30% of I_o), and introducing the frequency instead of the period, it follows that :

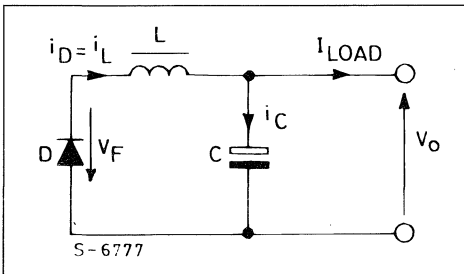
$$L = \frac{(V_i - V_o) V_o}{V_i \cdot 0.3 \cdot I_o \cdot f} \quad \text{where L is in Henry and f in Hz}$$

Calculation of the output capacitor C

From the output node in fig. 3 it may be seen that the current through the output capacitor is given by :

$$i_c(t) = i_L(t) - I_o$$

Figure 3 : Equivalent Circuit Showing Recirculation when Q1 is Turned Off.



From the behaviour shown in fig. 2 it may be calculated that the charge current of the output capacitor, within a period, is $\Delta I_L/4$, which is supplied for a time $T/2$. It follows therefore that :

$$\Delta V_C = \frac{\Delta I_L}{4C} \frac{T}{2} = \frac{\Delta I_L T}{8C} = \frac{\Delta I_L}{8fC} \quad (19)$$

but, remembering expression (4) :

$$\Delta I_L^+ = \frac{(V_i - V_o) T_{ON}}{L} \quad \text{and} \quad T_{ON} = \frac{V_o}{V_i} T$$

therefore equation (19) becomes :

$$\Delta V_C = \frac{(V_i - V_o) V_o}{8 V_i f^2 L C}$$

Finally, calculating C it follows that :

$$C = \frac{(V_i - V_o) V_o}{8 V_i \Delta V_C f^2 L} \quad (20)$$

where : L is in Henrys
C is in Farads
f is in Hz

Finally, the following expression should be true :

$$ESR_{max} = \frac{\Delta V_{Cmax}}{\Delta I_L} \quad (21)$$

It may happen that to satisfy relation (21) a capacitance value much greater than the value calculated through (20) must be used.

TRANSIENT RESPONSE

Sudden variations of the load current give rise to overvoltages and undervoltages on the output voltage. Since $i_c = C (dv_c/dt)$ (22), where $dv_c = \Delta V_o$, the instantaneous variation of the load current ΔI_o is supplied during the transient by the output capacitor. During the transient, also current through the coil tends to change its value.

Moreover, the following is true :

$$v_L = L \frac{di_L}{dt} \quad (23) \quad \text{where } di_L = \Delta I_o$$

$$v_L = V_i - V_o \quad \text{for a load increase}$$

$$v_L = V_o \quad \text{for a load decrease}$$

Calculating dt from (22) and (23) and equalizing, it follows that :

$$L \frac{di_L}{v_L} = C \frac{dv_c}{i_c}$$

Calculating dv_c and equalizing it to ΔV_o , it follows that :

$$\Delta V_o = \frac{L \Delta I_o^2}{C (V_i - V_o)} \quad (24) \quad \text{for } + \Delta I_o$$

$$\Delta V_o = \frac{L \Delta I_o^2}{C V_o} \quad (25) \quad \text{for } - \Delta I_o$$

From these two expressions the dependence of overshoots and undershoots on the L and C values may be observed. To minimize ΔV_o it is therefore necessary to reduce the inductance value L and to increase the capacitance value C. Should other auxiliary functions be required in the circuit like reset or crowbar protections and very variable loads may be present, it is worthwhile to take special care for minimizing these overshoots, which could cause spurious operation of the crowbar, and the undershoot, which could trigger the reset function.

DEVICE DESCRIPTION

Fig. 4 shows the package in which the device is mounted and the pin function assignments.

The internal structure of the device is shown in fig. 5. Each block will now be examined.

Power supply

The device is provided with an internal stabilized power supply that, besides supplying the reference

voltage of 5.1V for the whole system, also supplied the internal analog blocks.

Special features of the voltage reference are its accuracy, temperature stability and high line rejection. Through zenze-zap trimming, the voltage is within $\pm 2\%$ limits.

Figure 4 : Pin Assignments of the L296.

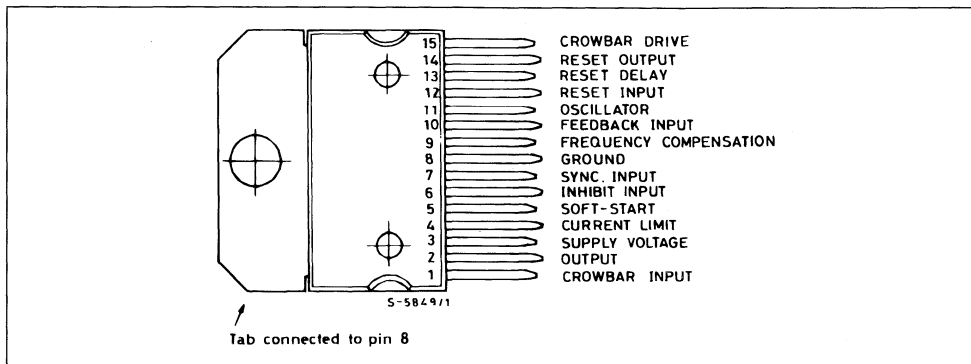
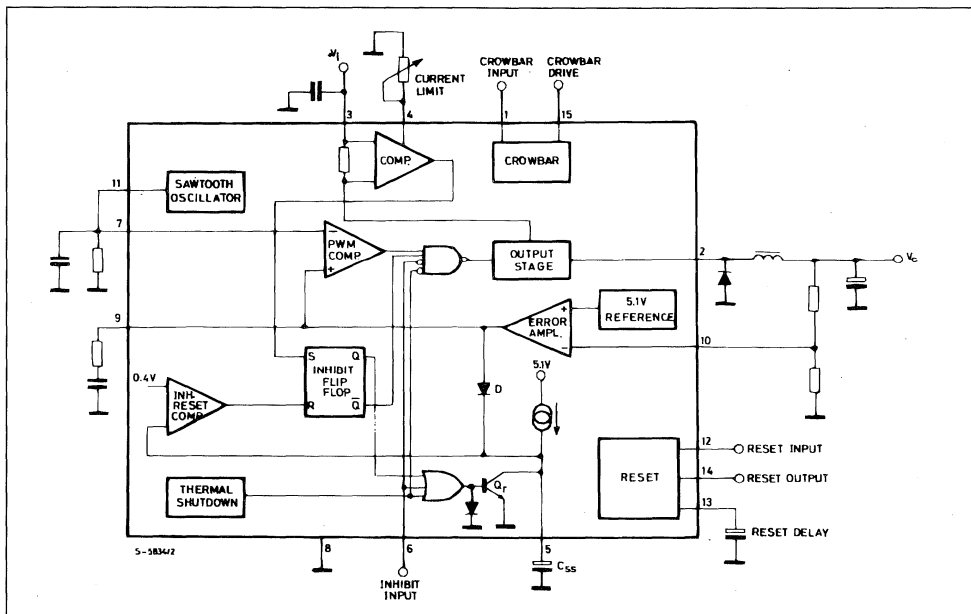


Figure 5 : Block Diagram of the L296. In Addition to the Basic Regulation Loop the Device includes Functions such as Reset, Crowbar and Current Limiting.



OSCILLATOR

The oscillator block generates the saw-tooth waveform that sets the switching frequency of the system. This signal, compared with the output voltage of the error amplifier, generates the PWM signal to be sent to the power output stage. The saw-tooth, whose amplitude is between 1.2V and 3.2V, is generated by charging rapidly the C_{OSC} capacitor which then discharges across the R_{OSC} resistance. As shown in fig. 6, the oscillator is realized by a comparator (with grounded compatible input) with hysteresis whose thresholds are 1.2V and 3.2V respectively. The C_{OSC} capacitor and the R_{OSC} resistance are connected to the non-inverting input of the comparator which set the oscillating frequency is fixed. When the voltage on pin 11 is less than 3.2V, the switch S_1 is closed and the current generator charges the C_{OSC} capacitor rapidly ; in this phase S_2 is also closed. As soon as 3.2V is reached the comparator output drives S_2 open (therefore opening S_1 , too) ; the inverting input voltage is reduced to about

1.2V and the capacitor starts to discharge itself across the R_{OSC} resistor (the I_{bias} effect is neglected). When the voltage reaches 1.2V, S_2 and S_1 close again and a new cycle starts. The generated waveform is shown in fig. 7.

To achieve a good accuracy of the switching frequency it is essential to have a charging time of the capacitor which is much smaller than the discharging time. In this way, the oscillation frequency only depends on the external components C_{OSC} and R_{OSC} . For this reason the capacitor charging current (when S_1 is ON) is typically around 10mA. For example, with a 2.2nF capacitor to switch from 1.2V to 3.2V about 400ns is required, which is negligible compared to the 10 μ s period that occurs when the operation is performed at 100kHz. The diagrams shown in fig. 8 allow the calculation of the R_{OSC} value (R_1 in fig. 8) with C_{OSC} as a parameter (C_3 in fig. 8) when the oscillation frequency required for operation has been previously fixed.

Figure 6 : Internal Schematic of the Oscillator.

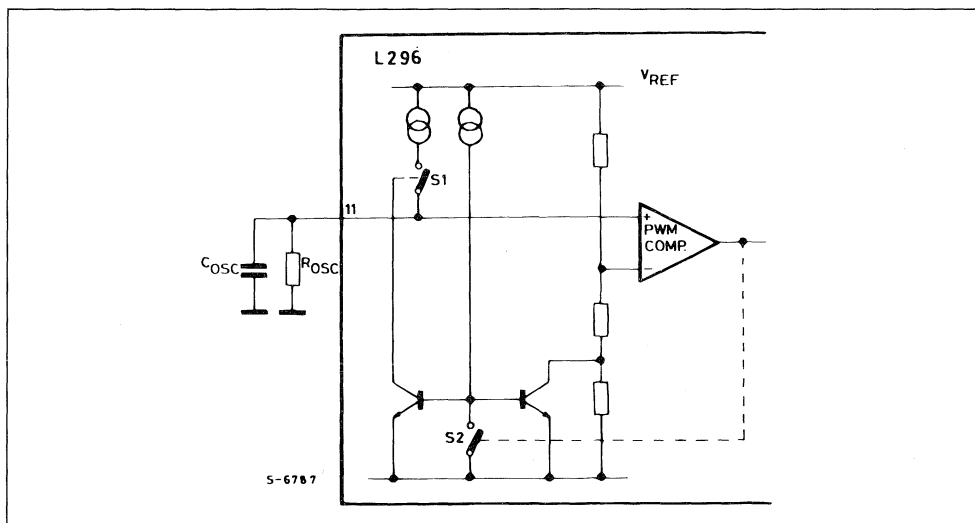


Figure 7a : Oscillator Waveform at Pin 11 with
 $f = 100\text{KHz}$ ($R_{OSC} = 4.3\text{K}\Omega$,
 $C_{OSC} = 2.2\text{nF}$).

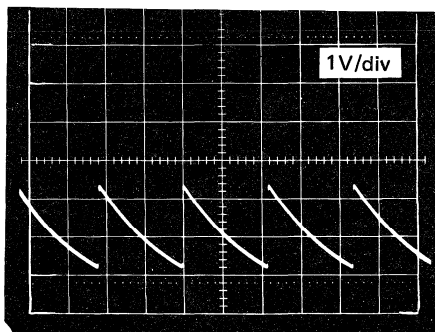


Figure 7b : Oscillator Waveform at Pin 11 with
 $f = 50\text{KHz}$ ($R_{OSC} = 9.1\text{K}\Omega$,
 $C_{OSC} = 2.2\text{nF}$).

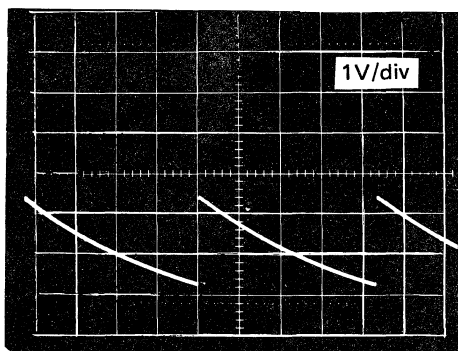


Figure 8 : Nomogram for the Choice of Oscillator Components.

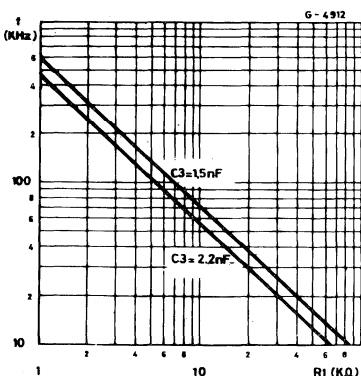


Fig. 8 shows two suggested values for the C_{OSC} capacitance. Excessively low capacitance value may give rise to an inaccuracy of the upper threshold due to the switching delays of the comparator. This inaccuracy is caused by an excessively short rise time of the voltage. A capacitance value too high gives rise to a charging time which is too compared to the discharging time. An additional inaccuracy cause would be therefore present for the switching frequency, now due to spread of the charge current.

The oscillation frequency is given by the following formula :

$$f_{osc} = \frac{1}{R_{OSC} C_{OSC}} \quad (26)$$

PWM (see fig. 9)

The PWM signal is generated on the comparator output ; the triangular-shaped waveform and the continuous signal coming from the output of the transconductance error amplifier are sent to its inputs. The PWM signal is then transferred to the driving stage of the output power transistor.

SOFT START (see fig. 9)

Soft start is an essential function for correct start-up, to prevent stresses and possible breakdown from occurring in the power transistor and to obtain a monotonically increasing output voltage.

In particular, the L296, as it does not have any duty cycle limitation and due to the type of current limitation does not allow the output to be forced to a steady state without the aid of the soft-start facility. Soft-start operates at the start-up of the system, after the inhibit has been activated, after an intervention of the current limitation and after the intervention of the thermal protection.

The soft-start function is realized through a capacitor connected to pin 5 which is charged at constant current ($\approx 100\mu\text{A}$) up to a value of about V_{REF} . During the charging time, through PNP transistor Q58, the voltage on pin 9 is forced to increase with the same rising speed as on pin 5. Starting from the discharged capacitor condition (pin 5 voltage = 0V) the power transistor is in the OFF condition, as the voltage on pin 9 is smaller than the minimum level of the ramp voltage. As the capacitor is charged, the PWM signal begins to be generated as soon as the error amplifier output voltage crosses the ramp ; the power stage starts to switch with steadily increasing duty cycle. This behaviour is shown in fig. 10. As soon as the steady condition is reached the duty cycle sets itself to the right value due to the effect of the feedback network while the soft-start capacitor completes its charging to a value very close to V_{REF} .

The soft-start effect is determined, apart from the switch-on time, when the current limitation operates, due to either an overload or a short circuit, to keep the mean value of the current absorbed by the power supply low.

Moreover from fig. 11 it may be observed that since the voltage on pin 9 can decrease under the mini-

mum ramp level and increase over the maximum level no limitations have been provided on the duty cycle, which therefore may vary between 0 and 100%.

Figure 9 : Partial Internal Schematic Showing PWM and Soft Start Blocks.

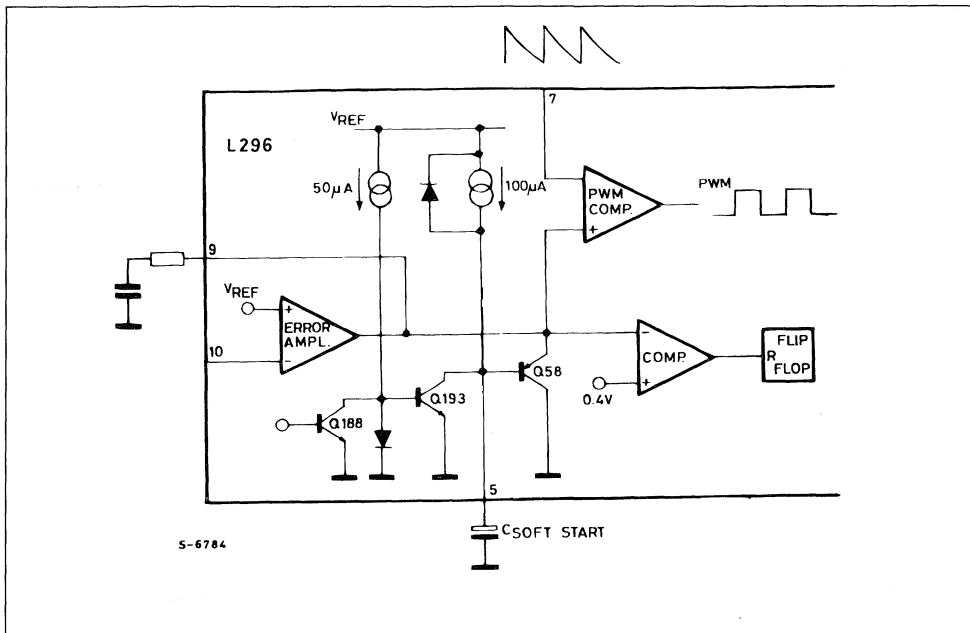
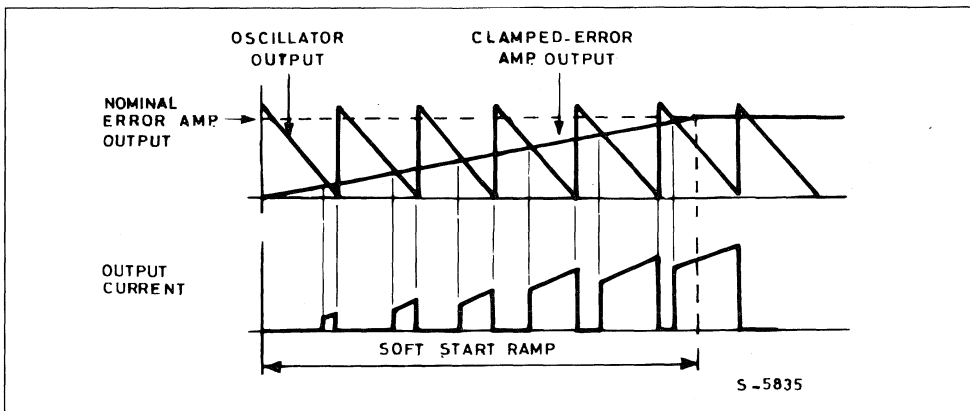


Figure 10 : Soft Start Waveforms. When power is applied, or after an inhibit, the L296's output current rises slowly under control of the soft start circuit.



cult to establish an exact maximum number of devices, as it depends on different conditions.

The first consideration concerns the accuracy which must be achieved and maintained on the oscillation frequency. Since the bias current on pin 7 is an output current, the sum of all the bias currents must be much smaller than the capacitor discharge current in close proximity to the lower discharge threshold. Therefore, assuming $C_{OSC} = 2.2\text{nF}$ and $R_{OSC} = 4.3\text{K}\Omega$, it follows that :

$$\frac{1.2\text{V}}{4.3\text{K}\Omega} = 280\mu\text{A}$$

Assuming that a 10% variation may be accepted, it follows therefore that the number of synchronizable devices is given by :

$$N = \frac{28\mu\text{A}}{I_{\text{bias max}}}$$

This means that if the overall I_{bias} is too high it may modify the discharging time of the capacitor.

The second consideration concerns the layout design.

In the presence of a great number of devices to be synchronized, the length of the paths may become significant and therefore the distributed inductance introduced along the paths may begin to modify the triangular shaped waveform, particularly the rising edge which is very steep. This effect would affect the devices that are physically located more distant from the master device.

The amplitude of the saw-tooth to be externally connected must be with in 0.5V and 3.5V, values also representing the maximum swing of the error amplifier output.

CURRENT LIMITATION

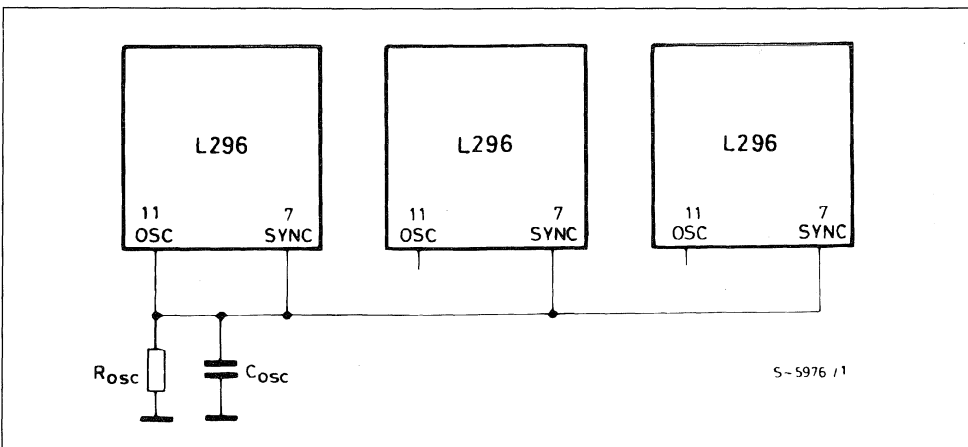
The current limitation function has been realized in a rather innovative way to avoid overload condition during the short circuit operation. In fact, while for all the other devices a constant current limitation is implemented by acting on the duty cycle (therefore, in short circuit conditions an output current is equal to the maximum limitation current), the new control approach allows operation in short circuit conditions with a mean current much smaller than the allowed 4A value. Operation of the current limiter will now be described.

Refer to the block diagram, fig. 13.

The current which is delivered from the output transistor to the load flows through the current sensing resistor R_S . When the voltage drop on R_S is equal to the offset voltage of the current comparator, the comparator generates a set pulse for the flip-flop, with a delay of about 1 μsec . The purpose of this delay is to avoid triggering of the protection circuit on the current peak that occurs during the recirculation phase. Therefore, the output Q goes low and the power stage is immediately switched off, while the output Q goes high and acts directly on the soft-start capacitor discharging the soft-start capacitor at a constant current (about 50 μA).

When the voltage on pin 5 reaches 0.4V the comparator triggers, supplying a reset pulse to the flip-flop ; from now on, the power stage is enable and the soft-start phase starts again. When the limitation cause, either overload or short circuit, is still present the cycle repeats again. The waveform of the output current on pin 2 is shown in fig. 14.

Figure 12 : In multiple supplies several L296's can be synchronized as shown here.



From fig. 14 it may be observed how this current limitation technique allows the short circuit operation with a very low output current value.

It is possible to reduce the maximum current value by acting on pin 4. On this pin a voltage of about

3.3V is present ; by connecting a resistance a constant current, given by $3.3/R$, is sent to ground. This current reduces the offset voltage of the current comparator, therefore anticipating its triggering threshold.

Figure 13 : Partial Schematic Showing the Current Limiter Circuit.

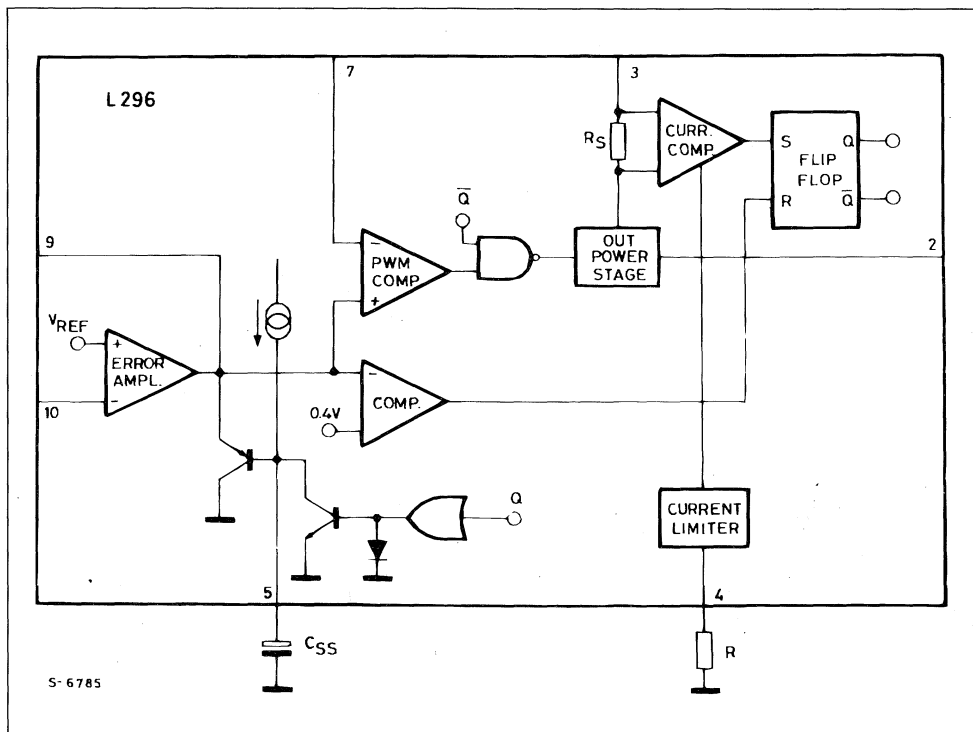


Figure 14a : Current Limiter Waveforms.

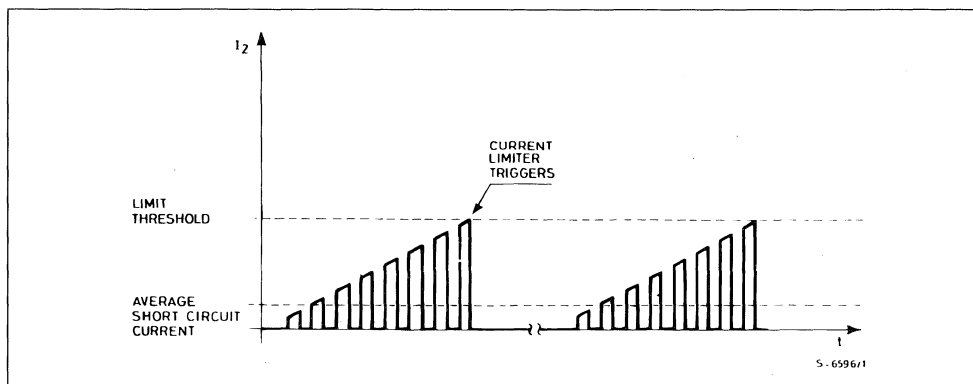


Figure 14b : Load Current in Short Circuit Conditions
($V_i = 40V$, $L = 300\mu H$, $f = 100K\Omega$).

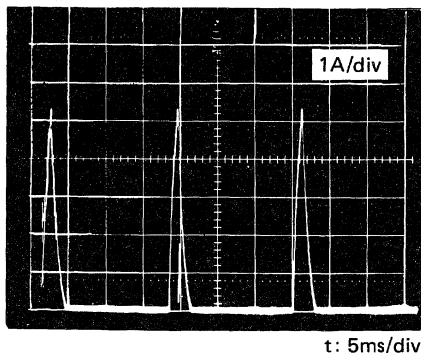
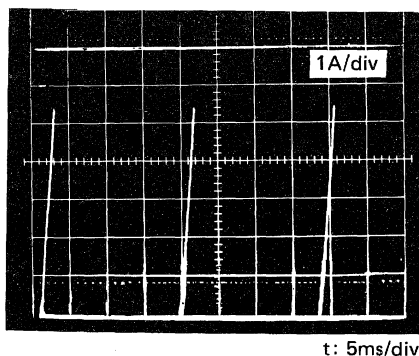


Figure 14c : Current at Pin 2 when the Output is Short Circuited.



RESET

The reset function is of great importance when the device is used to supply microprocessors, logic devices, and so on. This function differentiates the L296 device from all previous devices. The block diagram of the function is shown in fig. 15. A reset signal is generated when the output voltage is within

the limits required to supply the microprocessor correctly.

The reset function is realized through the use of 3 pins : the reset input pin 12, the reset delay pin 13 and the reset output pin 14. When the voltage on pin 12 is smaller than 5V the comparator output is high and the reset capacitor is not charged because the transistor Q is saturated and the voltage on pin 14 is at low level, since Q2 is saturated, too. When the voltage on pin 12 goes above 5V, the transistor Q switches OFF and the capacitor can start to charge through a current generator of about $100\mu A$. When the voltage on pin 13 goes above 4.5V the output of the related comparator switches low and the pin 14 goes high. As the output consists of an open collector transistor, a pull-up external resistance is required. In contrast, when the reset input voltage goes below 5V, less a hysteresis voltage of about 100mV, the comparator triggers again and instantaneously sets the voltage on pin 14 low, therefore forcing to saturation the Q1 transistor, that starts the rapid discharge of the capacitor. Obviously, the reset delay is again present when the voltage on pin 13 is allowed to go under 4.5V.

To achieve switching operations without uncertainties the two comparators have been provided with an hysteresis of about 100mV. In every operating condition the reset switching is guaranteed with a minimum reset input of 4.75V, the value required for correct operation of the microprocessor even in the presence of the minimum V_{REF} value.

Normally pin 12 is used connected to pin 10. When it is connected to the output, the function may be more properly called "reset" ; on the other hand, when it is connected through resistive divider, to the input voltage, the function is called "power fail". Fig. 16 and fig. 17 show the two possible usages.

The "power-fail" function is used to predict, with a given advance, the drop of the regulator output voltage, due to main failures, which is enough to save the data being processed into protected memory areas. Fig. 18 summarizes the reset function operation.

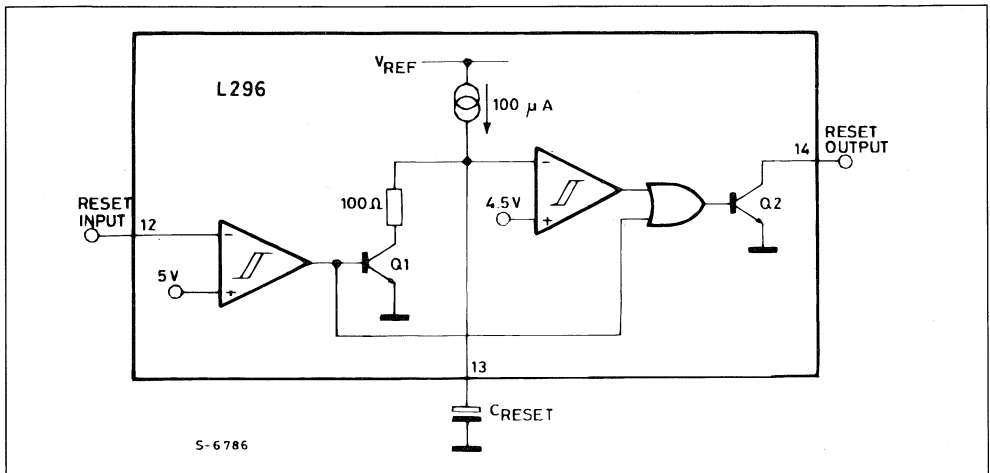
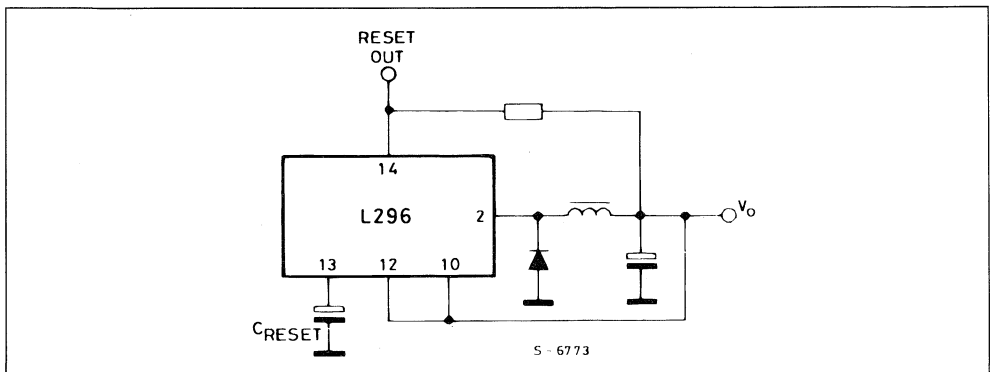
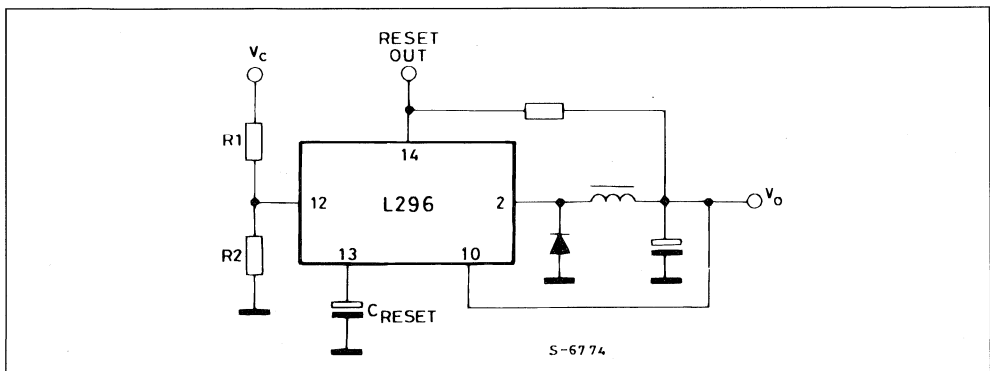
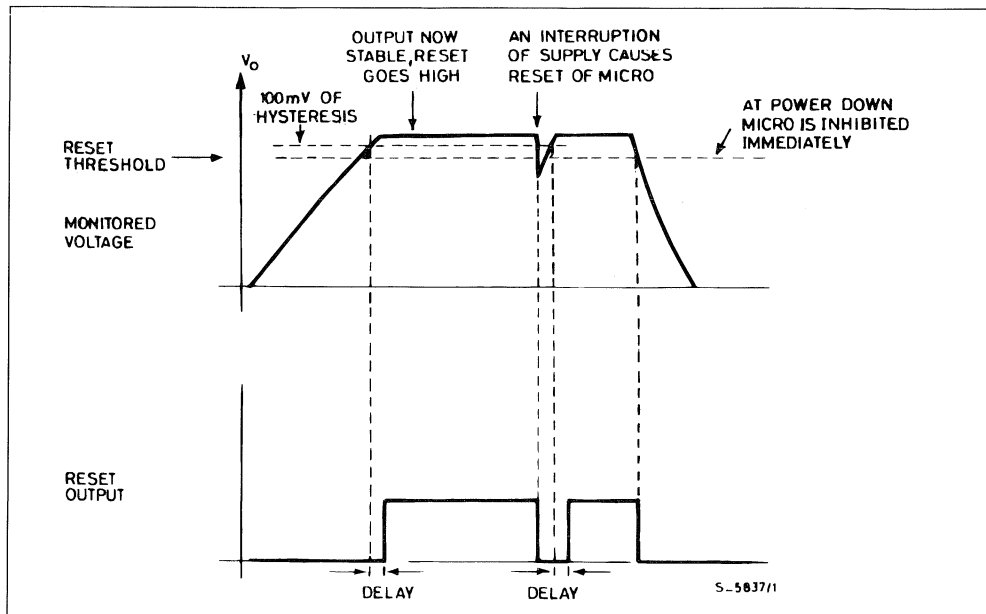
Figure 15 : Partial Schematic Showing Reset Circuit.**Figure 16 :** For Power - On reset the reset block is connected as shown here.**Figure 17 :** To obtain a power fail signal, the reset block is connected like this.

Figure 18 : Waveform of the Reset Circuit.

CROWBAR

This protection function is realized by a completely independent block, using pin 1 as input and pin 15 as output. It is used to prevent dangerous overvoltages from occurring when the output exceeds 20% of rated value. Pin 15 is able to output a 100mA current to be sent to the gate of a SCR which, triggering, short circuits either output or the input. When connected to the input, as the SCR is triggered a fuse in series connected to power supply is blown and to bring the system back to operation manual intervention is requested. Figs. 19, 20 and 21 show the different configurations.

When the voltage on pin 1 exceeds by about 20% the V_{REF} value the output stage is activated, which sends a current to the SCR gate, after a delay of about $5\mu\text{sec}$ to make the system insensitive to low-duration spikes. When activated, the output stage delivers about 100mA ; when not activated, it drains about 5mA and shows a low impedance to the SCR gate to avoid uncorrect triggering due to random noise. If the crowbar function is not used connect pin 1 to ground.

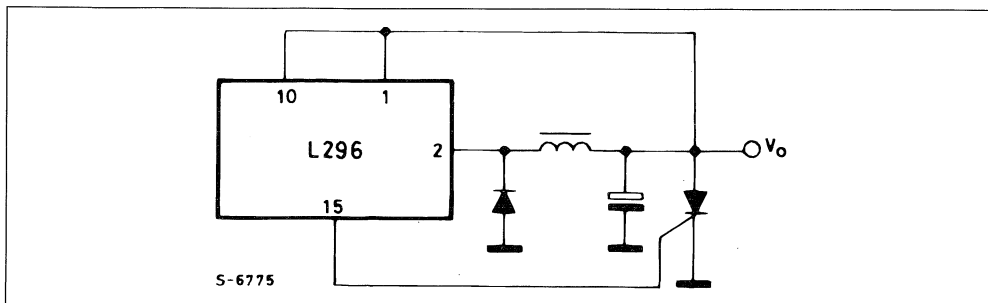
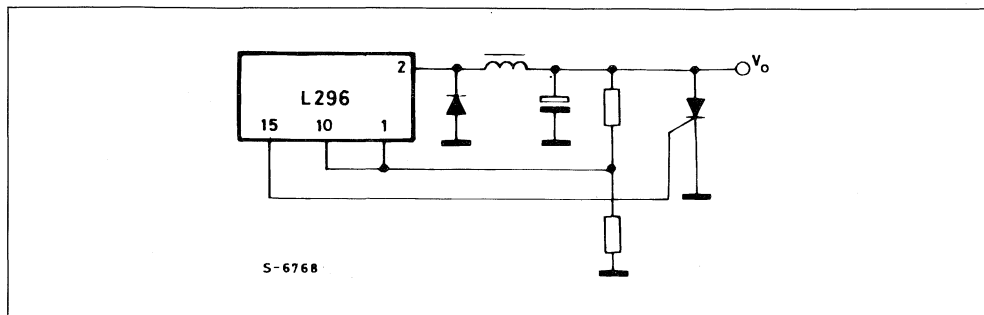
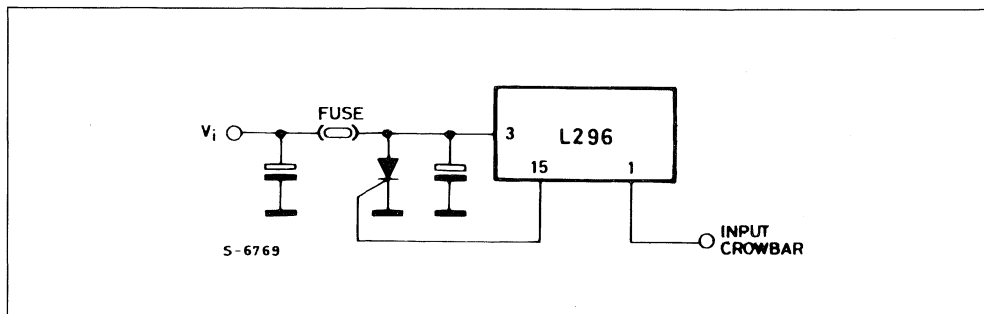
Figure 19 : Connection of Crowbar Circuit at Output for 5.1V Output Applications.

Figure 20 : Connection of Crowbar Circuit at Output for Output Voltages above 5.1V.**Figure 21** : Connection of Crowbar Circuit to Protect Input. When triggered, the scr blows the fuse.

INHIBIT

The inhibit input (pin 6) is TTL compatible and is activated when the voltage exceeds 2V and deactivated when the voltage goes under 0.8V. As may be seen in the block diagram, the inhibit acts on the power transistor, instantaneously switching it off and also acts on the soft-start, discharging its capacitor. When the function is unused, pin 6 must be grounded.

THERMAL PROTECTION

The thermal protection function operates when the junction temperature reaches 150°C ; it acts directly on the power stage, immediately switching it off, and on the soft-start capacitor, discharging it. The thermal protection is provided with hysteresis and, therefore, after an intervention has occurred, it is necessary to wait for the junction temperature to decrease of about 30°C below the intervention threshold.

APPLICATIONS

Though the L296 is designed for step-down regulator configurations it may be used in a variety of other

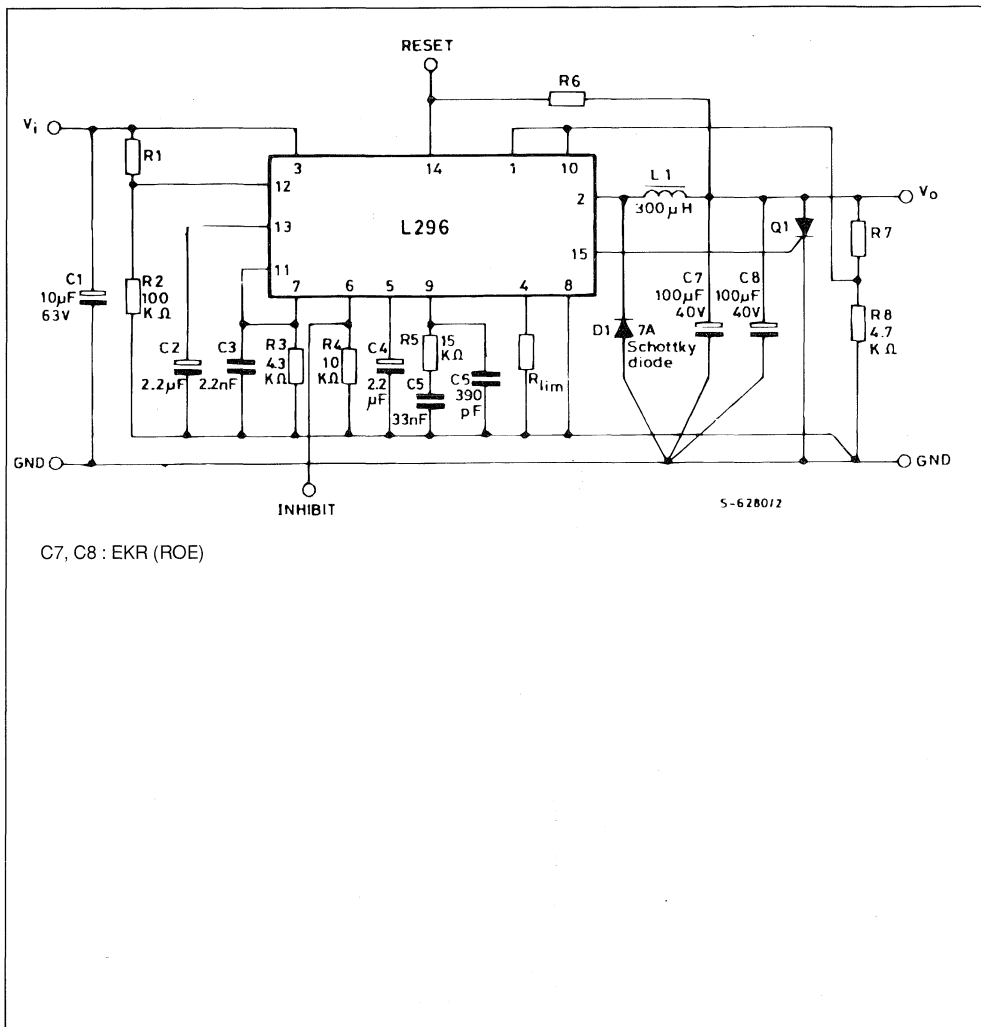
applications. We will now examine these possibilities and show how the capabilities of the device may be extended.

In fig. 22 the complete typical application is shown, where all the functions available on the device are being used. This circuit delivers to the load a maximum current of 4A and a voltage which is established by the voltage divider constituted by R_7 and R_8 resistances. The following table is helpful for a quick calculation of some standard output voltages :

Resistor Value for Standard Output Voltages		
V_O	R_8	R_7
12 V	4.7 k Ω	6.2 k Ω
15 V	4.7 k Ω	9.1 k Ω
18 V	4.7 k Ω	12 k Ω
24 V	4.7 k Ω	18 k Ω

To obtain $V_O = V_{REF}$ the pin 10 is directly connected to the output, therefore eliminating both R_7 and R_8 . The switching frequency is 100kHz.

Figure 22 : Schematic, PCB Layout and Suggested Component Values for the Evaluation Circuit used to characterize the L296. This is a typical stepdown application which exercises all the device's functions.



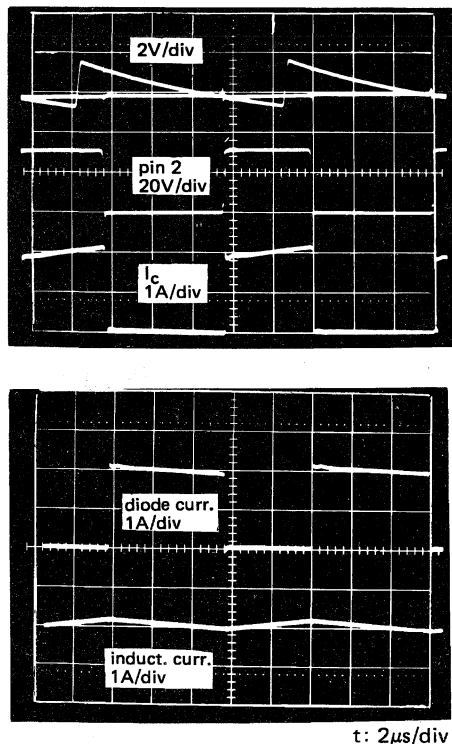
SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	
Thomson GUP 20 x 16 x 7	65	0.8 mm.	1 mm.

SUGGESTED INDUCTOR (L1) (continued)

Core Type	No Turns	Wire Gauge	Air Gap
Siemens EC 35/17/10 (B6633 & - G0500 - x 127)	40	2 x 0.8 mm.	
VOGT 250 μH Toroidal Coil, Part Number 5730501800			

Figure 23 : Oscilloscope Photographs Showing Main Waveform of the Figure 22 Circuit.



The oscilloscope photographs of the main waveforms are shown in fig. 23. The output voltage ripple ΔV_o depends on the current ripple in the coil and on the performance of the output capacitor at the switching frequency (100kHz). A capacitor suitable for this kind of application must have a low ESR and be able to accept a high current ripple, at the working frequency. For this application the Roederstein EKR series capacitors have been selected, designed for high frequency applications (>200kHz) and manufactured to show low ESR value and to accept high current ripples. To minimize the effects of ESR,

two 100μF/40V capacitors have been connected in parallel. The behaviour of the impedance as a function of frequency is shown in fig. 24.

Also the selection of the catch diode requires special care. The best choice is a Schottky diode which minimizes the losses because of its smaller forward voltage drop and greater switching frequency rate. A possible limitation comes from the backward voltage, that generally reaches 40V max.

When the full input voltage range of the device is required in this application it is possible to use super fast diodes with 35 to 50ns rated recovery time, where no more problems on the backward voltage occur (on the other hand, they show a greater forward voltage). The use of slower diodes, with $t_{rr} = 100$ ns or more is not recommended; The photographs in fig. 25 show the effects on the power current and on the voltage on pin 2, due to the diodes showing different speeds. Diodes showing t_{rr} greater than 35-50ns will reduce the overall efficiency of the system, increasing the power dissipated by the device.

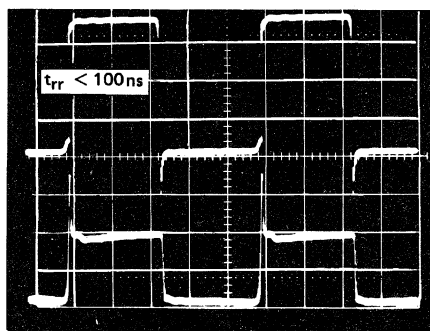
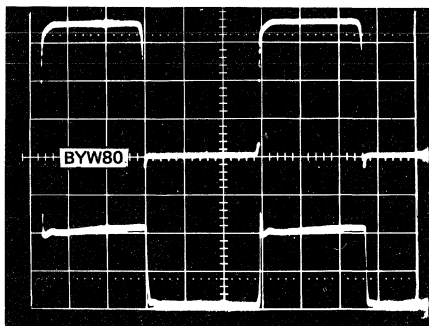
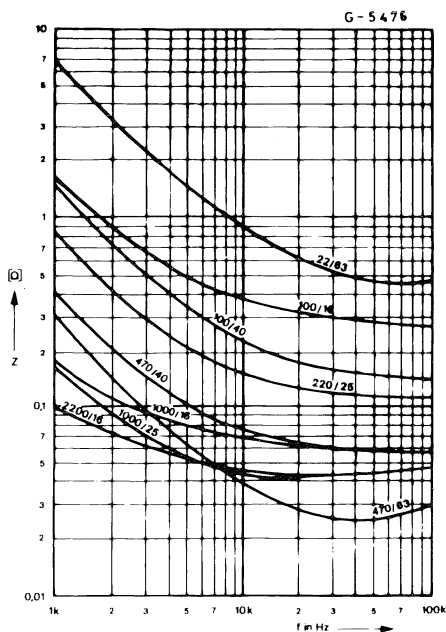
The third component requiring care is the inductor. Fig. 22a shows the part numbers of some types used for testing. Besides having the required inductance value, the coil has to show a very high saturation current.

Therefore, a correct dimensioning requires a saturation current above the maximum value of I_{2L} , the current limit threshold.

To achieve high saturation with ferrite cores an air gap between the two core halves must be provided; the air gap causes a leakage flux which is radiated in the surrounding space. To better limit this phenomenon "pot cores" may be used, whose geometry is such to better limit the flux radiated to the outside. Using toroidal cores, for instance of Magnetic 58930-A2 moly-permalloy kind, both the requirements of high saturation and low leakage flux are satisfied. The saturation is softer that the saturation shown by the ferrite materials. The air gap is not concentrated in one area, but is finely distributed along the whole core; this gives the low leakage flux value.

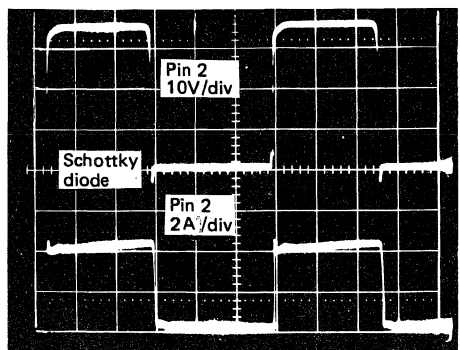
Careful selection of the external components therefore allows the realization of a power supply system whose benefits are significant when compared to a system with the same performance but realized with the linear technique.

Figure 24 : Typical Impedance/Frequency curves for EKR Capacitors.



t: 2 μ s/div

Figure 25 : Oscilloscope Photographs Showing the Waveform obtained with Diodes having Different t_{rr} Values.



t: 2 μ s/div

LOW COST APPLICATION AND PREREGULATOR

Fig. 26 shows the low cost application of a 4A and $V_o = 5.1V$ power supply. A minimum amount of essential external components is required, which are necessary for correct operation. It is impossible to save other components, specially the soft-start capacitor. Without soft-start, the system cannot reach the steady state and there is also a serious risk of damaging the device.

This application is very well suited not only as a low-cost power supply, but also as pre-regulator for post-regulators distributed in different circuit points, or even on different boards (fig. 27). The post-regulators may be selected among the low-drop types, like L4805 and L387 for example, still obtaining a high efficiency, combined with an excellent regulation. The use of L387 device allows us to use also the reset function, useful to power a microprocessor.

SWITCHING vs LINEAR

Switching regulators are more efficient than linear types so the transformer and heatsink can be smaller and cheaper. But how much can you gain ?

We can estimate the savings by comparing equivalent linear and switching regulators. For example, suppose that we want a 4 A/5 V supply.

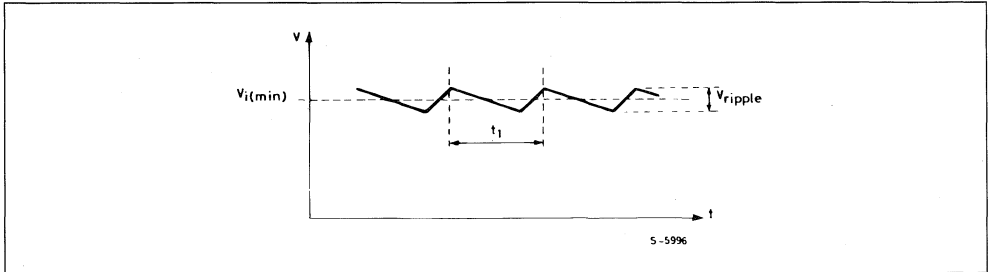
Linear

For a good linear regulator the minimum dropout will be at least 5V at 4A. The minimum input voltage is given by :

$$V_{i \min} = V_o + \frac{1}{2} V_{\text{ripple}}$$

where :

$$V_{\text{ripple}} \cong \frac{I_o t_1}{C} = \frac{4 \times 8 \times 10^{-3}}{10 \times 10^{-3}} = 3.2 \text{ V}$$



(a good approximation is 8ms for t_1 at mains frequency of 50Hz and 10.000 μ F for C, the filter capacitor after the bridge). Therefore $V_{i \min} \cong 1.6\text{V}$. Since operation must be guaranteed even when the mains voltage falls 20%, the nominal voltage on load at the terminals of the regulator must be :

$$V_{\text{nom}} = \frac{V_{i \min}}{0.8} = \frac{10.6}{0.8} = 13.25\text{V}$$

To allow even a small margin we have to choose :

$$V_{\text{nom}} = 14\text{V}$$

The power that the series element must dissipate is therefore :

$$P_d = (V_{\text{nom}} - V_o) I_o = 36\text{W}$$

and a heatsink will be necessary with a thermal resistance of :

$$R_{\text{th heats.}} = 0.8^\circ\text{C/W}$$

and the transformer must supply a power of :

$$P_{\text{diss}} = 14 \times 4 = 56\text{W}$$

It must therefore be dimensioned for :

$$PD = \frac{56}{0.9} = 62\text{VA}$$

Switching (L296)

Assuming the same nominal voltage (14V), the L296 data sheet indicates that the power dissipated in this case is only 7W. And this power is dissipated in two elements ; the L296 itself and the recirculation diode.

It follows that the transformer must be roughly 30VA and the heatsink thermal resistance about 11 $^\circ$ C/W.

	Linear	Switching
Transformer	62 VA	30 VA
Heatsink	0.8 $^\circ$ C/W	11 $^\circ$ C/W

This comparison shows that the L296 switching regulator allows a saving of roughly 50% on the cost of the transformer and an impressive 80-90% on the cost of the heatsink. Considering also the extra functions integrated by the L296 the total cost of active and passive components is roughly the same for both types.

Finally, it is important to note that a lower power dissipation means that the ambient temperature in the regulator enclosure can be lower - particularly when the circuit is enclosed in a box - with all the advantages cooler operation brings.

If for some reason it is necessary to use higher supply voltages the switching technique, and hence the L296, becomes even more advantageous.

Figure 26 : A Minimal Component Count 5.1V / 4A Supply.

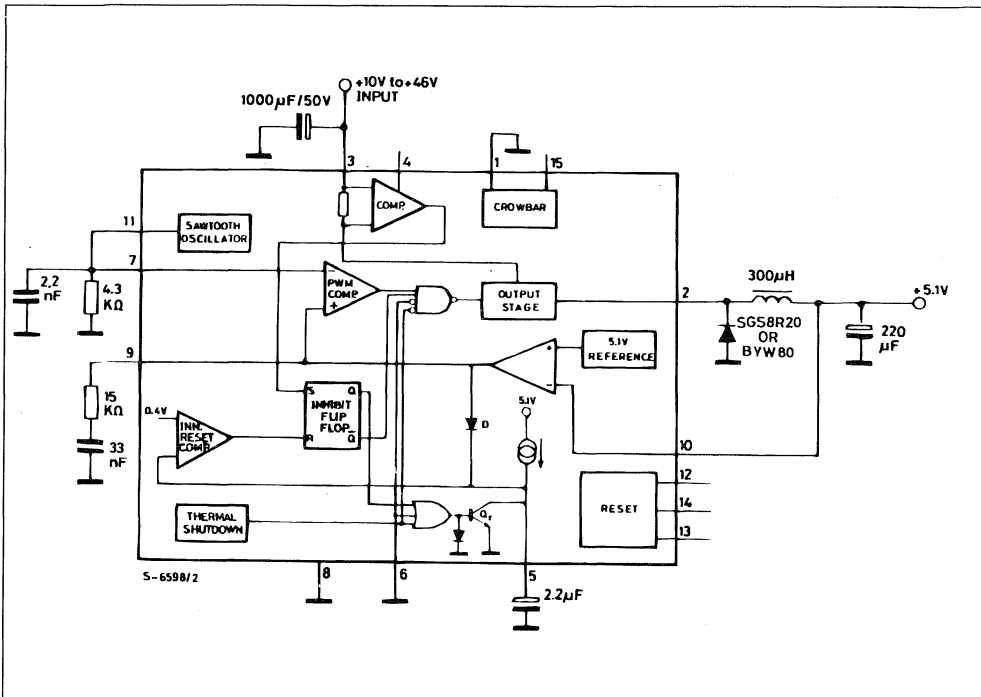
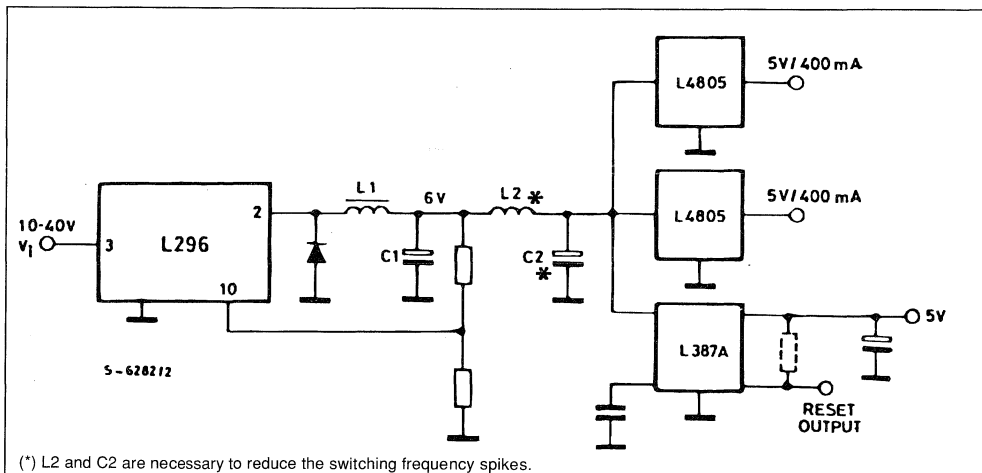


Figure 27 : The L296 may also be used as a preregulator in distributed supply systems.



POWER SUPPLY COMPLETE WITH TRANSFORMER

Fig. 28 shows a power supply complete of transformer, bridge and filter, with regulation on the output voltage from 5.1V to 15V.

As already stated above, the output capacitors have to show some special features, like low ESR and high current ripple, to obtain low voltage ripple values and high reliability. The input filter capacitors must not be neglected because they have to show excellent features, too, having to supply a pulsed current, required by the device at the switching frequency. The current ripple is rather high, greater than the load current. For this application, two parallel connected 3300 μ F/50V EYF (ROE) capacitors have been used.

POWER SUPPLY WITH MAINS SWITCHING PREREGULATOR

When it is desirable to eliminate the 50/60Hz transformer - in portable or volume-limited equipment - a

mains preregulator can be added to reduce the input voltage to a level acceptable for the L296.

In this case the pre-regulator circuit is connected to the primary of the transformer which now operates at the switching frequency and is therefore smaller and lighter.

Using a UC3840 which includes the feed-forward function it is possible to compensate mains variation within wide limits. The secondary voltage is therefore only affected by load variations. Using one or more L296s as postregulators, feedback to the primary is no longer necessary, reduces the complexity and cost of the transformer which needs only a single secondary winding.

Fig. 28A shows a multi-output supply with a mains preregulator.

Figure 28 : A Typical Variable Supply showing the Mains Transformer.

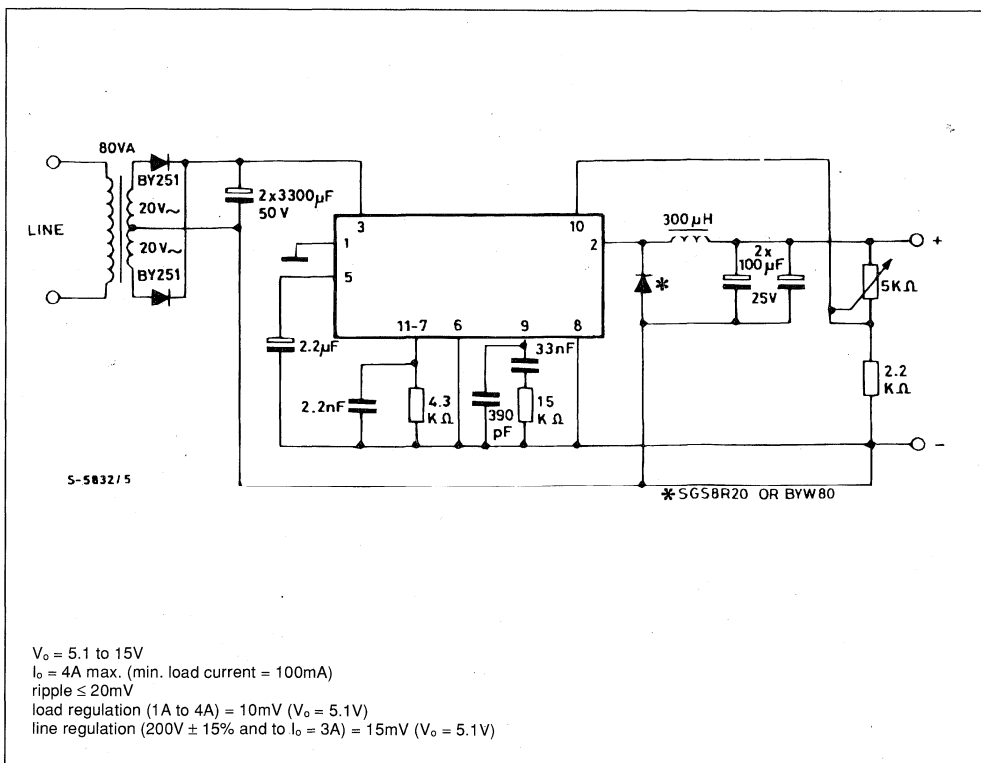
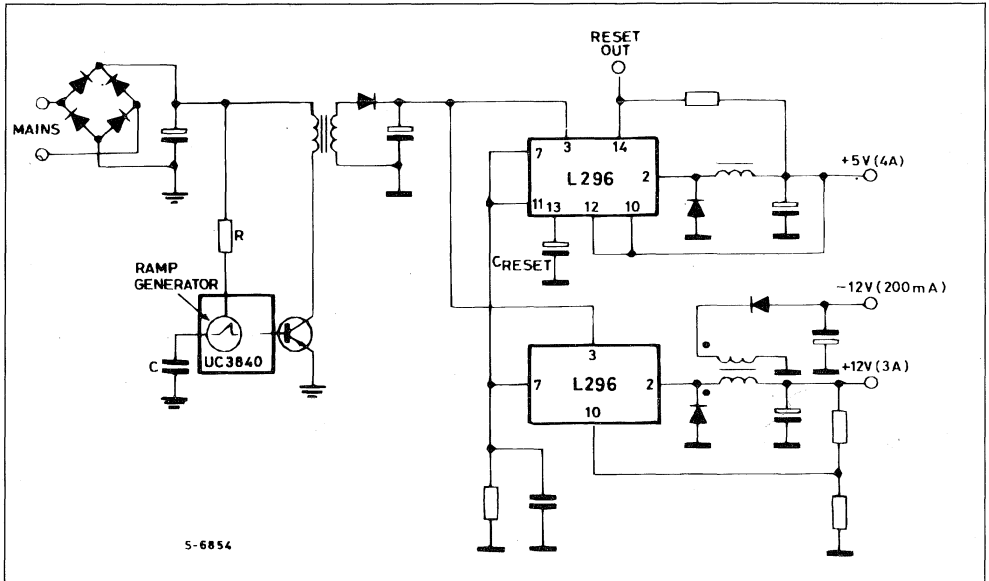


Figure 28A : A Multiple Output Supply using a Switching Preregulator rather than a Mains Transformer.

POWER SUPPLY WITH 0 - 30V ADJUSTABLE VOLTAGE

When output voltages lower than 5V are required, the circuit shown in fig. 29 may be used.

Calibration is performed by grounding the P1 slider. Acting on P2, the current which flows through the 10k Ω resistor is fixed at approximately 2.5mA to obtain an output voltage of 30V. The equivalent circuit is shown in fig. 30.

Acting now on the slider of P1, the current flowing through the divider may be varied. The new equivalent circuit is shown in fig. 31.

Reducing the current flowing, also the voltage drop across the 10k Ω resistance is reduced, together with V_o . When the current reaches zero, it follows that $V_o = V_{REF}$. When the voltage on the slider of P1 exceeds V_{REF} , the current starts to flow in opposite direction and V_o begins to decrease below 5V.

When $I_1 \times 10k\Omega = V_{REF}$ it follows that $V_o = 0$.

DUAL OUTPUT REGULATOR

The application shown in fig. 32 is specially interesting because it provides two output voltages. The first voltage, the main one, is directly controlled by the feedback circuit. The second voltage is obtained through an auxiliary winding.

It often happens, when microprocessors, logic devices etc., have to be power supplied, that a main 5V output and an auxiliary +12V or -12V output are required, the latter with lower current requirements (100 ÷ 200mA) and a stabilization level not excessively high. As the auxiliary power supply is obtained through a completely separated winding, it is possible to obtain either a positive or negative voltage (compared to the main voltage or also a completely isolated voltage. With V_i variable between 20V and 40V, $V_o = 5.1V$ and $I_o = 2.5A$, the auxiliary -12V/0.2A voltage is within a $\pm 2\%$ tolerance.

Figure 29 : Variable 0–30V supply illustrating how output voltages below 5.1V are obtained.

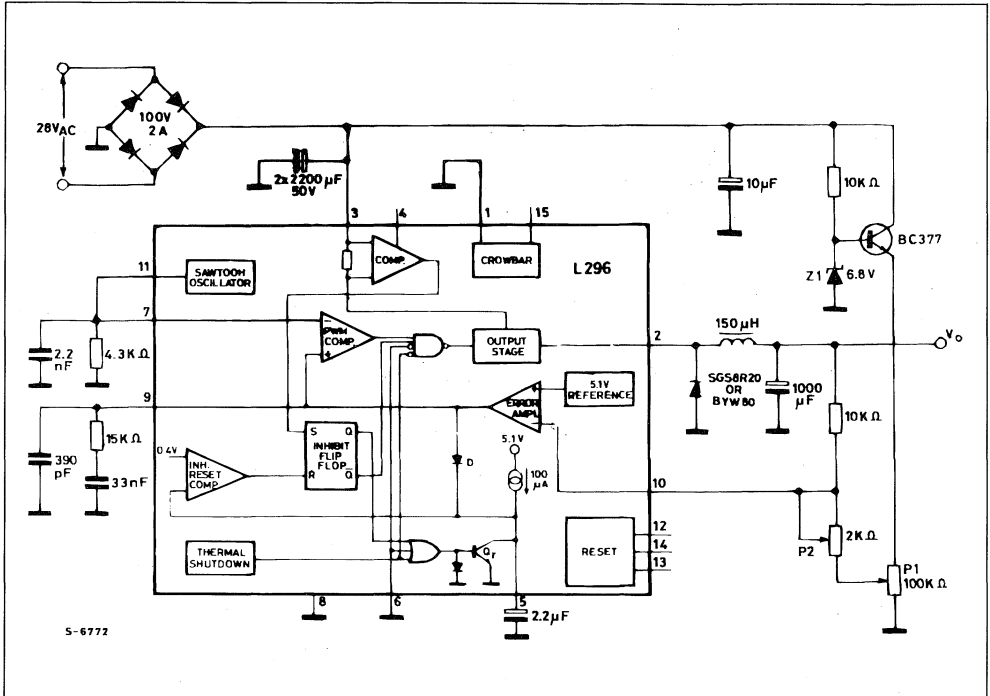


Figure 30 : When setting up the figure 29 circuit the slider of P1 is grounded, giving the equivalent circuit shown here, and P2 adjusted to give an output voltage of 30V.

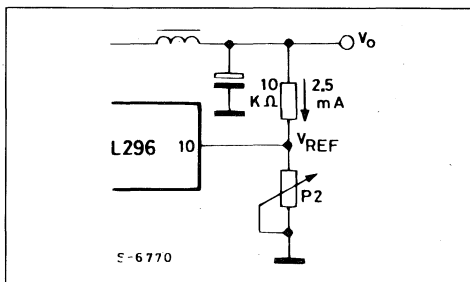


Figure 31 : Partial Schematic showing Output Voltage Adjustment of Figure 29.

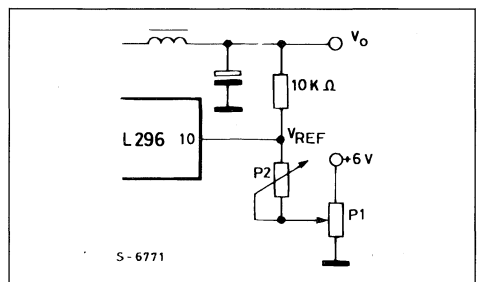
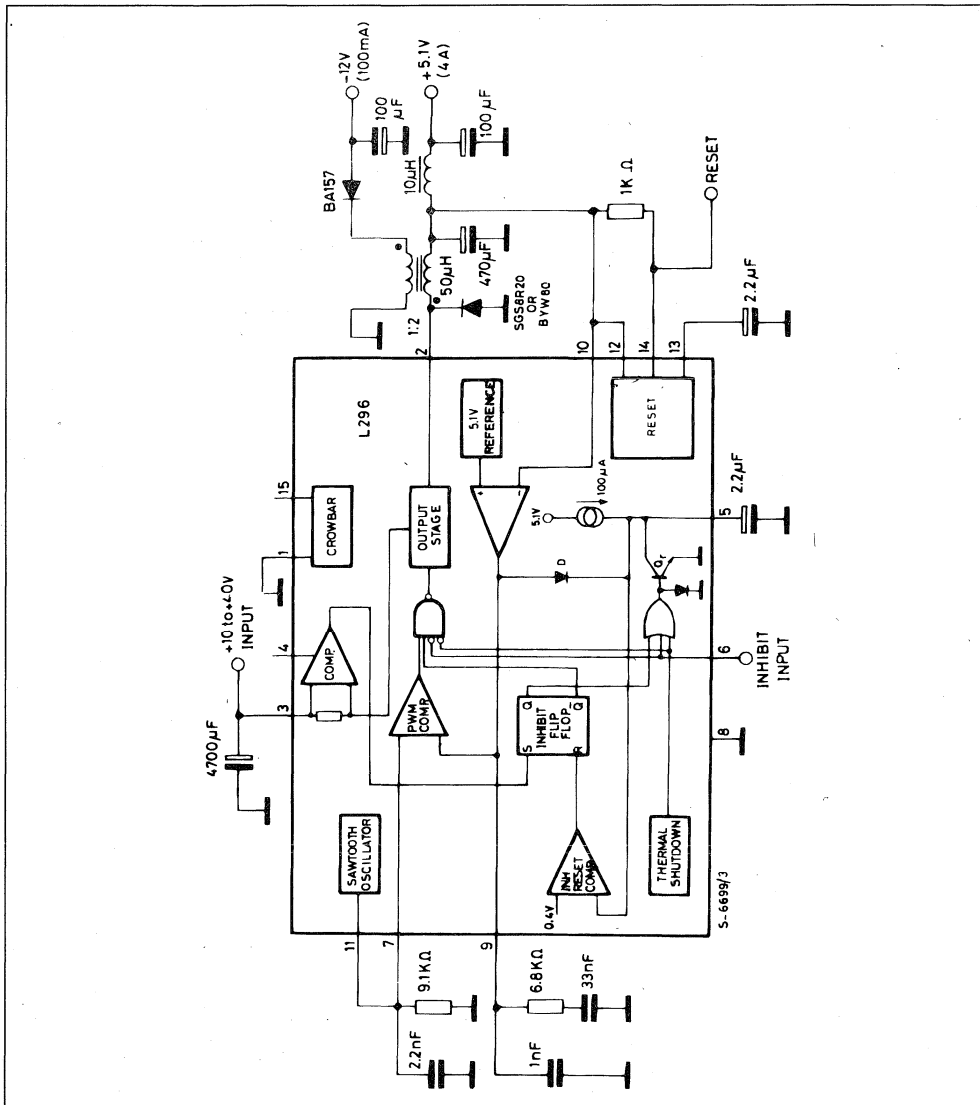


Figure 32 :Dual output regulator showing how an additional winding can be added to the inductor to generate a secondary output.



PERSONAL COMPUTER POWER SUPPLY

Using two mutually synchronized devices it is possible to obtain a four output power supply suitable for power a microprocessor system.

$$V_{O1} = 5.1V/4A$$

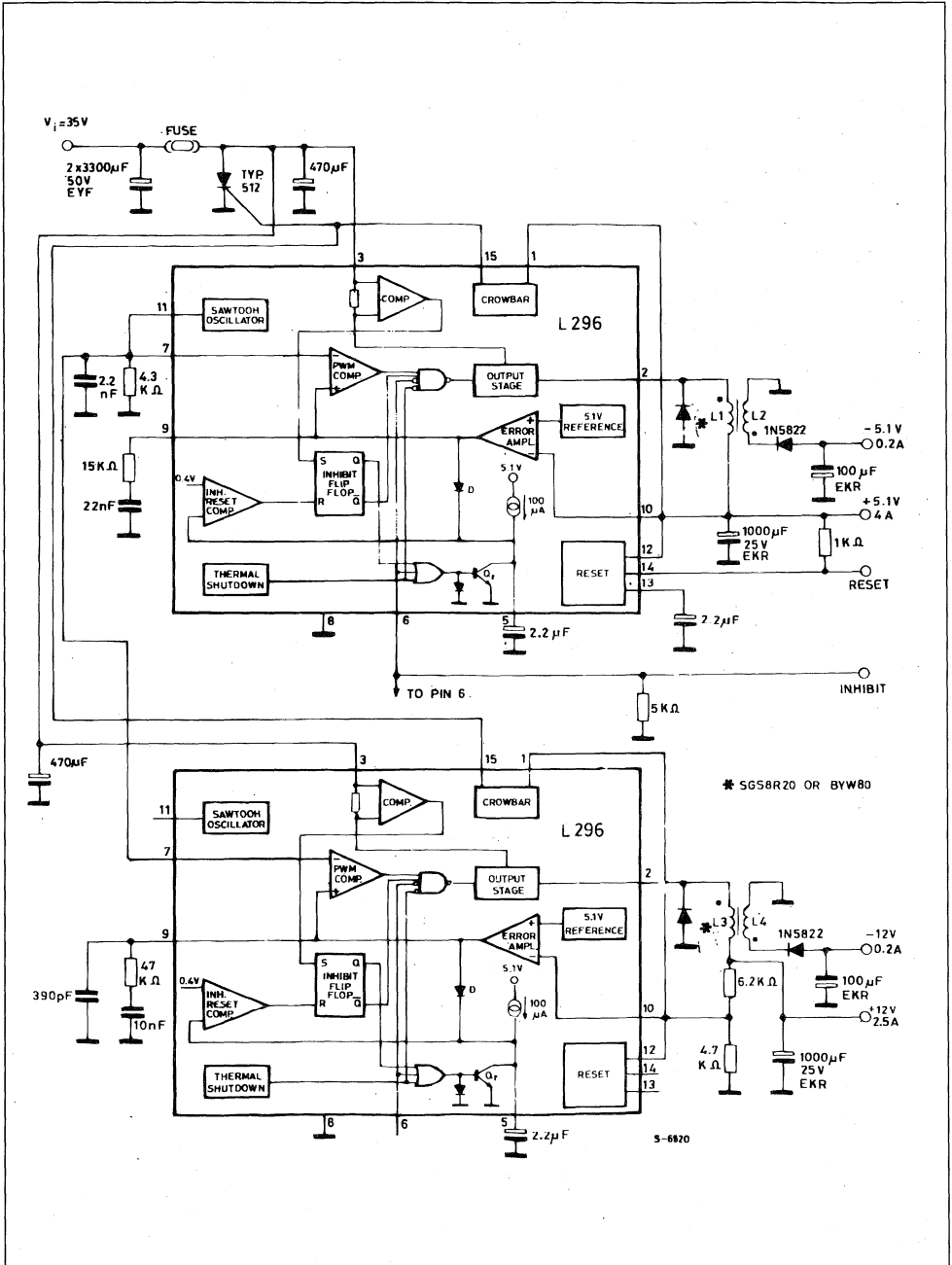
$$V_{O2} = 12V/2.5A \text{ (up to } 4A)$$

$$V_{O3} = -5V/0.2A$$

$$V_{O4} = -12V/0.2A$$

The schematic diagram is shown in fig. 33. The 5V output is also provided with the reset function, that is available also for the 12V output.

Figure 33 : Microcomputer Supply with 5V, -5V, 12V and -12V Outputs.



The feedback is direct, no other external component is used and no calibration is therefore required. An output is obtained with the accuracy of the reference voltage ($\pm 2\%$). For the 12 V output, by using a resistive divider with 1 % resistance an output is obtained whose spread is within $\pm 4\%$.

The two devices are mutually synchronized not to give rise to intermodulation which could generate unpleasant noise and, at the same time, a further component saving is achieved.

The crowbar function is implemented on both 5V and 12V outputs, using a single SCR connected to the input. The latter, by discharging to ground the electrolytic filter capacitors, blows the fuse connected in series with the devices power supply. In this way, should a faulty be present on either of the main outputs, the supply is switched off for whole system.

To inhibit both the devices with a single input signal, it is possible to connect the two inhibit inputs (pin 6) together ; the 5K Ω resistance is used when the inhibit input is left open. If this input is not used it must be grounded.

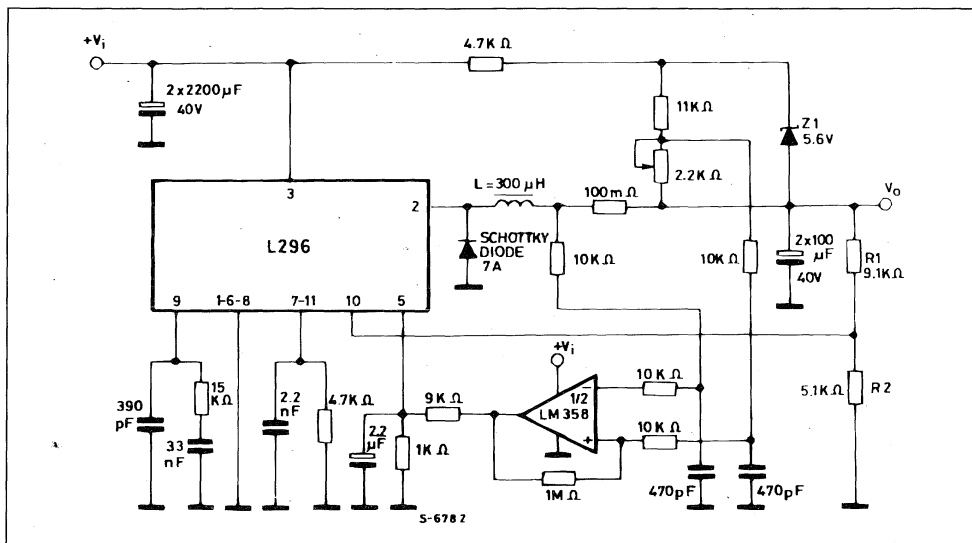
As may be noted in the diagram, to obtain the two auxiliary voltages is very simple and cost-effective.

It is suggested that the diodes are fast types ($\tau_{rr} < 50\text{nsec}$) ; should slower diodes be required some more turns have to be added to the auxiliary winding.

BATTERY CHARGER

When the device has to be used as current generator it is necessary to avoid the internal current limiter is operated. Fig. 34 shows the circuit realizing constant current limitation. In this way it is possible to obtain a 6V, 12V and 24V battery charger. For each of these voltages a max. current of 4A is available, which is large enough for batteries up to 40-45Ah (for 12V type). With reference to the electric diagram through the 2K Ω potentiometer the max output current is set, while through the R₁ – R₂ output divider the voltage is set. (R₁ may be replaced by either a potentiometer or a 3 position switch, to directly obtain the three 6V, 12V and 24V voltages).

Figure 34 : Battery charger circuit illustrating how the device is used to regulate the output current.



HIGHER INPUT VOLTAGE

Since a maximum input voltage of 46V (operating value) may be applied to the device the diagram shown in fig. 35 may be used when it is necessary to exceed this limit.

This system is particularly useful when operating at low output voltages. In this case a mean current I_{DC} which has a low value when compared to I_0 is obtained. In fact, since $V_0 = V_i (T_{ON}/T)$ and $V_0 I_0 = V_i I_{DC}$ (assuming the device has an ideal efficiency), it follows that $I_{DC} = I_0 (T_{ON}/T)$.

Assuming to be :

$$V_o = 5V \quad I_o = 4A \quad \text{and} \quad V_3 \approx 37V$$

it follows that :

$$T_{ON} / T = V_o / V_i = \frac{5}{37} = 0.135$$

$$I_{IDC} = 4 \times 0.135 = 0.54A.$$

With input voltage 50V and $I_o = 4A$, the external transistor dissipates about 7W. High good efficiency is still achieved, around 74% ; in the real case, considering also the device losses, an efficiency around 62% is achieved.

During output short circuits the external transistor is not overloaded because in this condition I_{IDC} re-

duces to values lower than 100mA. It is not possible to realize this application with series post-regulator because the efficiency would be unacceptably low.

MOTOR CONTROL

The L296 is also suitable for use in motor controls applications. Fig. 36 shows how to use the device to drive a motor with a maximum power of about 100W and provided with a tachometer generator for a good speed control.

Figure 35 : The maximum input voltage can be raised above 46V by adding a transistor as shown here.

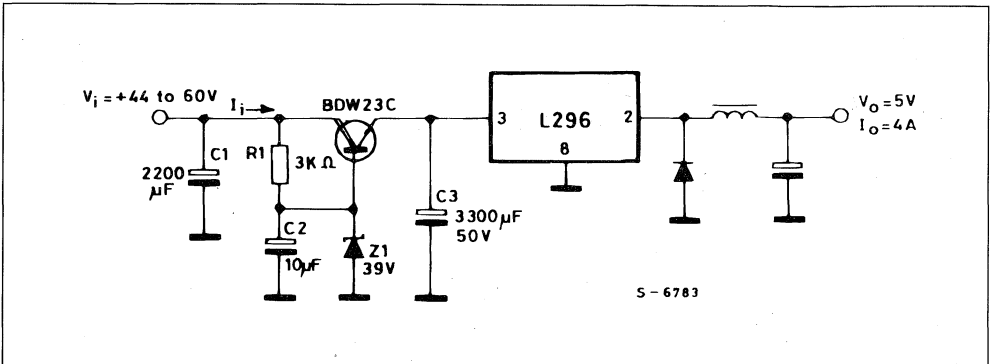
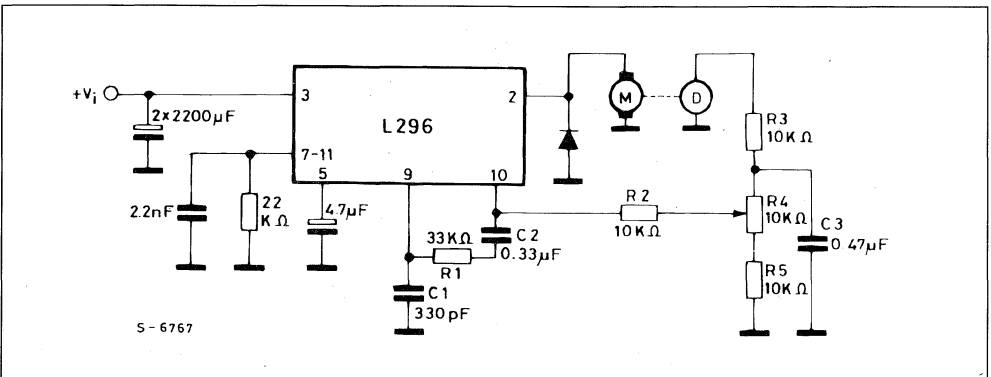


Figure 36 : With a tacho dynamo supplying feedback the L296 can be used as a motor speed controller.



HIGHER CURRENT REGULATORS

It is possible to increase the output current to the load above 4A through the use of an external power transistor. Fig. 37 shows a suitable circuit. The frequency is around 40kHz to prevent the device from losing excessive power due to switching on the external power.

The circuits shown in fig. 38 and fig. 39 show how current limitation may be realized in two different ways : through a sensing resistor connected in series with the collector of the external power transistor or through a current transformer.

In the first case, the sensing resistor is a low value resistor able to withstand the maximum load current required. The V_{CE} of the power transistor is higher than its V_{CEsat} ; when the resistor is connected in series to the collector V_{CE} is reduced ; consequently since the overall dissipated power is constant, the power dissipated by the sensing resistor is subtracted from that dissipated by the power transistor. The values indicated in figs. 38 and 39 realize adjustable current limitation for load currents around 10A.

Figure 37 : The output current may be increased by adding a power transistor as shown in this circuit.

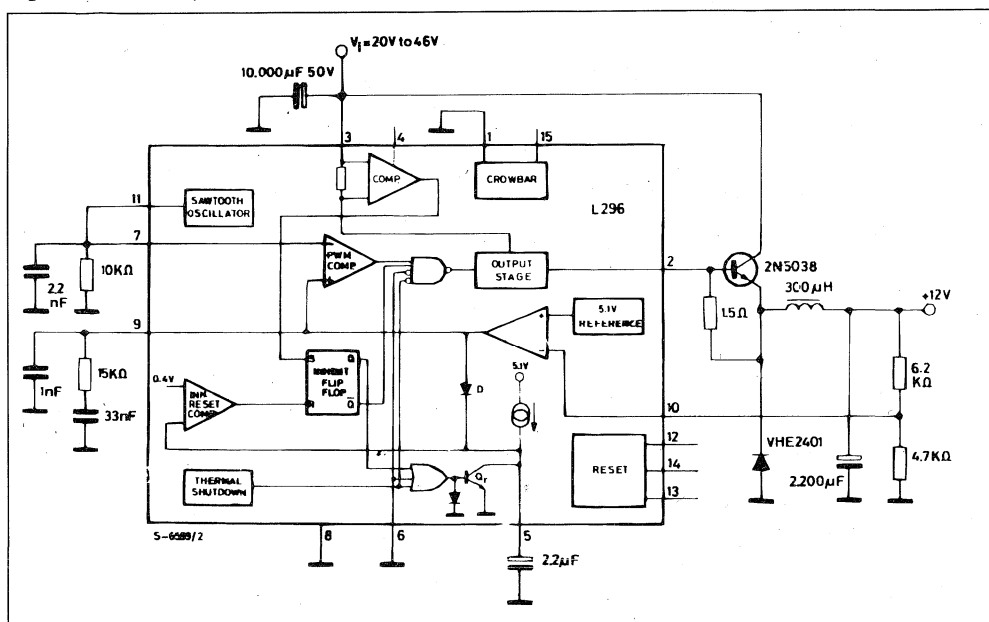


Figure 38 : This circuit shows how current limiting for the external transistor is obtained with a sensing resistor.

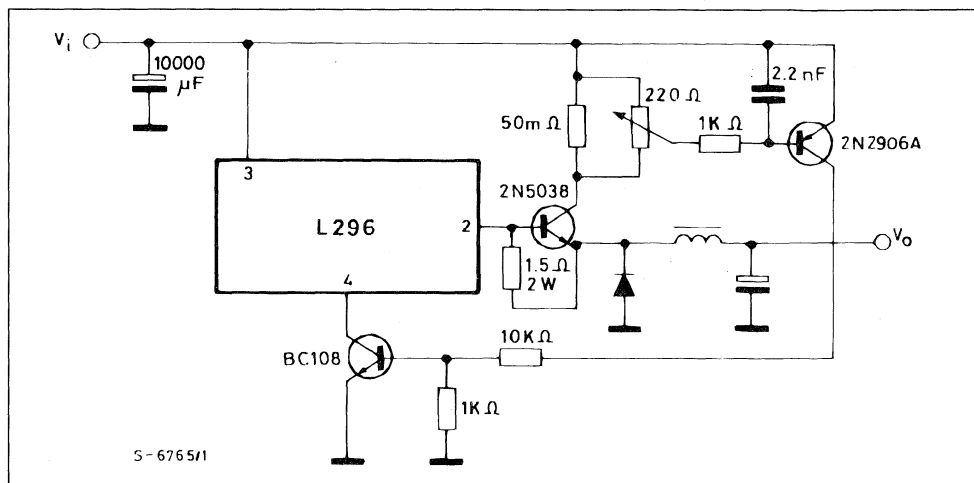
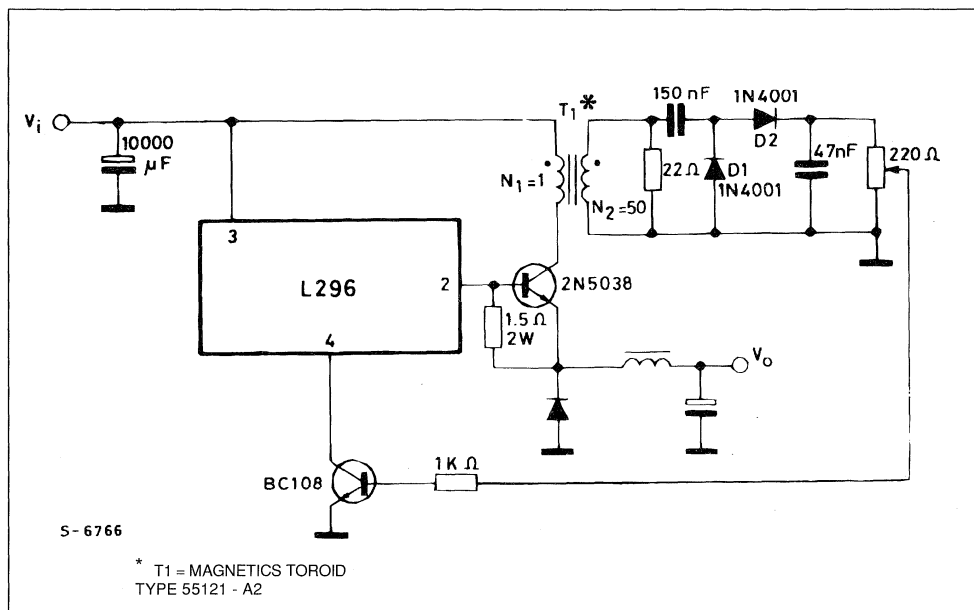


Figure 39 : A small transformer is used in this example for current limiting.



STEP-UP CONVERTER

With the L296 it is also easy to realize a step-up converter, by using a MOS power transistor. Fig. 40 shows the electric diagram of the step-up converter. The frequency is 100kHz, operation is in discontinuous mode and the device internal current limiter is used. Therefore no other external protection is required.

The input voltage could be a 12V car battery, from which an output voltage of 35V may be obtained. Lower output voltage of 35V may be obtained. Lower output voltage values may be obtained by reducing the value of R_7 .

Figure 40 : A Step-up Converter using a Power MOS Transistor.

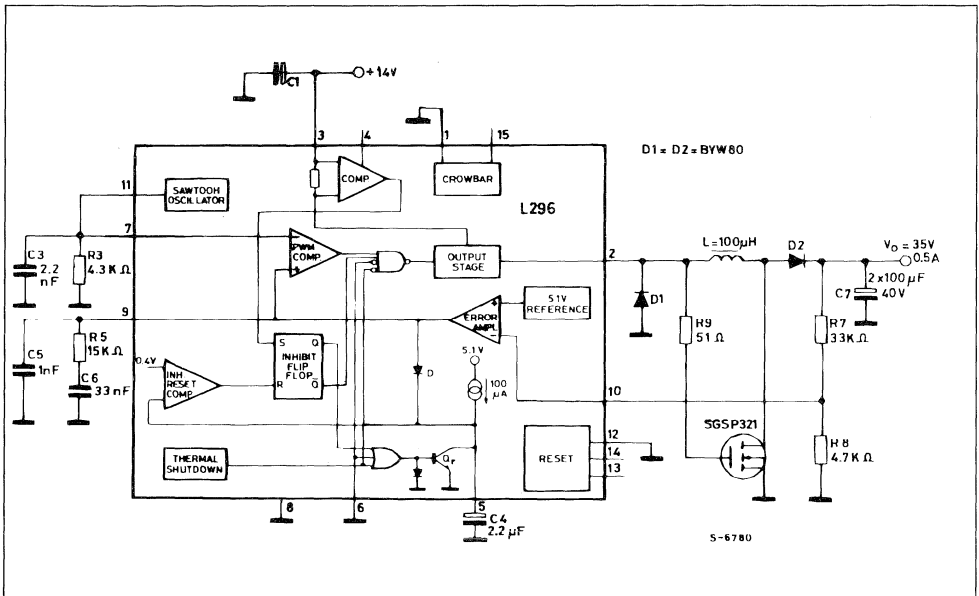
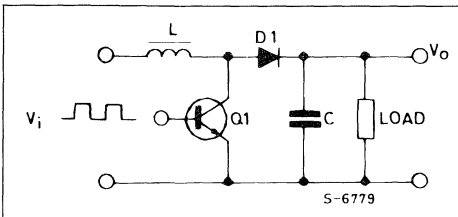


Figure 41 : Basic Schematic for Step-up Configurations.



In this configuration, unlike the step-down configuration, the peak current is not strictly related to the load current. The energy stored in the coil is suc-

DESCRIPTION OF OPERATION

Fig. 41 shows the diagram of the circuit realizing the step-up configuration.

When the transistor Q1 is ON, the inductance L charges itself with a current given by :

$$i_L = \frac{V_i}{L} t$$

The peak current in the coil is :

$$I_{\text{peak}} = \frac{V_i}{L} T_{\text{ON}}$$

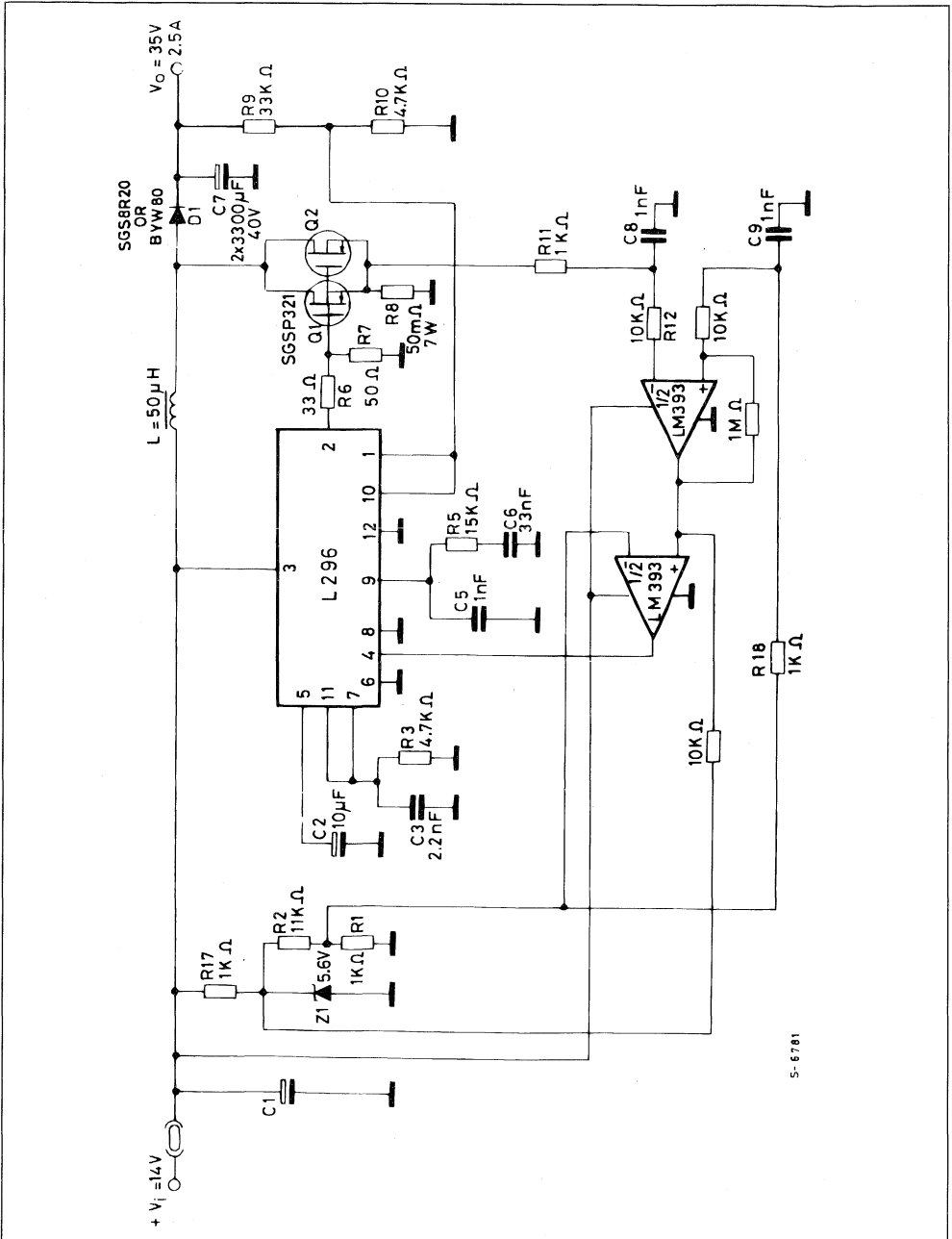
cessively discharged across the load when the transistor switches OFF. To calculate the I_o load current, the following procedure may be used :

$$\frac{1}{2} L I_{\text{peak}}^2 = V_o I_o T$$

$$I_o = \frac{L I_{\text{peak}}^2}{2 V_o T} = \frac{V_i^2 T_{\text{ON}}^2}{2 L V_o T}$$

For a greater output power to be available, the internal limitation must be replaced by an external circuit to protect the external power devices and to limit the current peak to a convenient value. A dual comparator (LM393) with hysteresis is used to avoid uncertainties when the current limitation operates. The electric diagram is shown in fig. 42.

Figure 42 : High power step-up converter showing how the current limiting function is realized externally.



LAYOUT CONSIDERATIONS

Both for linear and switching power supplies when the current exceeds 1A a careful layout becomes important to achieve a good regulation. The problem becomes more evident when designing switching regulators in which pulsed currents are over imposed on dc currents. In drawing the layout, therefore, special care has to be taken to separate ground paths for signal currents and ground paths for load currents, which generally show a much higher value.

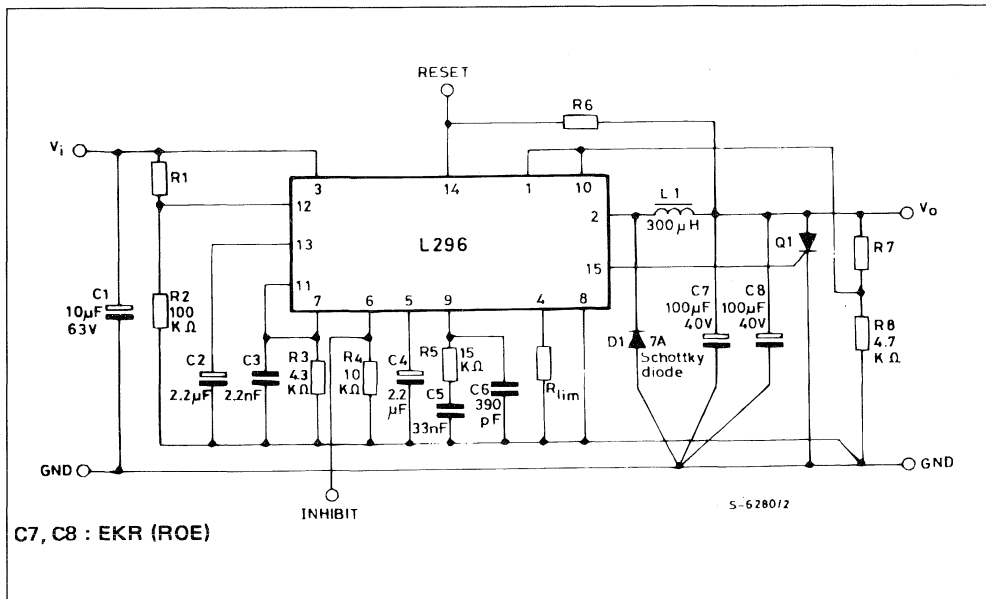
When operating at high frequencies the path length becomes extremely important. The paths introduce

distributed inductances, producing ringing phenomena and radiating noise into the surrounding space.

The recirculation diode must be connected close to pin 2, to avoid giving rise to dangerous extra negative voltages, due to the distributed inductance.

Fig. 43 and fig. 44 respectively show the electric diagram and the associated layout which has been realized taking these problems into account. Greater care must be taken to follow these rules when two or more mutually synchronized devices are used.

Figure 43 : Typical application circuit showing how the signal and power grounds are connected.



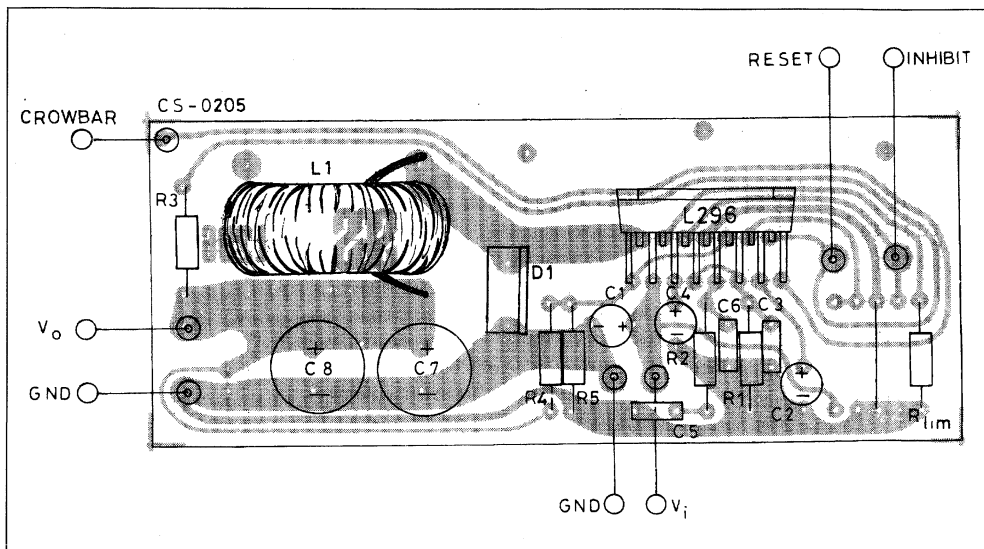
SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 - A2MPP	43	1.0 mm.	
Thomson GUP 20 x 16 x 7	65	0.8 mm.	1 mm.
Siemens EC 35/17/10 (B6633 & - G0500 - x 127)	40	2 x 0.8 mm.	
VOGT 250 µH Toroidal Coil, Part Number 5730501800			

Resistor Value for Standard Output Voltages

V _O	R ₈	R ₇
12 V	4.7 kΩ	6.2 kΩ
15 V	4.7 kΩ	9.1 kΩ
18 V	4.7 kΩ	12 kΩ
24 V	4.7 kΩ	18 kΩ

Figure 44 : A Suitable PCB Layout for the Figure 43 Circuit realized in Accordance with the Suggestions in the Text (1 : 1 scale).



HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reaching values which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150°C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150°C for long periods or of more than 170°C for short periods. In any case the temperature accelerates the ageing process and therefore influences the device life ; an increase of 10°C can halve the device life. A well designed heatsink should keep the junction temperature between 90°C and 110°C. Fig. 45 shows the structure of a power device. As demonstrated in thermo-dynamics, a thermal circuit can be considered to be an electrical circuit where R_1 , R_2 represent the thermal resistance of the elements (expressed in °C/W) (see fig. 46).

C_1 , C_2 are the thermal capacitance (expressed in °C/W)

I is the dissipated power

V is the temperature difference with respect to the reference (ground)

This circuit can be simplified as shown in fig. 47, where :

C_c is the thermal capacitance of the die plus that of the tab.

C_h is the thermal capacitance of the heatsink

R_{jc} is the junction case thermal resistance

R_h is the heatsink thermal resistance

Figure 45.

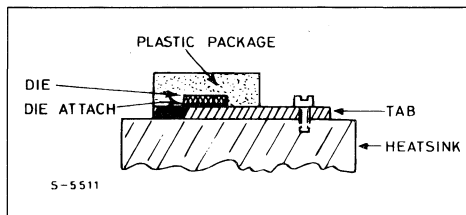


Figure 46.

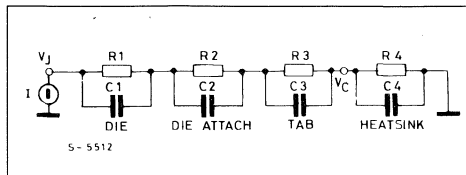
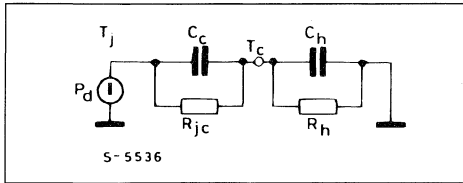
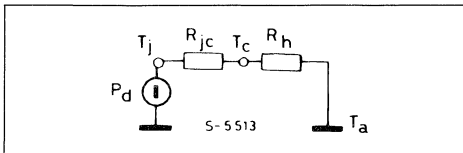


Figure 47.



But since the aim of this section is not that of studying the transistors, the circuit can be further reduced as shown in figure 48.

Figure 48.



If we now consider the ground potential as ambient temperature, we have :

$$T_j = T_a + (R_{jc} + R_h) P_d \quad a)$$

$$R_h = \frac{T_j - T_a - R_{jc} P_d}{P_d} \quad b)$$

$$T_c = T_a + R_h P_d \quad c)$$

Thermal contact resistance depends on various factors such as the mounting, contact area and planarity of the heatsink. With no material between the device and heatsink the thermal resistance is around 0.5°C/W ; with silicone grease roughly 0.3°C/W and with silicone grease plus a mica insulator about 0.4°C/W . See fig. 49. In application where one external transistor is used together, the dissipated power must be calculated for each component. The various junction temperature can be calculated by solving the circuit shown in fig. 50. This applies if the dissipating elements are fairly close with respect to the dissipator dimensions, otherwise the dissipator can no longer be considered as a concentrated constant and the calculation becomes dif-

ficult. This concept is better explained by the graph in fig. 51 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of heatsink and the same dissipated power. The graph in fig. 51 refers to the specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio of 3 between the two sides. The temperature jump will depend on the total dissipated power and on the devices geometrical positions. We want to show that there exists an optimal position between the two devices :

$$d = \frac{1}{2} \cdot \text{side of the plate}$$

Figure 49.

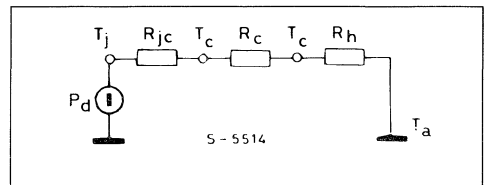


Figure 50.

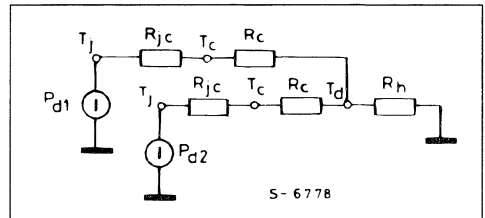


Fig. 52 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4). This graph may be useful in application with two L296 synchronized.

Figure 51.

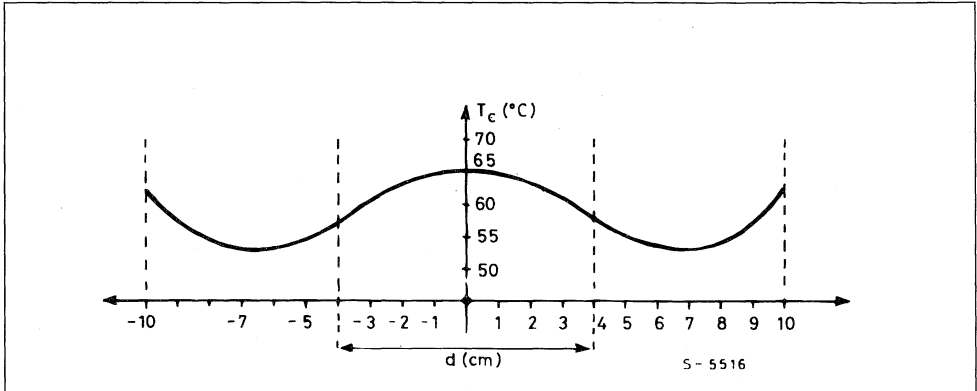
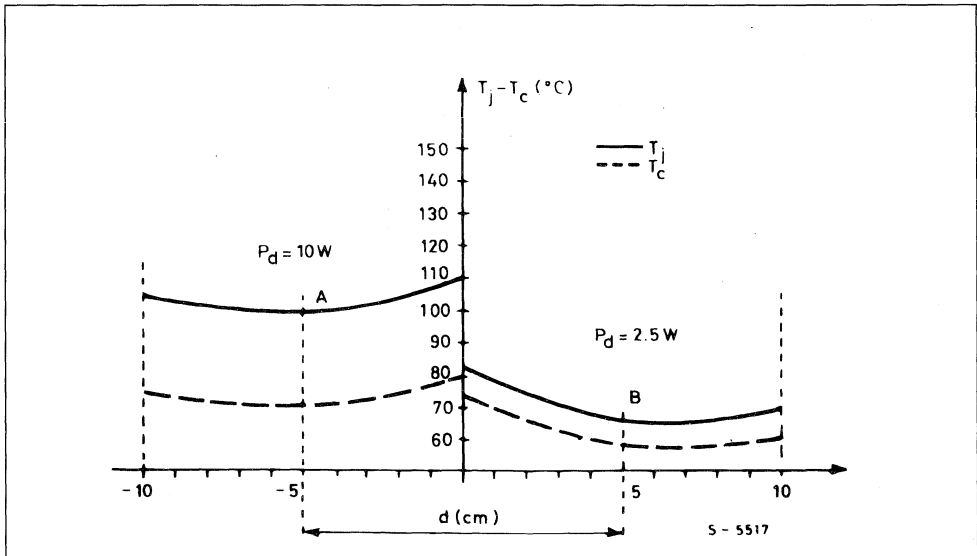


Figure 52.



APPENDIX A

CALCULATING SYSTEM STABILITY

This section is intended to help the designer in the calculation of the stability of the whole system.

Figure A1 shows the entire control system of the switching regulator.

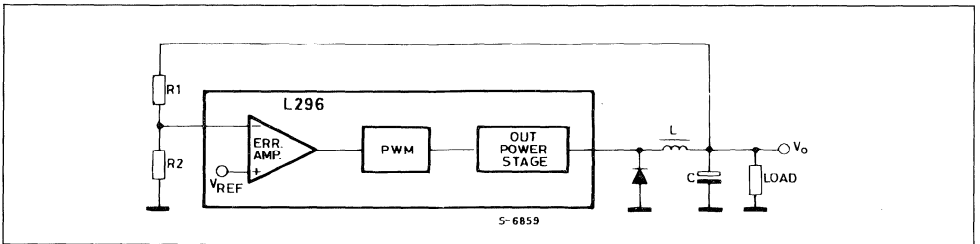
The problem which arises immediately is the transfer function of the PWM block and output stage, which is non-linear. If this function can be considered linear the analysis is greatly simplified.

Since the circuit operates at a constant frequency and the internal logic is fairly fast, the error introduced by assuming that this function is linear is minimized. Factors which could contribute to the non-linearity are an excessive delay in the output power transistor, ringing and parasitic oscillations generated in the power stage and non-linearity introduced by magnetic part.

In the case of the L296, in which the power transistor is internal and driven by well-controlled and efficient logic, the contribution to non-linearity is further reduced.

For the assumption of linearity to be valid the cut-off frequency of the LC filter must be much lower than the switching frequency. In fact, switching operation introduces singularities (poles) at roughly half the switching frequency. Consequently, as long as the LC filter is still dominant, its cut-off frequency must be at least an order of magnitude lower than the switching frequency. This condition is not, however, difficult to respect. The characteristics of LC filter affect the output voltage waveforms ; is generally much less than an order of magnitude below the switching frequency.

Figure A1 : The Control Loop of the Switching Regulator.



GAIN OF THE PWM BLOCK AND OUTPUT STAGE

The equation which links V_o to V_i is :

$$V_o = V_i \frac{T_{ON}}{T}$$

A variation ΔT_{ON} in the conduction time of the switching transistor causes a corresponding variation in the output voltage, ΔV_o , giving :

$$\frac{\Delta V_o}{\Delta T_{ON}} = \frac{V_i}{T}$$

Indicating with V_r the output voltage of the error amplifier, and with V_{ct} the amplitude of the ramp (the difference between the maximum and minimum values), T_{ON} is zero when V_r is at the minimum value and equal to T when V_r is at a maximum. Consequently :

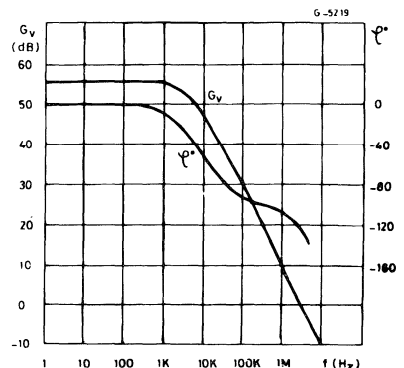
$$\frac{\Delta T_{ON}}{\Delta V_r} = \frac{T}{V_{ct}}$$

The gain is given by :

$$\frac{\Delta V_o}{\Delta V_r} = \frac{V_i}{V_{ct}}$$

Since V_{ct} is absolutely constant the gain of the PWM block is directly proportional to the supply voltage V_i .

Figure A2 : Open Loop Frequency and Phase Response of Error Amplifier.



The error amplifier is a transconductance amplifier (it transforms a voltage variation at the input into a current variation at the output). It is used in open loop configuration inside the main control loop and its gain and frequency response are determined by a compensation network connected between its output and ground.

In the application a series RC network is recommended which gives high system gain at low frequency - to ensure good precision and mains ripple rejection and a lower gain at high frequencies to ensure stability of the system. Figure A2 shows the gain and phase curves of the uncompensated error amplifier.

The amplifier has one pole at about 7kHz and a phase shift which reaches about -90° at frequencies around 1MHz.

The introduction of a series network $R_C C_C$ between the output and ground modifies the circuit as shown in figure A3.

Figure A4 shows the gain and phase curves of the compensated error amplifier.

Figure A3 : Compensation Network of the Error Amplifier.

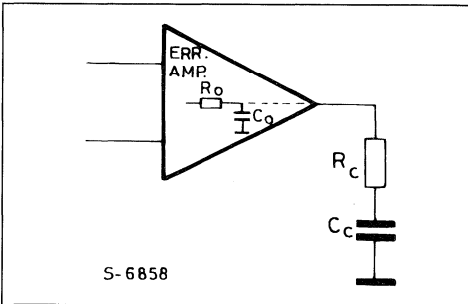
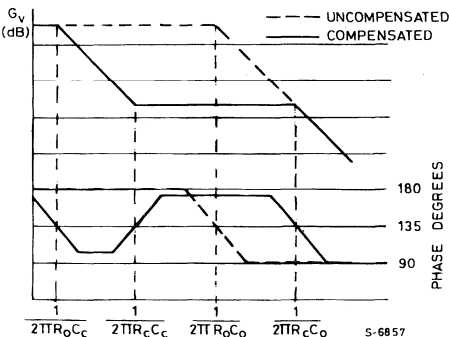


Figure A4 : Bode Plot Showing Gain and Phase of Compensated Error Amplifier.



CALCULATING THE STABILITY

For the stability calculation refer to the block diagram shown in figure A5.

The transfer functions of the various blocks are rewritten as follows.

The simplified transfer function of the compensated error amplifier is :

$$G_{EA} = g_m Z_c = \frac{1 + s R_C C_C}{s C_C} \quad (g_m = \frac{1}{2500})$$

The DC gain must be considered equal to :

$$A_o = g_m R_o$$

PWM block and output stage :

$$G_{PWM} = \frac{V_i}{V_{ct}}$$

LC FILTER :

$$G_{LC} = \frac{1 + s C \cdot ESR}{s^2 LC + s C ESR + 1}$$

where ESR is the equivalent series resistance of the output capacitor which introduces a zero at high frequencies, indispensable for system stability. Such a filter introduces two poles at the angular frequency.

$$\omega_o = \frac{1}{\sqrt{LC}}$$

Refer to the literature for a more detailed analysis.

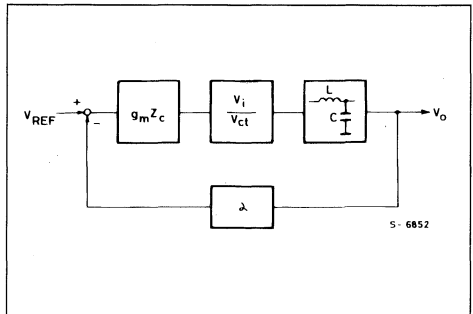
Feedback : consists of the block labelled α

$\alpha = 1$ when $V_o = V_{REF}$ (and therefore $V_o = 5.1V$)

and

$$\alpha = \frac{R_2}{R_1 + R_2} \quad \text{when } V_o > V_{REF}$$

Figure A5 : Block Diagram Used in Stability Calculation.



To analyse the stability we will use a Bode diagram. The values of L and C necessary to obtain the required regulator output performance, once the frequency is fixed, are calculated with the following formulae :

$$L = \frac{(V_i - V_o) V_o}{V_i f \Delta I_L}$$

$$C = \frac{(V_i - V_o) V_o}{8L f^2 \Delta V_o}$$

Since this filter introduces two poles at the angular frequency

$$\omega_o = \frac{1}{\sqrt{LC}}$$

we place the zero of the $R_C C_C$ network in the same place :

$$\omega_z = \frac{1}{R_C C_C}$$

Taking into account also the gain of the PWM block, the Bode plot of figure A6 is obtained.

The slope where the curve crosses the axis at 0dB is about 40dB/decade therefore the circuit is unstable.

Taking into account now the zero introduced by the equivalent series resistance (ESR) of the output capacitor, we have further condition for dimensioning the $R_C C_C$ network. Knowing the ESR (which is supplied by the manufacturer for the quality components) we can determine the value of R_C so that the axis is crossed at 0dB with a single slope. The zero introduced by the ESR is at the angular frequency :

$$\omega_{zESR} = \frac{1}{ESR \cdot C}$$

The overall Bode diagram is therefore as shown in figure A7.

Figure A6 : Bode Plot of System Taking Filter and Compensation Network into Account.

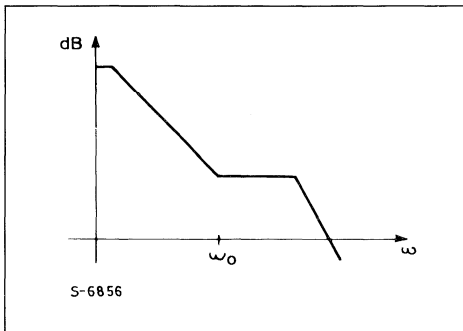
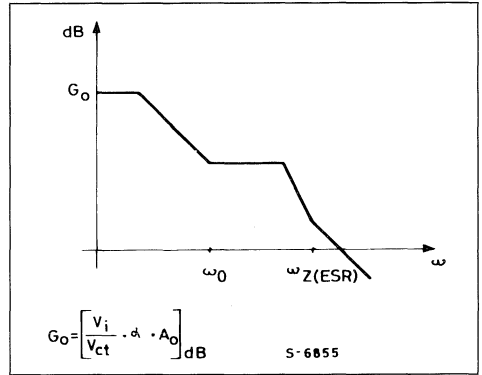


Figure A7 : Bode Plot of Complete System Taking into Consideration the Equivalent Series Resistance of the Output Capacitor.



DC GAIN AND LINE REGULATION

Indicating the open-loop gain of the error amplifier with A_o , the overall open-loop gain of the system is :

$$A_t = A_o \cdot \frac{V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}$$

When $V_o = V_{REF}$, the gain becomes :

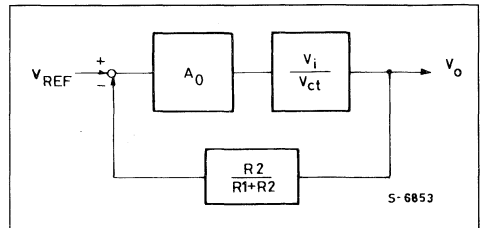
$$A_t = A_o \cdot \frac{V_i}{V_{ct}}$$

Considering the block diagram of figure A8 and calculating the output variation ΔV_o caused by a variation of V_i , from the literature we obtain :

$$\frac{\Delta V_o}{V_o} = \frac{\frac{\Delta V_i}{V_i}}{\frac{A_o V_i}{V_{ct}} \cdot \frac{R_2}{R_1 + R_2}}$$

This expression is of general validity. In our case the percentage variation of the reference must be added by vector addition.

Figure A8 : Block Diagram for Calculation of Line Regulation.



APPENDIX B

REDUCING INTERFERENCE

The main disadvantage of the switching technique is the generation of interference which can reach levels which cause malfunctions and interfere with other equipment.

For each application it is therefore necessary to study specific means to reduce this interference within the limits allowed by the appropriate standards.

Among the main sources of noise are the parasitic inductances and capacitances within the system which are charged and discharged fastly. Parasitic capacitances originate mainly between the device case and the heatsink, the windings of the inductor and the connection wires. Parasitic inductances are generally found distributed along the strips of the printed circuit board.

Fast switching of the power transistors tends to cause ringing and oscillations as a result of the parasitic elements. The use of a diode with a fast reverse recovery time (t_{rr}) contributes to a reduction in the noise flowing by the current peak generated when the diode is reverse biased.

Radiated interference is usually reduced by enclosing the regulator in a metal box.

To reduce conducted electromagnetic interference (or radio frequency interferences - RFI) to the levels

permitted a suitably dimensioned filter is added on the supply line. The best method, generally, to reduce conducted noise is to filter each output terminal of the regulator. The use of a fixed switching frequency allows the use of a filter with a relatively narrow bandwidth. For off-line switching regulators this filter is usually costly and bulky. In contrast, if the device is supplied from a 50/60 Hz transformer the RFI filter problem is greatly reduced.

Tests have been carried out at the laboratories of Roederstein to determine the dimensions of a mains supply filter which satisfies the VDE 0871/6.78, class B standard. The measurements (see figs. B1 and B2) refer to the application with the L296 supplied with a filtered secondary voltage of about 30V, with $V_o = 5.1V$ and $I_o = 4A$. The switching frequency is 100kHz.

Figure B1 shows the results obtained by introducing on the transformer primary a $0.01\mu F/250V \sim$ class X capacitor (type ERO F1772-310-2030). To reduce interference further below the limit set by the standards an additional inductive filter must be added on the primary of the transformer.

Figure B2 shows the curves obtained by introducing this inductive filter (type ERO F1753-210-124). Measurements have also been performed beyond 30MHz ; the maximum value measured is still well below the limit curve.

Figure B1 : EMI Measurements with a Capacitor Connected across the Primary Transformer with Screen Grounded (A)

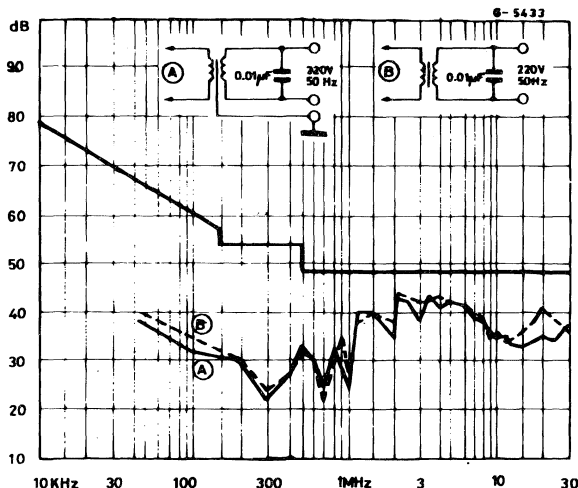
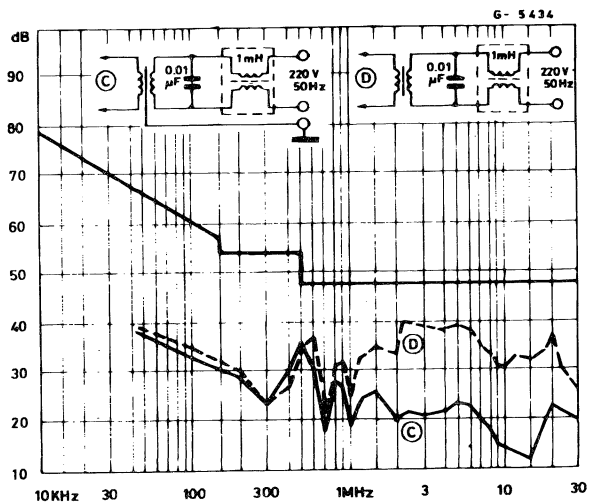
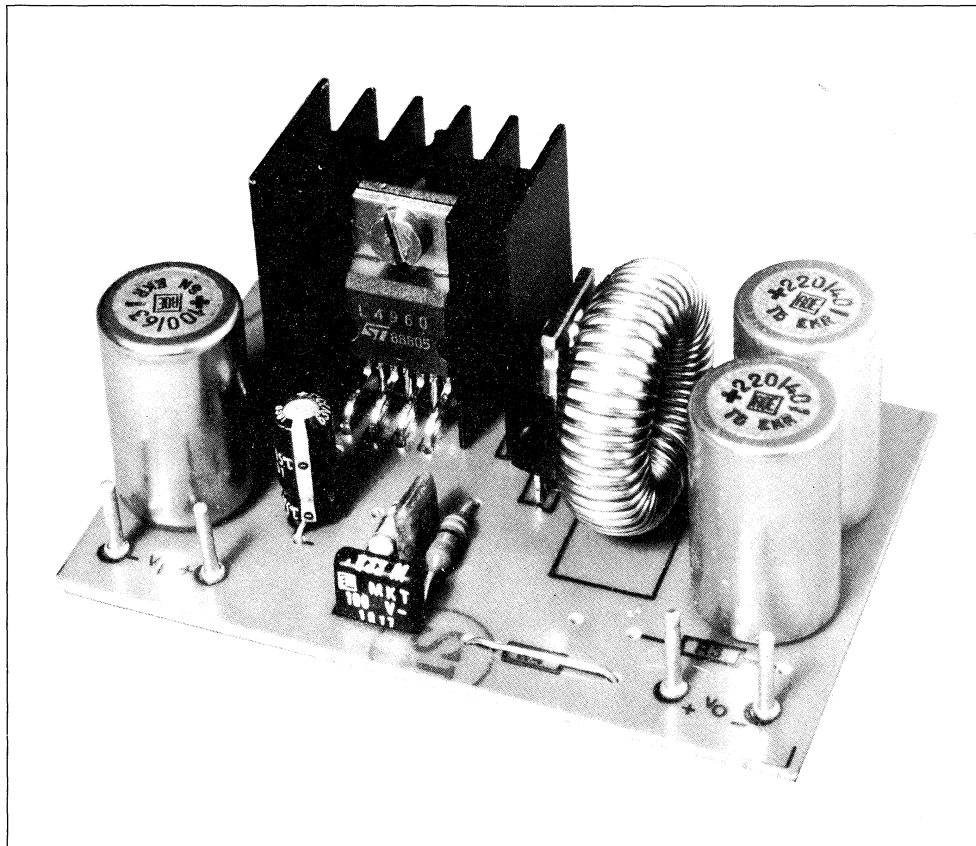


Figure B2 : EMI results with the addition of an inductive filter on the mains input.



DESIGNING MULTIPLE-OUTPUT POWER SUPPLIES WITH THE L296 AND L4960

Multiple output supplies can be realized simply and economically using the SGS THOMSON Microelectronics L296 and L4960 high power switching regulators. This note describes several practical circuits of this type.



Most of the switching regulators produced today have multiple outputs. The output voltages most frequently used - at least for powers up to 50W - are + 5V - 5V, + 12V and - 12V. In these supplies the 5 V output is normally the output which delivers the highest current and requires the highest precision. For the other voltages - particularly the negative outputs - less precision ($\pm 5\% \pm 7\%$) is usually sufficient. Often, however, for high current 12V outputs better stabilization and greater precision (typically

$\pm 4\%$ - the output tolerance of an L7800 series linear regulator) are required.

Multiple output supplies which satisfy these requirements can be realized using the SGS THOMSON L296 and L4960 high power switching regulator ICs. Several practical supply designs are described below to illustrate how these components are used to build compact and inexpensive multi-output supplies.

DUAL OUTPUT 15W SUPPLY

$V_{O1} = 5V/3A$, $V_{O2} = 12V/150mA$

A single L296 is used in this application to produce two outputs. The application circuit, figure 1, illustrates how the second output (12V) is obtained by adding a second winding to the output inductor. Energy is transferred to the secondary during the recirculation period when the internal power device of the L296 is OFF.

Since the 12V output is not separated from the 5V output fewer turns are necessary for the second

winding, therefore less copper is needed and load regulation is improved.

In applications of this type it is a good rule to ensure that the power drain on the auxiliary output is no more than 20-25% of the power delivered by the main output.

Table 1 shows the performance obtained with this dual output supply. This circuit operates at a switching frequency of 50KHz.

Figure 1 : Dual Output DC-DC Converter (5V/3A, 12V/150mA).

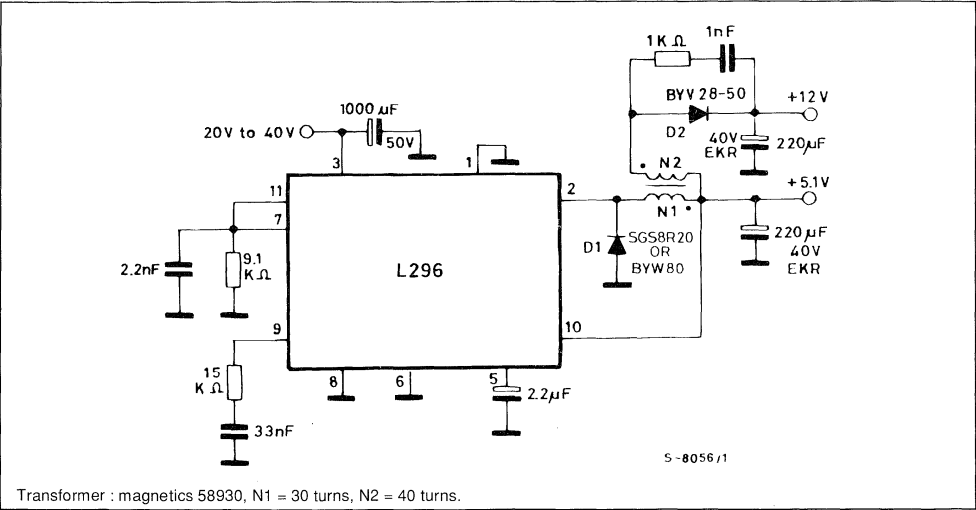


Table 1.

Parameter		V_{O1}	V_{O2}	Unit
Output Voltage $I_{O1} = 3A$	$V_i = 30V$ $I_{O2} = 150mA$	5.120	12.089	V
Output Ripple		70	40	mV
Line Regulation $I_{O1} = 3A$	$20V \leq V_i \leq 40V$ $I_{O2} = 150mA$	15	30	mV
Line Regulation $I_{O1} = 700mA$	$20V \leq V_i \leq 40V$ $I_{O2} = 100mA$	15	10	mV
Load Regulation $I_{O1} = 700mA \rightarrow 3A$	$V_i = 30V$ $I_{O2} = 150mA$	10	130	mV
Load Regulation $I_{O1} = 700mA$	$V_i = 30V$ $I_{O2} = 100 \rightarrow 150mA$	0	40	mV
Load Regulation $I_{O1} = 3A$	$V_i = 30V$ $I_{O2} = 100 \rightarrow 150mA$	0	40	mV
Efficiency	$V_i = 30V$ $V_{O1} = 5.120V$ $I_{O1} = 3A$ $V_{O2} = 12.089V$ $I_{O2} = 150mA$	75		%

DUAL OUTPUT 7.5W SUPPLY

$V_{O1} = 5V/1.5A$, $V_{O2} = 12V/100mA$

The same technique - adding a secondary winding - can also be used to produce an economical and simple dual output supply with the L4960, a device

containing the same control loop blocks as the L296 and a 2A output stage (fig. 2). Though this circuit costs very little the performance obtained (see table 2) is more than satisfactory. The switching frequency is 50kHz.

Figure 2 : Dual Output DC-DC Converter (5V/1.5A, 12V/100mA).

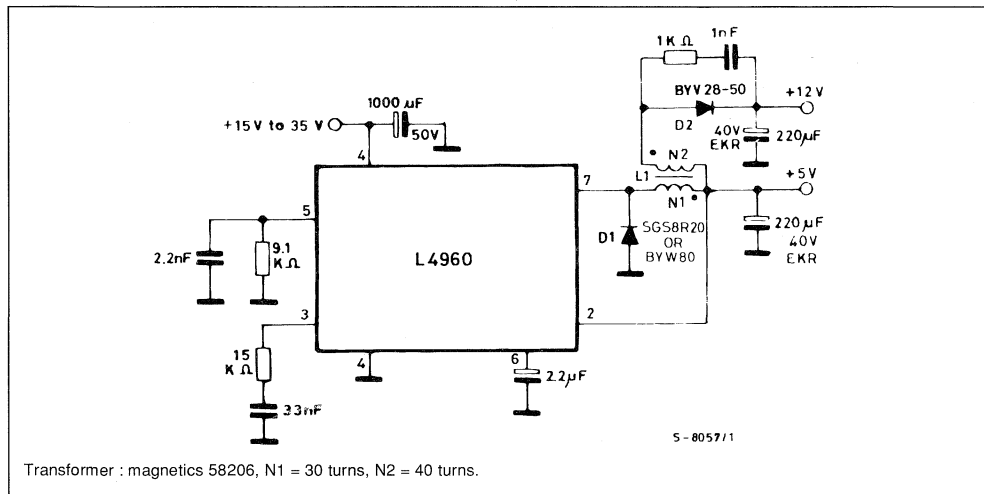


Table 2.

Parameter		V_{O1}	V_{O2}	Unit
Output Voltage	$V_i = 25V$ $I_{O1} = 1.5A$ $I_{O2} = 100mA$	5.050	12.010	V
Output Ripple		50	30	mV
Line Regulation	$15V \leq V_i \leq 35V$ $I_{O1} = 1.5A$ $I_{O2} = 100mA$	7	75	mV
Line Regulation	$15V \leq V_i \leq 35V$ $I_{O1} = 500mA$ $I_{O2} = 50mA$	7	60	mV
Load Regulation	$V_i = 25V$ $I_{O1} = 0.5A \rightarrow 1.5A$ $I_{O2} = 100mA$	3	100	mV
Load Regulation	$V_i = 25V$ $I_{O1} = 500mA$ $I_{O2} = 50mA \rightarrow 100mA$	0	55	mV
Load Regulation	$V_i = 25V$ $I_{O1} = 1.5A$ $I_{O2} = 50mA \rightarrow 100mA$	0	50	mV
Efficiency	$V_i = 25V$ $V_{O1} = 1.5V$ $V_{O2} = 100mA$	78		%

TRIPLE OUTPUT 15W SUPPLY

$V_{O1} = 5V/3A$, $V_{O2} = 12V/100mA$, $V_{O3} = -12V/100mA$

Figure 3 shows how to obtain two auxiliary outputs ($\pm 12V$) which are isolated from the 5V output. For this output power range an L296 is used.

To ensure good tracking of the 12V and -12V outputs the secondary outputs in this application should be bifilar wound.

This circuit operates at 50KHz and gives the performance indicated in table 3.

Figure 3 : Triple Output DC-DC Converter (5V/3A, 12V/100mA).

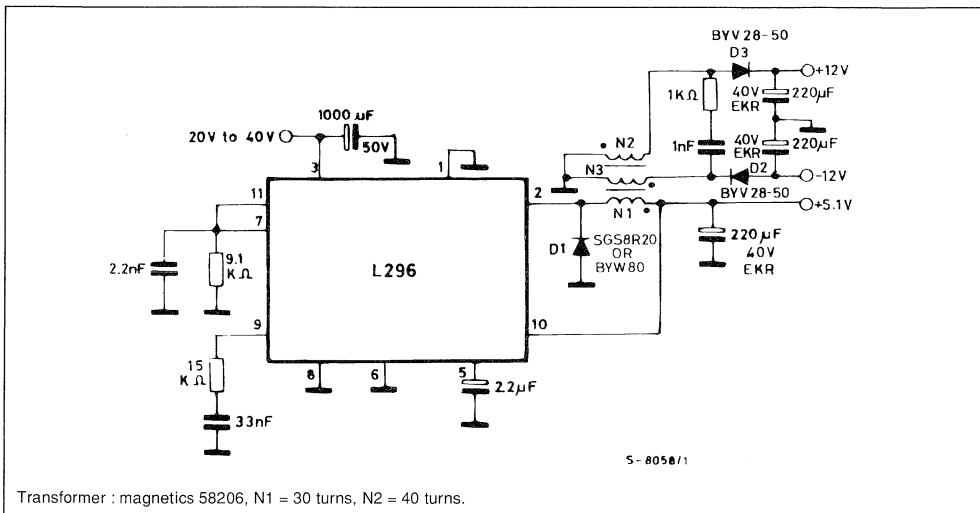


Table 3.

Parameter		V_{O1}	V_{O2}	V_{O3}	Unit
Output Voltage $I_{O1} = 3A$	$V_i = 30V$ $I_{O2} = I_{O3} = 100mA$	5.057	12.300	- 12.300	V
Output Ripple		80	30	30	mV
Line Regulation $I_{O1} = 700\text{ mA}$	$20V \leq V_i \leq 40V$ $I_{O2} = I_{O3} = 100mA$	15	60	60	mV
Line Regulation $I_{O1} = 3A$	$20V \leq V_i \leq 40V$ $I_{O2} = I_{O3} = 100mA$	18	100	100	mV
Load Regulation $I_{O1} = 0.7A \rightarrow 3A$	$V_i = 30V$ $I_{O2} = I_{O3} = 100mA$	4	150	150	mV
Load Regulation $I_{O1} = 3A$	$V_i = 30V$ $I_{O2} = 100mA$ $I_{O3} = 50 \rightarrow 100mA$	0	125	52	mV
Load Regulation $I_{O1} = 3A$ $I_{O2} = 50 \rightarrow 100mA$	$V_i = 30V$ $I_{O3} = 100mA$	0	50	120	mV
Efficiency		76			%

THE L296 AND L4960 HIGH POWER SWITCHING REGULATORS

The SGS THOMSON L296 is a monolithic stepdown switching regulator assembled in the 15-pin Multi-watt package. Operating with supply input voltages up to 46V it provides a regulated 4A output variable from 5.1V to 40V.

Internally the device is equipped with current limiter, soft start and reset (or power fail) functions, making it particularly suitable for supplying microprocessors and logic.

The precision of the L296's internal reference ($\pm 2\%$) eliminates the need for external dividers or trimming to obtain a 5V output.

The synchronization pin allows synchronous operation of several devices at the same frequency to avoid generating undesirable beat frequencies.

The L4960 is a similar device assembled in the 7-lead Heptawatt package. Like the L296 it has a maximum input voltage of 46V and it provides a regulated output voltage variable from 5V to 40V with a maximum load current of 2.5A. Current limiting, soft start and thermal protection functions are included.

The thermal protection circuit in both the L296 and L4960 has a hysteresis of 30°C to allow soft restarting after a fault condition.

THE STEP DOWN CONFIGURATION

Figure 5 shows the basic structure of a step down switching regulator. The transistor Q is used as a switch and the ON and OFF times are determined by the control circuit.

When Q is saturated current flows from the supply, V_i , to the load through the inductor L. Neglecting the saturation voltage of Q, $V_e \approx V_i$.

When Q is OFF, current continues to flow in the inductor L, in the same direction, forcing the diode into conduction immediately therefore V_e is negative. In these conditions the load current flows through L and D.

The average value of the current in the inductor is equal to the load current. In the inductor a triangular current ripple equal to ΔI_L is added to this average current.

During the time when Q is ON this ripple is :

$$\Delta I_L = \frac{(V_i - V_o) T_{ON}}{L}$$

and when Q is off it is :

$$\Delta I_L = \frac{V_o \cdot T_{OFF}}{L}$$

Equating these expression and assuming that the transistor and diode are ideal we obtain :

$$V_o = V_i \cdot \frac{T_{ON}}{T} \quad T_{ON} \text{ is the conduction time of the transistor}$$

T is the oscillator period

The absolute average current in the supply is therefore :

$$I_{IOC} = I_o \cdot \frac{T_{ON}}{T}$$

Once the working frequency and desired ripple current have been fixed the value of the inductor L is given by :

$$L = \frac{(V_i - V_o) V_o}{V_i f \Delta I_L}$$

and the value of the capacitor C required to give the desired output voltage ripple (ΔV) is :

$$C = \frac{(V_i - V_o) V_o}{8 L f^2 \Delta V}$$

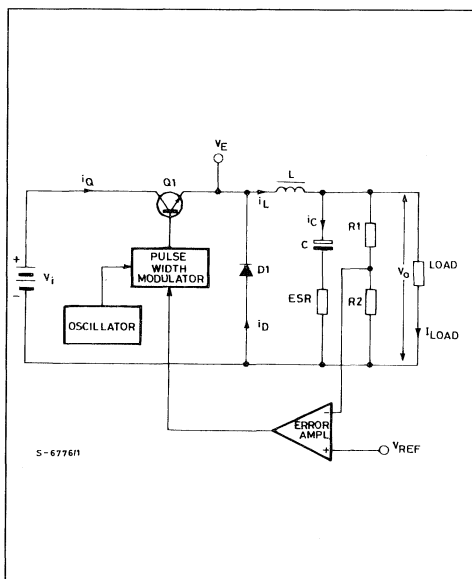
This capacitor must have a maximum ESR given by :

$$ESR_{MAX} = \frac{\Delta V_o}{\Delta I_L}$$

And, finally, the minimum load current, I_{OMIN} , must be :

$$I_{OMIN} = \frac{\Delta I_L}{2} = \frac{(V_i - V_o) V_o}{2 V_i f L}$$

Figure 5 : Basic STEP-DOWN Configuration.



30W DC-DC CONVERTER

Designing power supplies in the 30-40W range is becoming increasingly difficult because it is here that there is the greatest need to maintain performance levels and reduce costs. The application proposed here is very competitive because it exploits new ICs to reduce size, number of components and assembly costs.

This solution, the DC-DC converter, compares very favourable with off-line switching supplies in terms of cost. DC-DC converters can, in fact, be realized

even by designers with little experience and allows the convenience of working with low voltages. Off-line switching supplies are only preferable when the weight and size of the mains transformer in a DC-DC converter would be excessive.

In this circuit, figure 6 two devices are used, an L296 and an L4960. The L296 is used, to supply a 5V output with a current of 3A and the auxiliary -5V/100mA output and the L4960 is used to provide the 12V/1.5A output and the auxiliary -12V/100mA output.

Figure 6 : Multioutput DC-DC Converter with L296 and L4960 (5V / 3A, 12V / 1.5A, -12V/100mA, -5V/100mA).

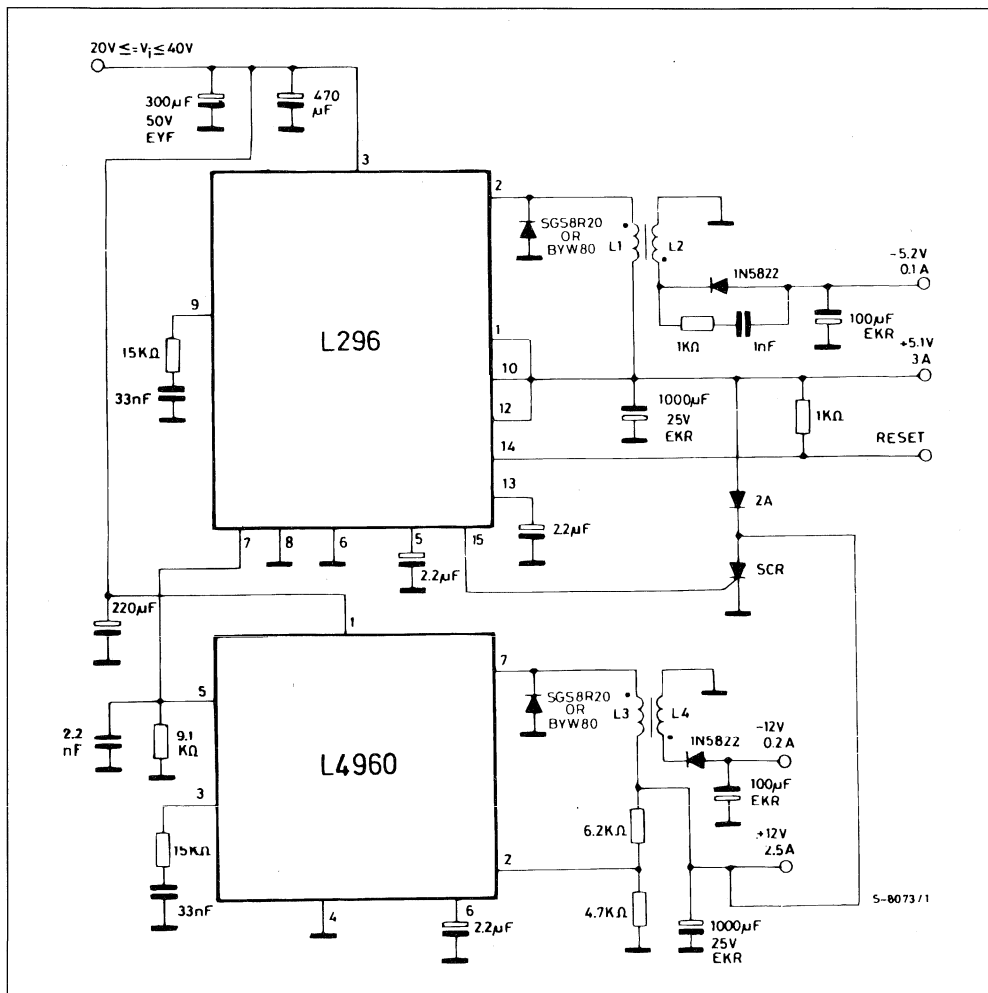


Table 5 shows the performance obtained with this power supply.

Table 5.

Parameter		V _{O1}	V _{O2}	V _{O3}	V _{O4}	Unit
Output Voltage	V _i = 30V I _{O1} = 3A I _{O2} = 100mA	5.080	- 5010	11.96	12.00	V
Output Ripple	I _{O3} = 1.5A I _{O4} = 100mA	50	30	50	40	mV
Line Regulation	20V ≤ V _i ≤ 40V I _{O1} = 1A I _{O3} = 0.5A	13	15	10	20	mV
Load Regulation	V _i = 30V I _{O1} = 1A to 3A	8	90			mV
	I _{O2} = 100mA I _{O3} = 0.5 to 1.5A			3	80	mV
Load Regulation	V _i = 30V I _{O1} = 3A	0	100			mV
	I _{O2} = 50 → 100mA I _{O3} = 1.5A			0	100	mV
Load Regulation	V _i = 30V I _{O1} = 1A	0	35			mV
	I _{O2} = 50 → 100mA I _{O3} = 0.5A			0	90	mV
Line Regulation	20 ≤ V _i ≤ 40V I _{O1} = 3A	15	45			mV
	I _{O2} = 100mA I _{O3} = 1.5A			15	40	mV

This application illustrates how two devices may be synchronized. Note also that the reset circuit is used in this case to monitor the output voltage (see figure 7).

If a power fail function is required in place of the reset function the figure 6 circuit should be modified as shown in figure 8.

Figure 7 : Reset Output Waveforms.

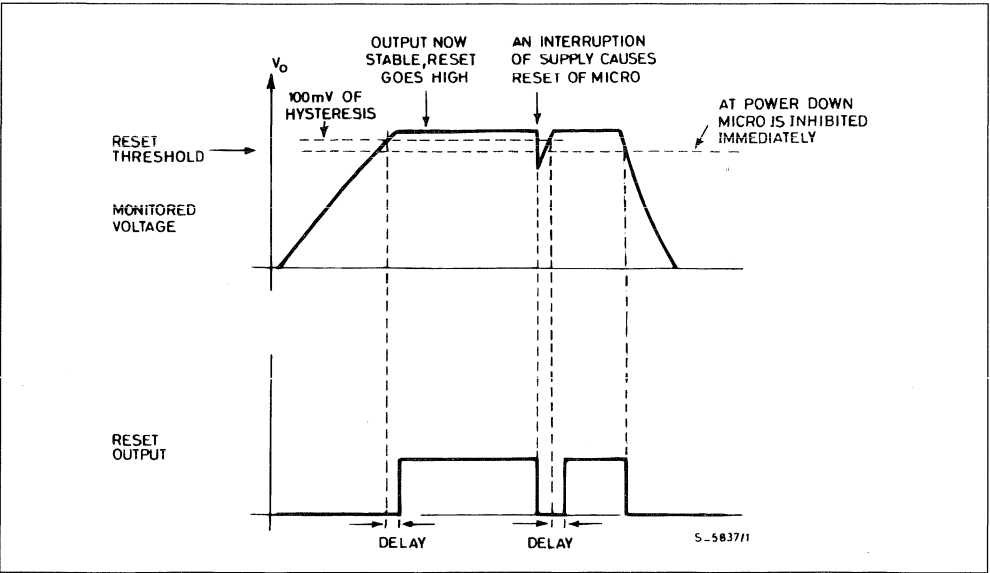
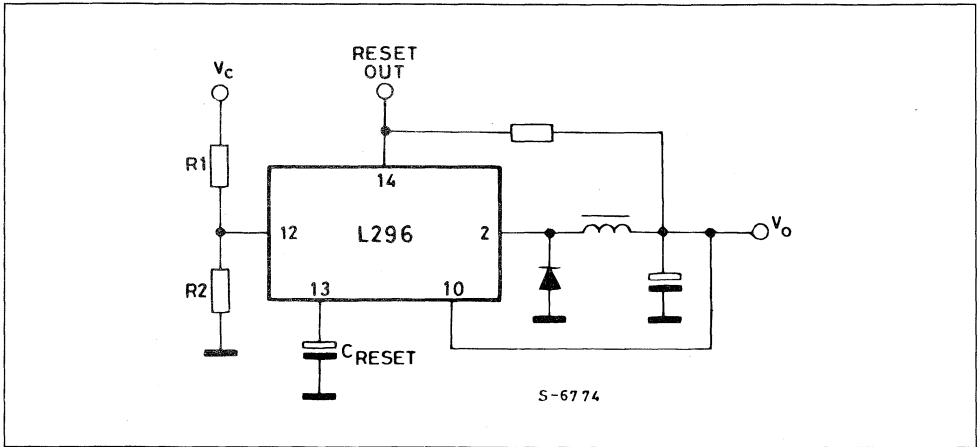


Figure 8.

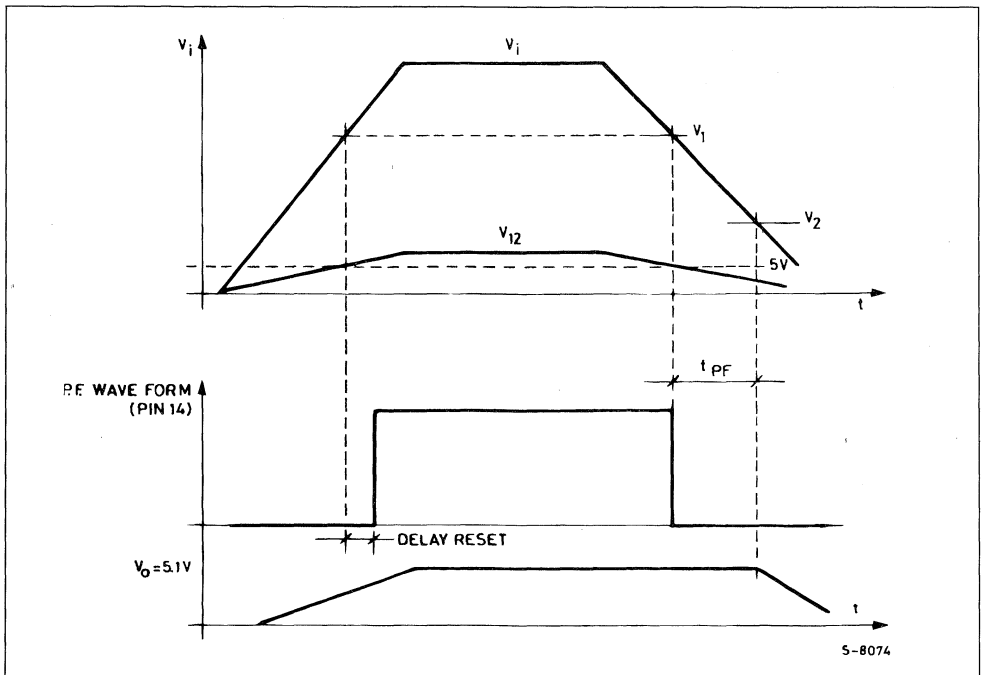


CALCULATING THE POWER FAIL TIME

The 'power fail time' is defined as the time from when the power fail output (pin 14) goes low to the time when the input voltage falls to the minimum level re-

quired to maintain the regulated output (see figure 9). From this definition we can evaluate the energy balance.

Figure 9.



The energy which the filter capacitor C supplies to the operating device while it discharges is :

$$E = 1/2 C (V_1^2 - V_2^2) \quad (1)$$

The load drains a power of $P_o = V_o I_o$. Taking into consideration the average efficiency η (derived with the input between V_1 and V_2), the power to be supplied at the input of the device is :

$$P_{o2} = \frac{P_o}{\eta} \quad (2)$$

Equating the expressions (1) and (2) gives :

$$1/2 C (V_1^2 - V_2^2) = \frac{P_o}{\eta} \cdot t_{PF}$$

where V_1 is the input voltage at which the voltage on pin 12 reaches 5V (through the divider R_1/R_2) ; V_2 is the maximum input voltage below which the device no longer regulates.

Rearranging this expression to obtain C :

$$C = \frac{2 P_o t_{PF}}{\eta (V_1^2 - V_2^2)}$$

EXAMPLE - Suppose that $V_o = 5V$, $I_o = 3A$, $T_{pf} = 10ms$ and $V_i = 35V$. Fixing $V_1 = 25V$ and $V_2 = 10V$ we obtain :

$$C = \frac{2 P_o t_{PF}}{\eta (V_1^2 - V_2^2)} = \frac{2 \times 15 \times 10 \cdot 10^{-3}}{0.75 (25^2 - 10^2)} = 760\mu F$$

We obtain choose a capacitor of 1000 μF .

CROWBAR

The L296 includes an internal crowbar function ; the only external component needed is an SCR. The intervention threshold of this block is fixed internally at 20% of the nominal value of the internal reference.

In the figure 6 circuit the SCR is triggered by an over-voltage on the 5V output (usually the most important output to monitor) and shortcircuits to ground the 5V output and, through the diode which connects the two outputs, the 12V output.

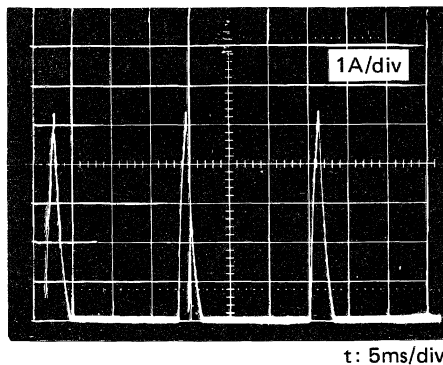
Since the internal current limiter in the device is designed to function as shown in figure 10 (that is, with pulsed output current) the SCR turns off in the gap between pulses and is re-activated again if, when the device restarts softly, the fault condition has not been eliminated. But if the fault no longer exists the SCR remains OFF and the output voltage returns to the normal value.

If the designer prefers the supply to remain off after the SCR has been activated the circuit can be modified as shown in figure 11. In this modification, when the SCR is triggered a very high current flows in the fuse, blowing it.

Since the filter capacitor can have a high value and be charged to high voltages the choice of SCR is important. The type used in this circuit - the TYP512 - is a plastic packaged SCR able to handle 12 Arms and 300A for 10ms. The maximum forward and reverse voltages are about 50V.

If the crowbar circuit is not used it is advisable to connect pin 1 to ground or pin 10.

Figure 10 : Load Current in Short Circuit Conditions ($V_i = 40V$, $L = 300\mu H$, $f = 100KHz$).



Current at Pin 2 when the Output is Short Circuited.

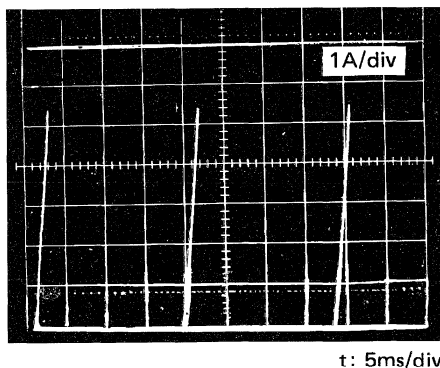
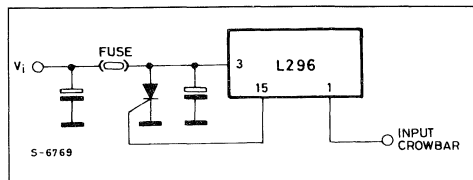


Figure 11.



OPTIMUM BASE DRIVE AND PROTECTION OF SWITCHING TRANSISTORS USING THE UAA4002

by Philippe MAIGE

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1. DECENTRALIZED PROTECTION OF POWER TRANSISTORS

It is not usually a simple matter to implement an efficient base control circuit combining fast switching, minimum losses and total safety of the switching component in switching systems involving high currents and voltages. Considerable care must be exercised in designing such systems, and the time involved on this stage is often considerable. The utilization of decentralized control and protection integrated circuits, now makes it easier to develop transistorized switching modules which are self-protected and galvanically isolated from their controlling circuits.

1.1. POWER TRANSISTORS PROTECTION

Power transistors are rugged and reliable devices, able to withstand limited overloads. The functional security of transistorized equipment therefore depends on the means used to ensure that the component's maximum ratings are not exceeded under any circumstances.

Key parameters of power transistors

The main parameters to be monitored in the case of a power transistor operating in switching mode are as follows :

In the cut-off state :

- The maximum collector-emitter voltage,
- The reverse bias voltage at the emitter-base junction (transistor operating with V_{CEV}).

In the conducting state :

- The collector current,
- The saturation state (sufficient base current for the transistor to remain saturated whatever the collector current).

During switching to the conducting state :

- Conformity with the forward bias safe operating area (FBSOA).

During switching to the cut-off state :

- Conformity with the reverse bias safe operating area (RBSOA).

These parameters may be monitored in various ways.

1.2. PASSIVE PROTECTION

Passive protection consists in the use of networks of passive components (resistors, capacitors, inductors, ...) to absorb low energy disturbances of limited duration.

This category includes :

- Input filters in switching mode power supplies protecting against high amplitude short duration overvoltages (lightening strikes, etc...)
- Peak limiting circuits which can eliminate switching overvoltages due to stray inductance.
- Switching aid circuits which may, in some circumstances, be regarded as protection devices. This applies, for example, to converter circuits in which the transistors' V_{CEV} withstand properties are exploited. The use of a switching aid network provides for distorting the switching cycle so as to maintain it within the authorised limits.

1.3. ACTIVE PROTECTION

Active protection, where the transistor is actively involved in its own protection, differs fundamentally from passive protection. When one of its vital parameters is out of limits, this is detected and indicated to a "security processor". This processor then decides, if there is a real hazard, to switch the transistor affected to the state in which it is least vulnerable (the cut-off state).

1.4. DECENTRALIZED PROTECTION

It is not always easy to use a true security processor, especially in circuits requiring the monitoring of parameters which are galvanically isolated from one another (bridged circuits, for example). The decentralization of protection to the level of each individual transistor of this circuit has therefore been envisaged. The vital parameters of each transistor are thus monitored in situ. If limits are exceeded, there is no indication transmitted to a centralized security processor, the information being instead processed locally by a decentralized processor which initiates immediate corrective action at the level of the transistor affected and independently of the remainder of the circuit.

The UAA4002 integrated circuit implements the "optimum base circuit control + total protection" functions and embodies a new concept : active and decentralized protection of power transistors.

Using this circuit reduces overall design time and results in transistorized equipment with enhanced performance and functional security, irrespective of the peculiarities of their environment.

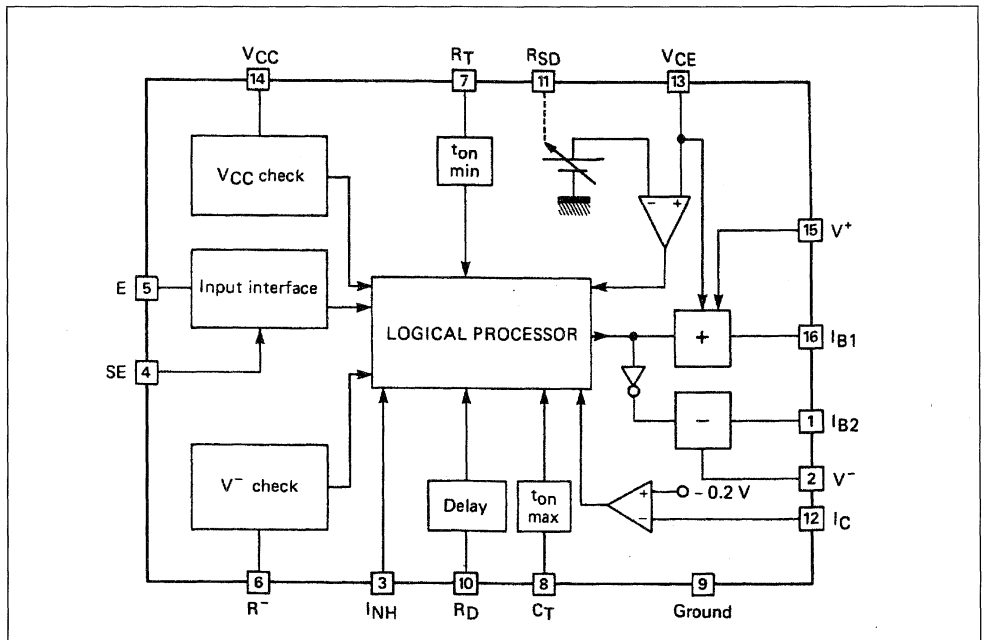
2. FUNCTIONAL DESCRIPTION

2.1. THE UAA4002, AN "INTELLIGENT" INTERFACE

The UAA4002 integrated circuit is housed in a 16-pin plastic case. Its main design features will now be described :

- It receives conduction information in the form of logic signals and converts these to a base current applied to the power transistor. This base current is self-regulated so as to maintain the switch in a quasi-saturated state. This significantly reduces the storage time of the switching transistor when turning off. The maximum current delivered by the UAA4002 is 0.5A. The circuit is designed for easy extension of the available base current through the addition of one or more external transistors.
- The UAA4002 applies to the base of switching transistor a high negative current, of as much as 3A. This ensures efficient cutting off, with a collector current fall time which is extremely short, reducing switching losses. Like the positive base current, the negative base current may be readily increased using external transistors.
- The UAA4002 uses a built-in high-speed logic processor to protect the switching transistor. This processor monitors the collector-emitter saturation voltage and the collector current of the transistor during conduction. It also monitors the positive and negative supply voltages of the integrated circuit, and the chip temperature. If further applies minimum and maximum conduction times as programmed by the user. Finally, by storing any fault condition until the end of the conduction period, it eliminates any "reswitching" phenomenon.
- Some functions may be disabled, providing considerable flexibility of use.

Figure 1 : UAA4002 Block Schematic.

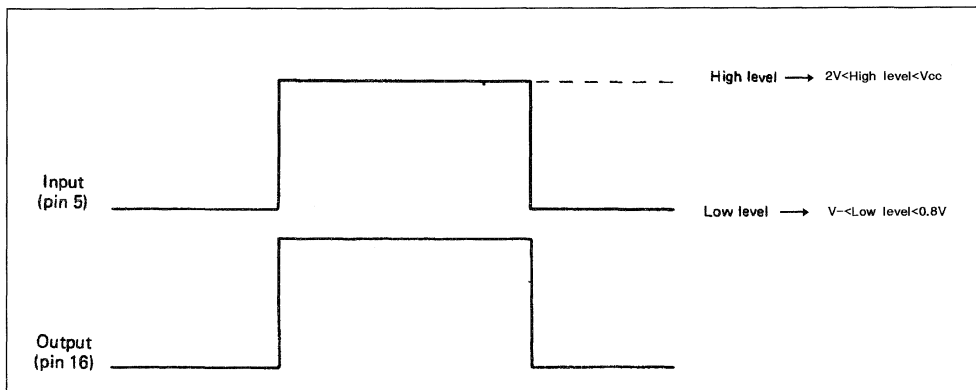


2.2. INPUT INTERFACE

The input interface provides the necessary adaptation between signals from regulation or control devices and the built-in logic processor of the integrated circuit.

There are two control modes, according to the logic level at select input SE (pin 4) : level mode and pulse mode.

Figure 2a : UAA4002 Level Control Mode.



In view of the signal propagation times within the circuit, the output signal is delayed by approximately 300ns relative to the input signal.

Pulse mode

This mode is used when the control circuit must be galvanically isolated. A practical example of this kind

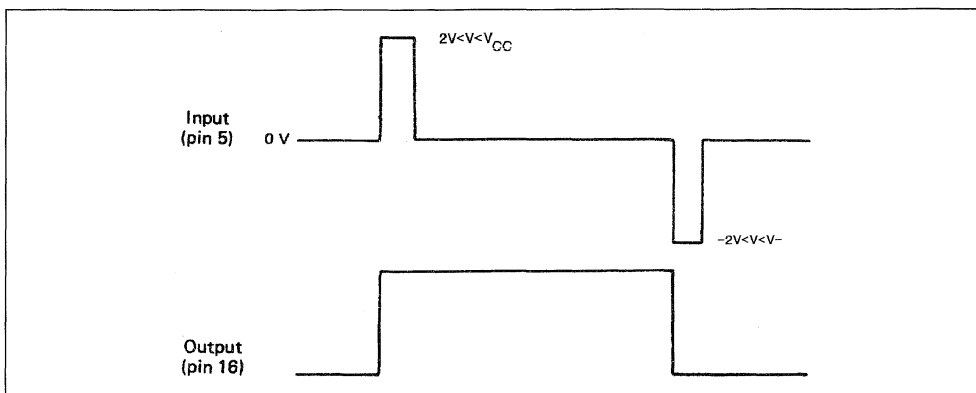
Level mode

This mode is selected by applying a "high" logic level to input SE. To achieve this, this input may be left "floating" or connected to the positive supply voltage V_{CC} through a resistor with a value of at least $4.7k\Omega$. Input E of the circuit (pin 5) is TTL- and CMOS-compatible. It is active at logic "1".

of situation will be described in the next section.

The UAA4002 is controlled by "alternate" pulses by applying a "low" logical level to input SE (pin 4), by connecting it directly to the ground (pin 9). The control signals applied to input E (pin 5) must have an amplitude of at least + 2V and must also be below the supply voltages V and V_{CC} .

Figure 2b : UAA4002 Pulse Control Mode.

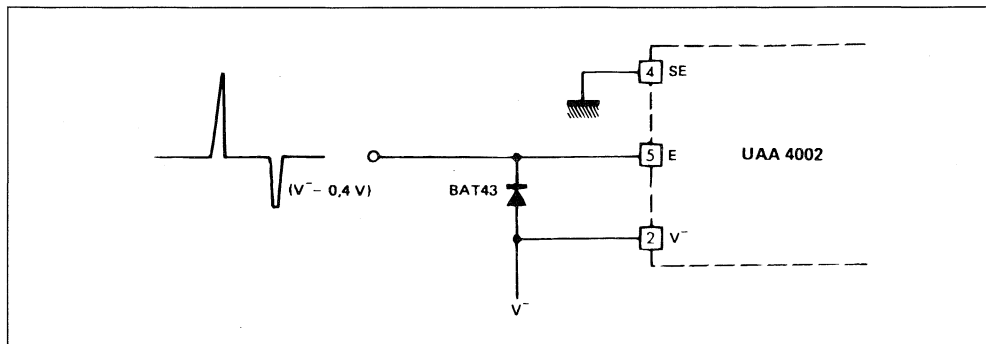


Specifically, this means that the negative supply voltage V^- must have an absolute value above 2.5V for this type of operation.

If, by accident or as the result of an error in using the circuit, the voltage V^- should be less than 2V (absolute value), the negative blocking pulses are ignored, resulting in continuous conduction. This is a particularly dangerous situation, which may be avoided by monitoring the negative supply voltage as described in section 2.4.

Negative pulses with an amplitude exceeding V^- are "clamped" by the integrated circuit to the voltage $V^- - V_D$, where V_D represents the threshold voltage of a diode. If the pulses have a high energy value content, there results a current in the substrate of the integrated circuit which disturbs its operation. To avoid this it is only necessary to "clamp" the negative pulses externally, using a diode with a low threshold. In all cases, a sufficiently high value for voltage V^- (-4 to -5V) is nevertheless preferable.

Figure 3 : Limitation of Negative Pulse Amplitude by Low Threshold Diode.



Pulse duration : to be recognized, the control pulses must have a duration of at least 100ns.

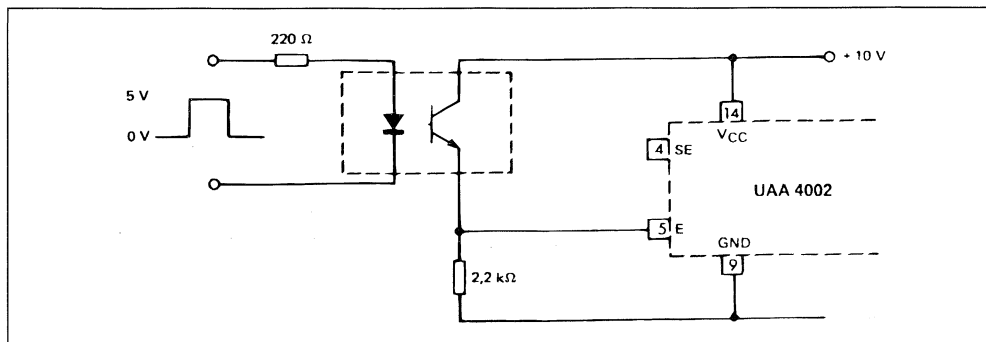
As in level mode, the propagation time of the signals within the circuit introduces a delay of approximately 300ns between the UAA4002 output signals and the corresponding control pulses.

Typical control circuits

Galvanic isolation between the control circuit which generates the conduction pulses and the UAA4002 is often required.

One possibility is to use an optocoupler. Figure 4 shows a typical circuit using this type of component.

Figure 4 : Optocoupler-isolated UAA4002 Control Input.



in view of the dynamic characteristics of optocouplers, this type of control circuit can be used only at relatively low frequencies (not more than a few KHz). For higher frequencies, particular care must be exercised in selecting the optocoupler, and it must be used optimally.

Another possibility, which is highly reliable and very economic, is to use a pulse transformer wound on a ferrite core.

Rather than transmitting the conduction pulse in its entirety, it is beneficial to use saturation of the magnetic circuit to implement a differentiating transformer. This reduces the size of the magnetic component, as a small ferrite core with only a few turns is quite sufficient. The UAA4002 is naturally programmed to accept alternate pulses in this case.

Figure 5 : Transformer-isolated UAA4002 Control Input.

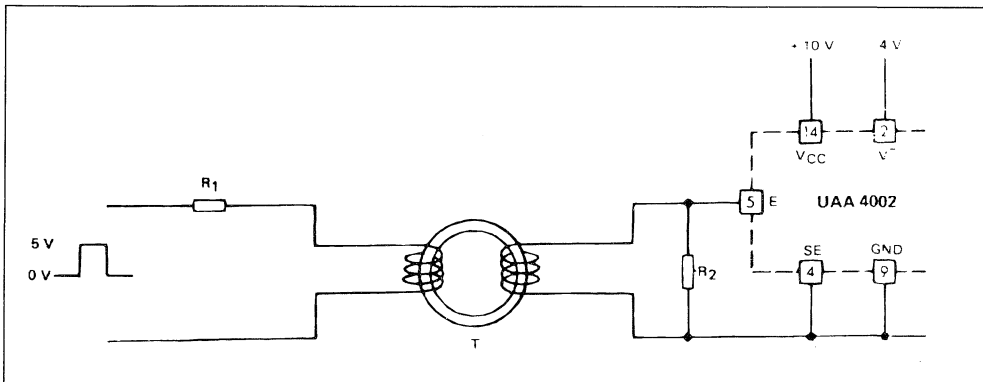


Figure 6 shows the results achieved with this circuit, using an FT 10 ferrite core (material code T6A) manufactured by LCC. The primary and secondary windings each comprise eight turns. The current limiting resistor R1 has a value of 270Ω and resistor R2 has a value of $1\Omega k$. The UAA4002 is associated with a BUX 48 high-speed switching transistor. The negative supply voltage is $-4V$.

The top trace shows the control signal applied to the primary winding of the transformer through resistor R1. The bottom trace is the signal obtained across the secondary winding and applied to input E of the UAA4002. The centre trace is the collector current of the transistor.

Figure 6 : UAA4002 Control Input Isolated by LCC FT 10 CORE.

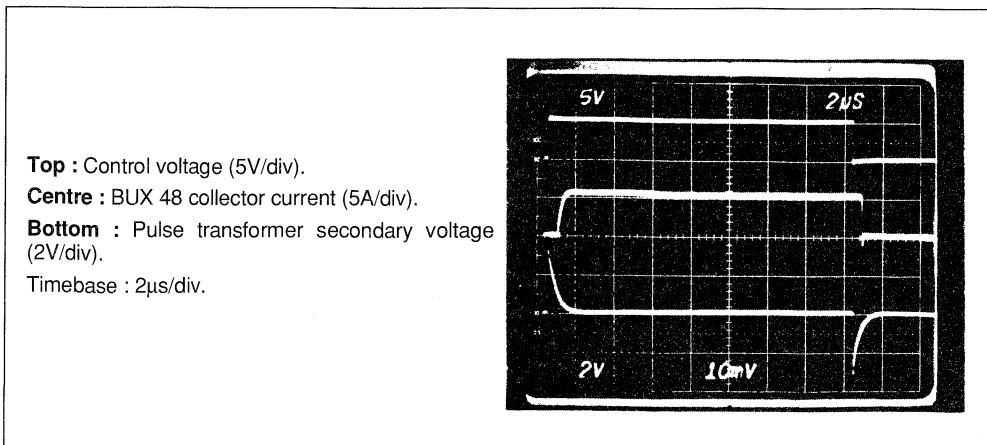
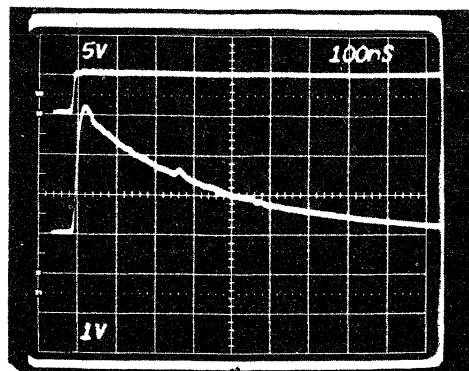


Figure 7.

Top : Control voltage (5V/div).

Bottom : UAA4002 input E voltage (1V/div).

Timebase : 100ns/div.



Note : As the pulses are not of rectangular waveform, the effective pulse width is that for which the triggering level ($\pm 2V$) is crossed, and not the total pulse width. For example, the oscillogram of figure 7 shows that the effective width of the pulses produced by the circuit described above is 150ns. An equivalent result could be obtained with less turns, but using a core of larger cross-section (LCC type FT 16, for example).

2.3. TIME CONSTANTS

Minimum conduction time $t_{on\ min}$

To enable the capacitor of the switching aid network associated with the power transistor to discharge completely, the logic processor ensures that the integrated circuit output pulse has a minimum duration $t_{on\ min}$. To be effective, this must be at least four times the time constant of the RCD network.

The value of $t_{on\ min}$ is programmed by a resistor R_T external to the circuit, connecting pin 7 to ground. The relationship between $t_{on\ min}$ and the value of resistor R_T is given by the equation :

$$t_{on\ min} (\mu s) = 0.06 \times R_T (k\Omega)$$

The usable range of values for $t_{on\ min}$ is between 1 and 12 μs .

Resistor R_T has a key role in the operation of the UAA4002 integrated circuit. It sets the value of a bias current internal to the circuit :

$$I (mA) = \frac{5}{R_T (k\Omega)}$$

For this reason, the values of certain other components depend on the value of this resistor which must, in practice, be determined first when computing the values of components around the UAA4002.

$t_{on\ min}$ embodies a priority security function : no other security function can stop the conduction during $t_{on\ min}$.

The $t_{on\ min}$ function cannot be disabled.

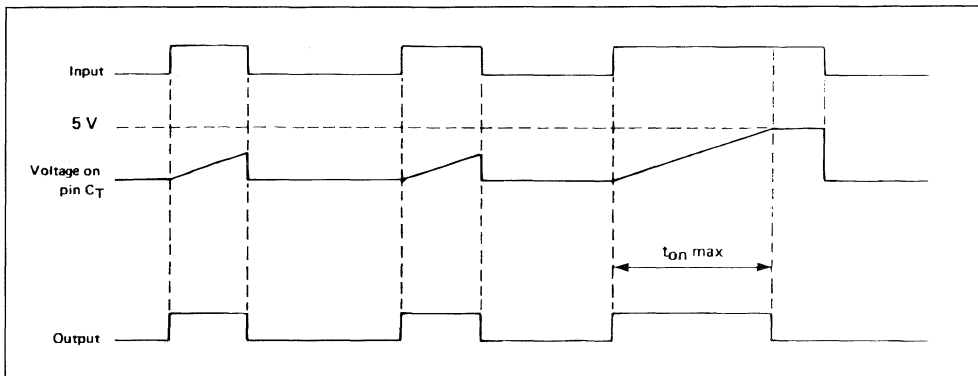
Maximum condition time $t_{on\ max}$

A maximum conduction time may be programmed by connecting a capacitor C_T between pin 8 and ground.

At the start of each conduction period the capacitor C_T is loaded by a constant current $I/2$, where I is the current through resistor R_T ($I = 5/R_T$). When the voltage across C_T reaches 5V the conduction is stopped. The value of $t_{on\ max}$ is thus given by the equation :

$$t_{on\ max} (\mu s) = 2 \times R_T (k\Omega) \times C_T (nF)$$

Capacitor C_T is discharged rapidly at the end of each conduction period.

Figure 8 : $t_{on\ max}$ Principle.

$t_{on\ max}$ embodies an important security function, being used, for example, to limit the power transmitted by a chopper circuit or to prevent accidental interruption of transmission resulting in continuous conduction in pulse control mode.

Disabling the $t_{on\ max}$ function

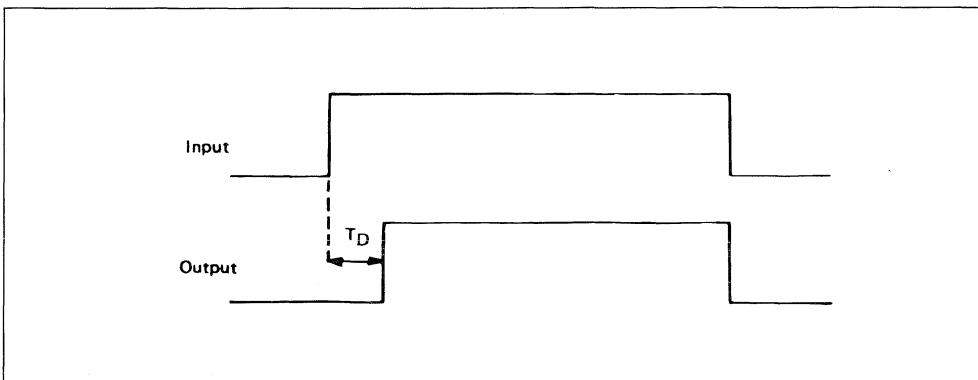
If the $t_{on\ max}$ function is not to be used, it is only

necessary to replace capacitor C_T with a short-circuit.

Time-delay function

A constant time-delay T_D may be implemented between the rising edge of the control pulse and the beginning of the conduction pulse at the circuit output.

Figure 9 : Time Delay Function.



The value of T_D may be adjusted between 1 and 20 μs using resistor R_D connected between pin 10 and ground. The value of T_D is given by the equation :

$$T_D (\mu\text{s}) = 0.05 \times R_D (\text{k}\Omega)$$

This function may be used to avoid the risk of simultaneous conduction in applications where a number of components are switched sequentially.

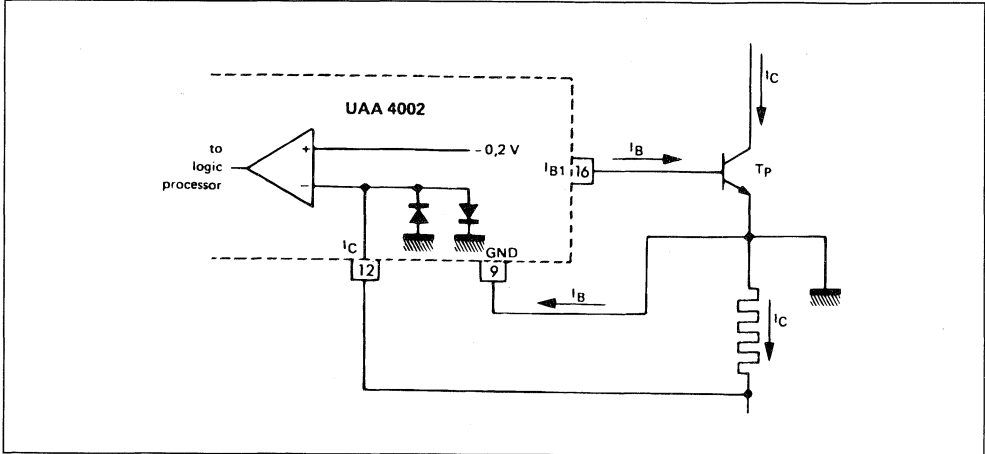
Disabling the function

If the time-delay function is not to be used, pin 10 is connected directly to supply voltage V_{CC} .

2.4. PROTECTION FUNCTIONS

Power transistor collector current limiting

The collector current of the power transistor is measured by means of a shunt connected in the negative return of the power supply. As a result, the current measured is the actual collector current rather than the emitter current, since the base current of the switching transistor does not flow through the shunt.

Figure 10 : Switching Transistor Collector Current Measurement.

A voltage below 0.2V on input I_C causes a comparator to change state. This information is transmitted to the logic unit, which blocks the output pulses from the circuit until the next positive transition of the input signal. If the voltage across the measuring shunt exceeds 0.2V for the required limiting current value, a voltage divider bridge may be used. Figure 11 shows a limiting device with the collector current limited to 8A, using a 0.12Ω shunt.

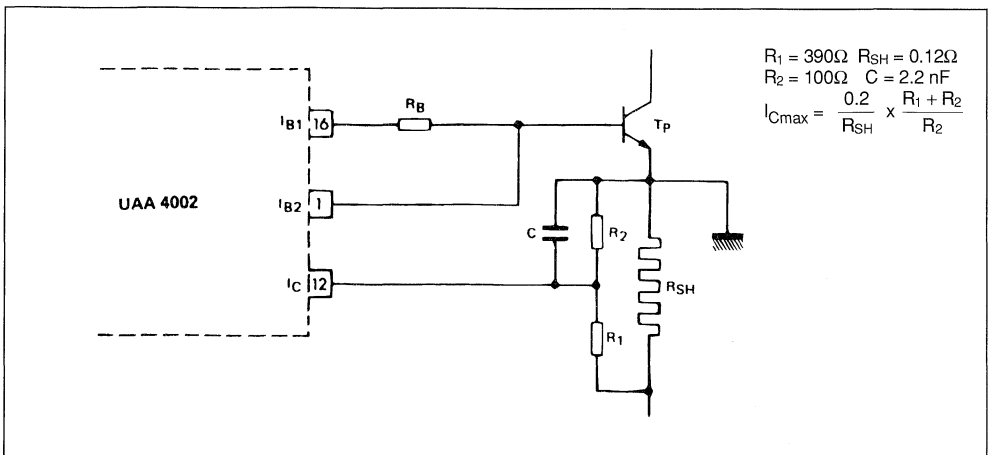
The shunt may be a wire-wound resistor, preferably non-inductive. Capacitor C across resistor R_2 filters the noise which is always present in a measuring shunt. This filter function may also be employed to

ignore transient exceeding of the limiting current value, where this may be regarded as non-hazardous to the switching transistor.

When the switched currents are high (more than a few dozen amperes), it may be difficult or even impossible to use a shunt. There is then the two-fold problem if requiring a very low resistance in combination with a high power dissipation ratings. In such cases, a current transformer may be used.

Disabling the function

If input I_C (pin 12) is not used, it must be connected directly to ground (pin 9).

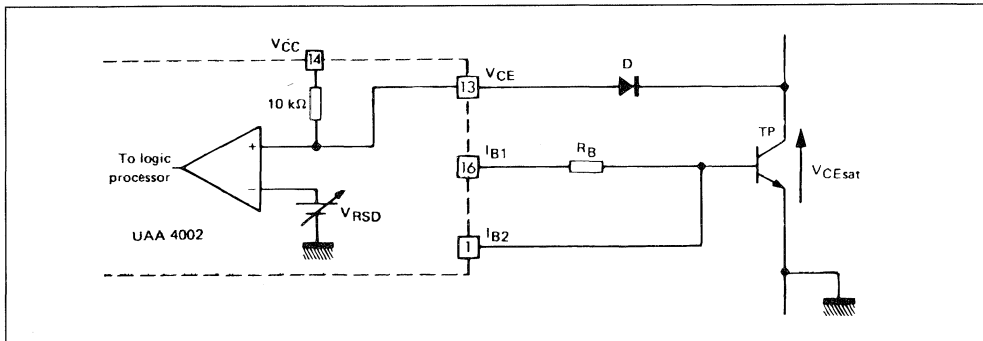
Figure 11 : Limitation of Collector Current to 8A.

Protection against desaturation of the power transistor

The switching transistor collector-emitter voltage is measured by means of a diode having its anode connected to input V_{CE} of the UAA4002 (pin 13) and its cathode connected to the collector of the transistor. During the conduction phase, this diode con-

ducts and the voltage on input V_{CE} is (ignoring the diode threshold) the same as the transistor collector-emitter voltage. When the transistor is cut off, the diode is also cut off and the voltage on input V_{CE} is the same as the positive supply voltage V_{CC} to the integrated circuit.

Figure 12 : V_{CEsat} Voltage Monitoring.



Diode D must be a high-speed diode able to withstand the transistor collector-emitter voltage when the transistor is cut off.

During the conduction phase, a comparator monitors the voltage on pin V_{CE} . If this becomes higher than the voltage programmed on pin R_{SD} (V_{RSD}), it advises the logic processor of this. The processor responds by blocking the control input until the next conduction cycle.

In this way, the power transistor is protected against any possibility of desaturation due, for example, to an insufficiently high base current or to a collector current overload.

The detection threshold V_{RSD} is set by the value of the resistor connected between pin R_{SD} (pin 11) and ground resistor R_{SD} carries a current $2I$, where I is the current through resistor R_T .

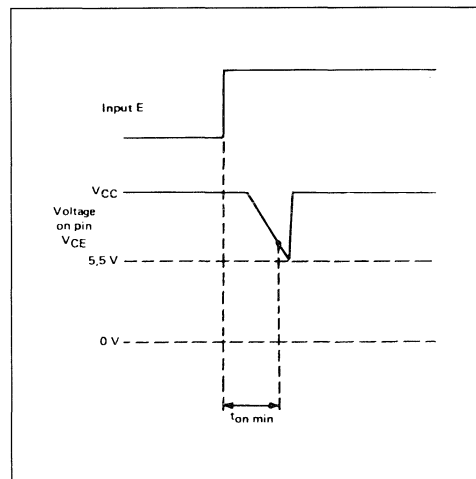
Thus the voltage (in Volts) across resistor R_{SD} is given by the equation :

$$V_{RSD} = 2 \times I \times R_{SD} = 10 \times R_{SD}/R_T$$

The range of adjustment for voltage V_{RSD} is between 1 and 5.5V. If pin R_{SD} is not connected, the voltage on it is internally limited to 5.5V.

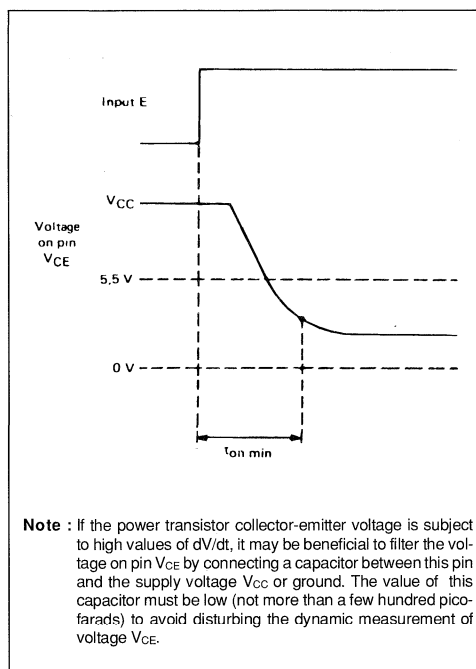
To enable the switching transistor collector-emitter voltage to fall when conduction begins, the function protecting against desaturation is disabled during $t_{on min}$. If this were not the case, there would be a systematic fault indication since the fault condition is always present at the start of each conduction cycle. This also means that the time $t_{on min}$ must permit the collector-emitter voltage to fall : after $t_{on min}$,

Figure 13a : $t_{on min}$ is insufficient : after $t_{on min}$ the voltage on pin V_{CE} is above 5.5V and the conduction is stopped.



the collector-emitter voltage must be less than the desaturation detection threshold. Thus, when high-voltage transistors are used, it may be necessary for this reason to set a value for $t_{on min}$ which is significantly greater than that set by the time constant of the RCD network.

Figure 13b : $t_{on\ min}$ is insufficient for the collector emitter voltage to fall.



Disabling the function

This protection function is disabled by connecting pin R_{SD} direct to potential V .

Supply voltage monitoring

A comparator internal to the circuit ensures that there is no output signal if the positive supply voltage V_{CC} is less than 7V. This threshold is not adjustable.

It is also possible to disable the output pulses from this circuit if the negative supply voltage V^- is insufficient, so as to guarantee switching of the power transistor.

The threshold is adjusted by means of an external resistor R^- connecting pin R^- (pin 6) to the negative supply voltage V^- . The principle for determining the threshold is similar to that for determining threshold V_{RSD} .

A current of $2 \times I$ ($2 \times 5/R_T$) is injected into resistor R^- . The voltage at pin R^- is given by the equation :

$$V_R = R^- \frac{10}{R_T} \times I - V^-$$

This voltage is applied to an internal comparator, the threshold for which is set at 5V. The change of state occurs when :

$$V_R = 5V = 10 \times \frac{R^-}{R_T} - I V^-$$

The limiting value of V^- as a function of the resistance R^- is given by the equation :

$$I V^- I_{min} = 10 \times \frac{R^-}{R_T} - 5$$

The value of resistor R^- corresponding to voltage V_{min} is given by the equation :

$$R^- = \frac{R_T}{2} \left(1 + \frac{|V^-|_{min}}{5} \right)$$

Example : $R_T = 68\ k\Omega$ ($t_{on\ min} = 4\ \mu s$)

$$I V^- I_{min} = 3.25V \leftrightarrow R^- = 56\ k\Omega$$

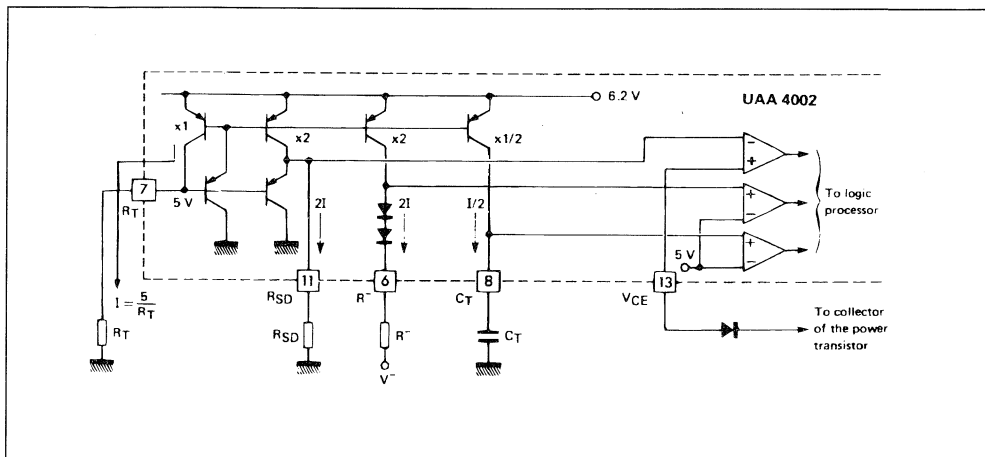
In addition to ensuring correct switching of the power transistor, monitoring of the negative voltage eliminates the risk of continuous conduction discussed in section 2.2., resulting from failure to act on negative blocking pulses in pulse mode.

Disabling supply voltage monitoring

Monitoring of the positive supply voltage V_{CC} may not be disabled.

Monitoring of the negative supply voltage V^- is optional. If not to be used, pin R^- may be connected to ground or to the V^- rail.

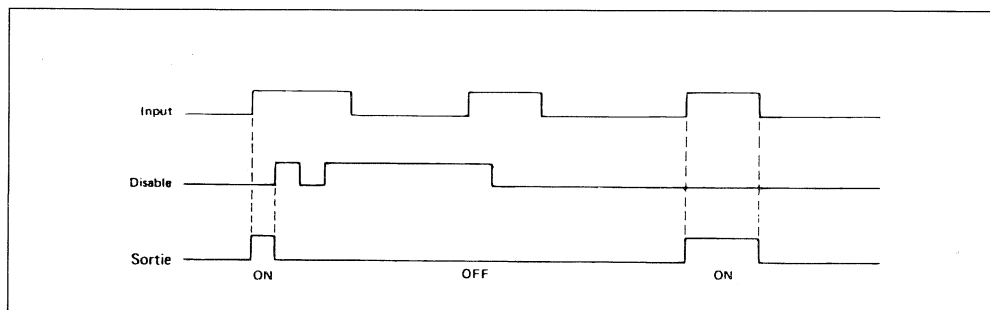
Figure 14 shows that part of the circuit which programs the thresholds for protection against desaturation (V_{SD}), negative supply monitoring (V_R) and time-delay (T_D).

Figure 14 : Programming of V_{SD} , V_R and T_D .**Disable function**

It is possible to disable or shorten conduction in the power transistor by applying a "high" logic level to the disable input (pin 3). This input is CMOS and TTL-compatible. An RS bistable internal to the circuit stores any disable which originates during con-

duction, until the next conduction pulse. This input can therefore be controlled by a pulsed signal (minimum duration 100ns).

If not used, the disable input must be connected directly to ground.

Figure 15 : Disable Function.**Thermal protection**

The UAA4002 is protected against excessive overheating by a thermal cut-out which automatically cuts off the output pulses if the chip temperature ex-

ceeds 150°C. The interruption is stored for a complete conduction period, but the output pulses reappear as soon as the chip temperature falls below the limiting temperature value.

2.5. - UAA4002 OUTPUT STAGE

Introduction

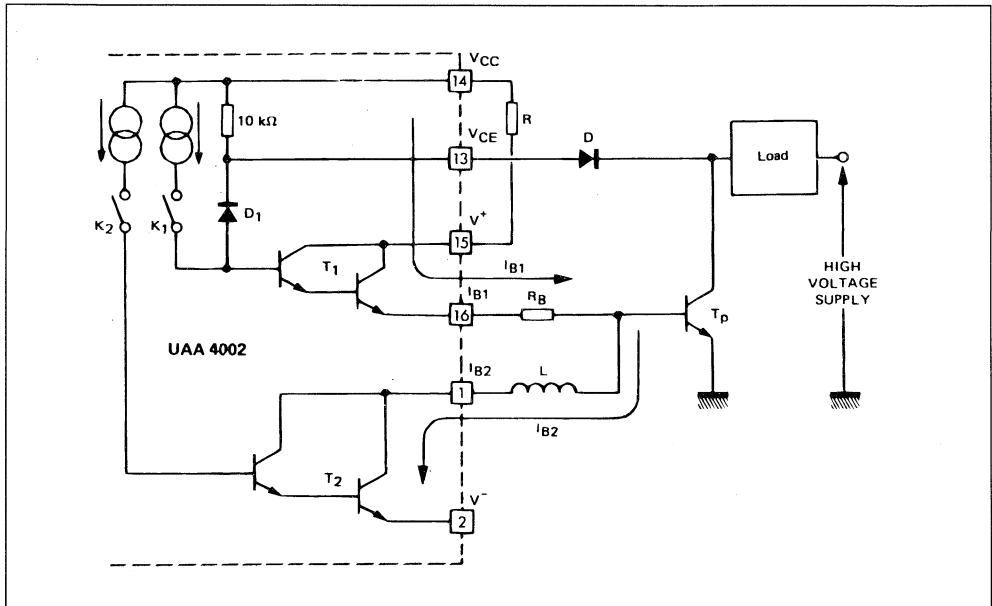
The highly sophisticated output stage of the UAA4002 offers high performance in terms of switching transistor control. Its principal features are as follows :

- the switching transistor can be direct driven,

- the transistor is maintained in a quasi-saturated state, hence reduced storage time,
- control power is limited to the strict minimum.

This stage is in fact in two parts, a positive driver stage which turns on the transistor and a negative driver stage which turns off the transistor.

Figure 16 : UAA4002 Output Stage.



Power transistor conduction

Conduction in the power transistor is brought about by closing contact K_1 (see figure 16). The Darlington T_1 is caused to conduct and a positive current I_{B1} flows in the base circuit of power transistor T_P , which also conducts. This base current is self-regulated so as to maintain transistor T_P in a quasi-saturated state. The more this transistor tends to saturate, the greater proportion of current I_{B1} is shunted by diodes D and D_1 . This eliminates the effect of dispersion in power transistor characteristics : whatever the gain of the power transistor, the base current value is that required to maintain the transistor quasi-saturated. The control power is therefore minimized and switching performance optimized.

NOTE : The circuit which has just been described constitutes an anti-saturation device. It should not

be confused with the circuit which protects the power transistor against desaturation, described in section 2.4.

Resistor R_B contributes to stabilization of the base current regulation loop. The resistance of this resistor must be low : a value of approximately 1 Ω will generally suffice. Too high a value increases the saturation voltage of transistor T_P and thus the conduction losses. Resistor R_B may even be omitted if oscillation in the base current of transistor T_P , if any, may be ignored.

The saturation voltage of transistor T_P during conduction is given by the equation :

$$V_{CEsat} = V_{BE} + R_B \times I_{B1} \text{ if } T_P \text{ is a transistor}$$

$$V_{CEsat} = 2V_{BE} + R_B \times I_{B1} \text{ if } T_P \text{ is a Darlington.}$$

In the above equations, V_{BE} represents the threshold voltage of a base-emitter diode. The Darling-

ton transistor T_1 is connected to the supply through resistor R , which sets the maximum base current $I_{B1 \max}$:

$$I_{B1 \max} = \frac{V_{CC} - V_{BE} - V_{CEsat} T_1}{R + R_B}$$

This expression applies if T_P is a transistor. When using a Darlington, it is only necessary to replace the term V_{BE} with $2V_{BE}$.

Current $I_{B1 \max}$ must provide for quasi-saturation of transistor T_P for the maximum collector current and for the minimum gain of the power transistor used. Nevertheless, $I_{B1 \max}$ must be less than 0.5A, the maximum current which the Darlington T_1 can carry.

$$I_{C \max} / H_{21 \min} < I_{B1 \max} < 0.5A$$

$V_{CEsat} T_1$ is the saturation voltage of Darlington T_1 , typically 1.2V for a current I_{B1} of 0.5A.

If the switching transistor requires a base current of more than 0.5A, the available current may be in-

creased by associating one or more external transistors with the UAA4002.

Turn-off switching of the power transistor

The closing of contact K_2 (figure 17) causes Darlington T_2 to conduct. The negative supply voltage is applied to the base of transistor T_P and a high negative base current I_{B2} flows, permitting the rapid evacuation of charges stored in the base-emitter junction of transistor T_P .

A low-value inductor L may be required between the base of transistor T_P and the I_{B2} output of the UAA4002, so as to limit the gradient dI_{B2}/dt . In many cases, this inductor is not required.

The Darlington T_2 can carry a maximum current of 3A. The corresponding saturation voltage is typically 3V. Like the positive stage, this stage is designed for easy augmentation of the available output current by the addition of one or more external transistors.

Figure 17 : The external NPN transistor provides for increasing the base current of power transistor T_P to several amperes.

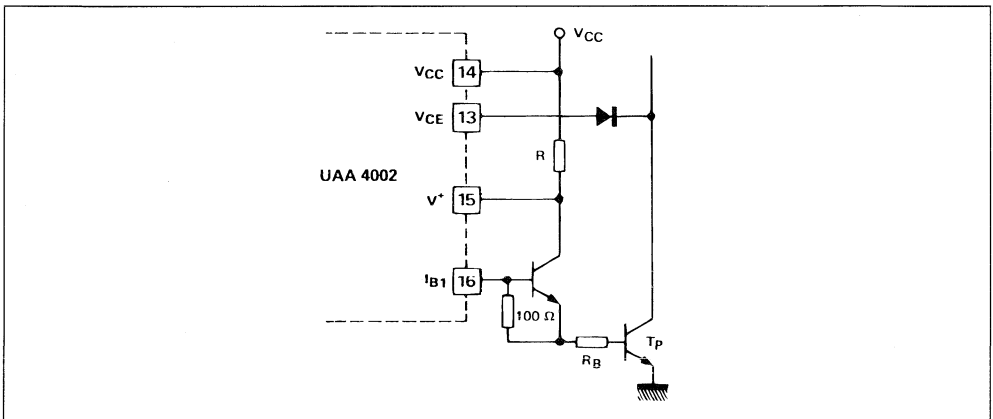


Figure 18 : The external NPN transistor increase the negative current available while decreasing the power dissipation in the UAA4002.

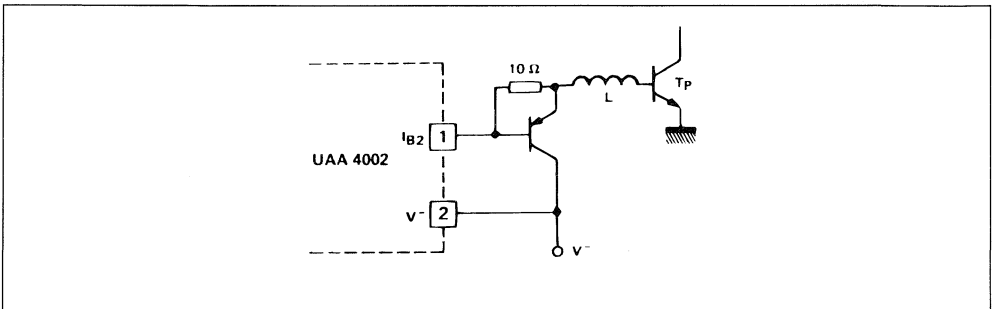
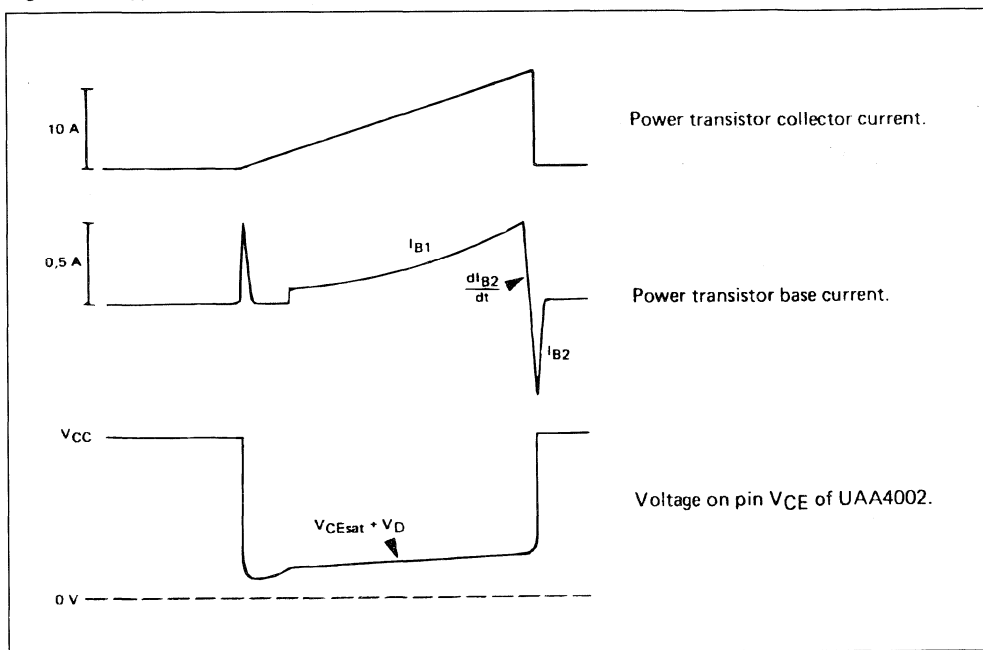


Figure 19 : Typical Inductive Load Waveforms.

When conduction begins, the base current assumes a high value briefly and then reverts to zero. This base current spike permits rapid switching on of the power transistor. The base current value is then that

required for quasi-saturation of the transistor. The base current curve is generally curved upwardly, due to the decreased gain of the power transistor with increased collector current.

3. HINTS TO USERS AND SPECIFIC APPLICATIONS OF THE UAA4002

3.1. HINTS TO USERS

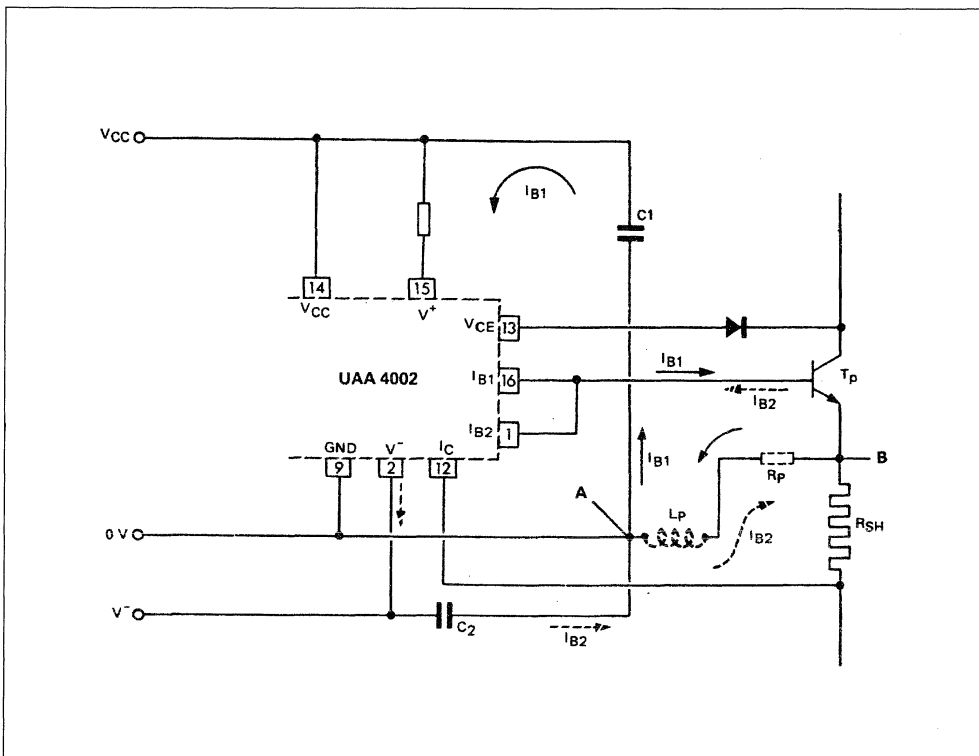
By adding external current amplifiers, the UAA4002 may be utilized in high-power equipments and used to control circuits switching currents of more than 100A at voltages up to several hundred volts and at very high switching speeds.

As an interface circuit the UAA4002 processes low-

RECOMMANDATIONS REGARDING WIRING

Figure 20 shows unsuitable wiring.

Figure 20: UAA4002 Application Susceptible to Malfunction.



The base current of the power transistor takes positive and negative peak values with high values of dB/dt . These result in high voltage drops and over-voltages in the ground connection between points A and B, the stray inductance here being shown in

energy signals which are susceptible to perturbation if certain precautions are not taken. The importance of perturbation phenomena should not be exaggerated, however. Any perturbation has a specific source, and there is always a way to eliminate it or attenuate its effects.

The purpose of this section is to set out certain rules, concerning wiring in particular, which will secure reliable operation of the UAA4002 and the associated switching device in short order.

dotted line. These spurious voltages are superimposed on I_c and V_{CE} and disrupt the measurement of these parameters. Generally this results in the detection of a non-existent fault condition which stops the conduction.

To correct the wiring of this circuit, the emitter of the power transistor must be regarded as a central grounding point.

Specifically, decoupling capacitors C_1 and C_2 must be connected directly to this point.

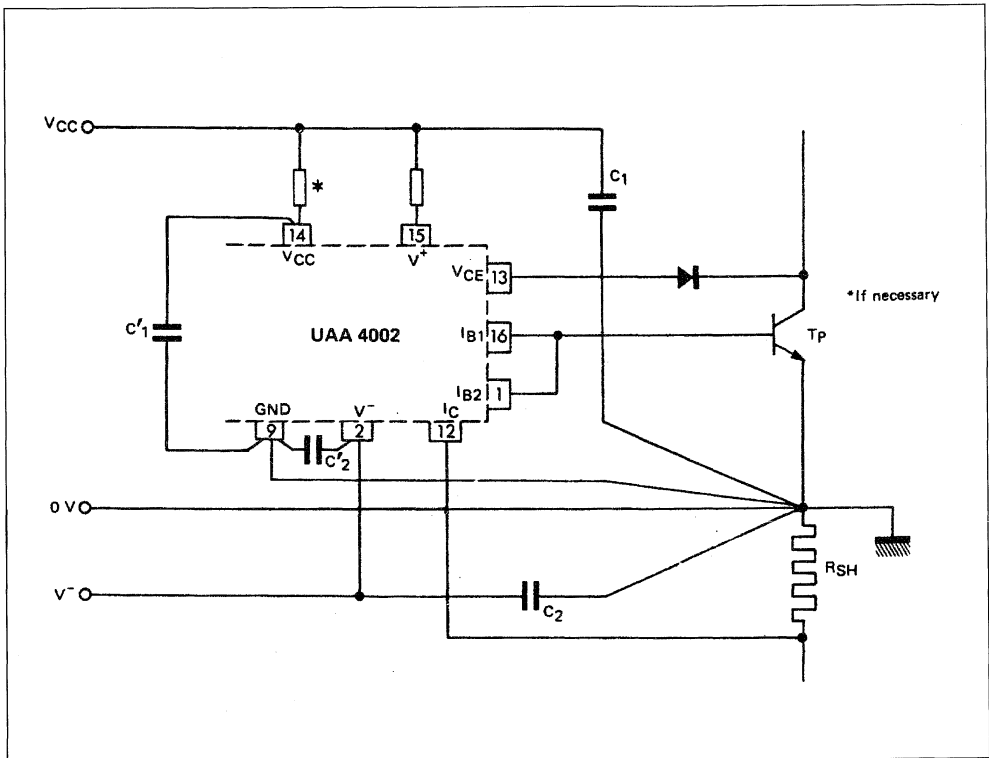
Also, as the base current of the power transistor is high when conduction starts, a transient decrease in the circuit supply voltage V_{CC} will generally be observed, in spite of the presence of filter capacitor C_1 .

An analogous phenomenon affects the negative supply voltage when the transistor is turned off. These transient voltage drops may trigger the supply voltage monitoring function, cutting off the conduction.

For this reason, it may be necessary to apply further supply voltage filtering, very close to the pins of the integrated circuit.

The final result is the circuit shown in figure 21.

Figure 21 : Correct Wiring of the UAA4002.



The emitter of the power transistor is taken as the central grounding point. The decoupling capacitors

must be of high quality (low inductance and low series resistance).

Persistent $t_{on\ min}$ operation

When developing a switching circuit using the UAA4002, it may be noticed that the conduction time cannot be made to exceed the minimum conduction time $t_{on\ min}$.

This is due to triggering of one the power transistor protection functions : collector current monitoring, protection against desaturation, circuit power supply voltage monitoring.

To overcome this fault, it is necessary to determine which function is responsible. To do this it is merely necessary to disable the functions one by one. When normal conduction is obtained, the protection function which is disabled at that time is the subject one.

Important note :

Remember that the duration $t_{on\ min}$ must be sufficient to allow the power transistor collector-emitter voltage to fall when conduction begins (see section 2.4.). In many cases, persistent $t_{on\ min}$ operation is due to the programming of too short a value for $t_{on\ min}$.

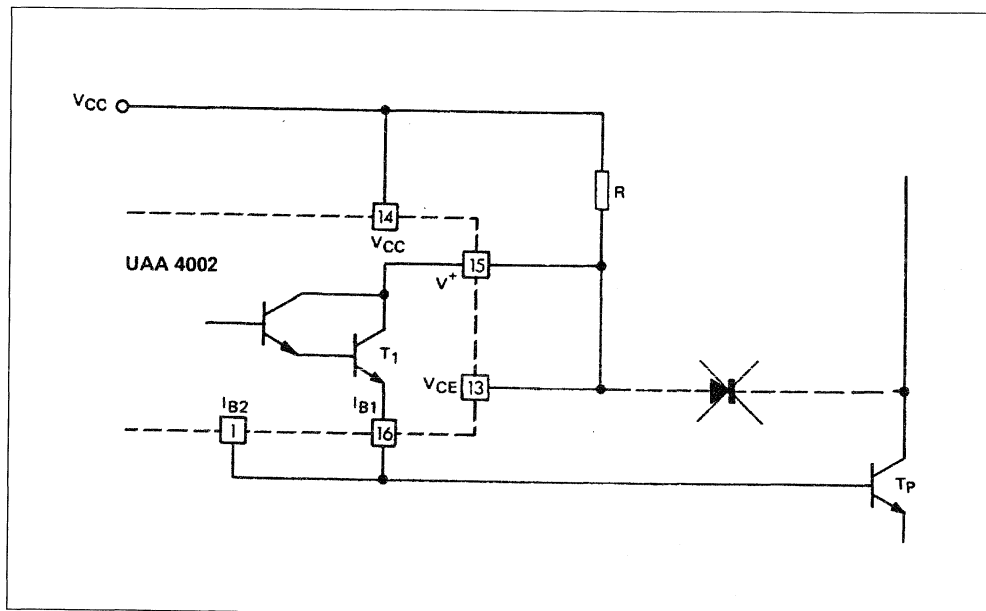
3.2. DISABLING THE ANTI-SATURATION PROTECTION DEVICE

In normal utilization of this integrated circuit, the switching transistor base current is self-regulated so as to maintain the transistor quasi-saturated. This brings about a significant improvement in the switching performance of the power transistor, but also slightly increases conduction losses, as compared with fully saturated operation.

It is possible to disable the base current regulation loop, in which case the UAA4002 supplies the power transistor with constant base current which is independent of the collector current.

This is achieved by disconnecting the diode between the power transistor collector and input V_{CE} of the UAA4002 and connecting pins V_{CE} and V^+ together.

Figure 22 : Base Current Regulation Disabling.



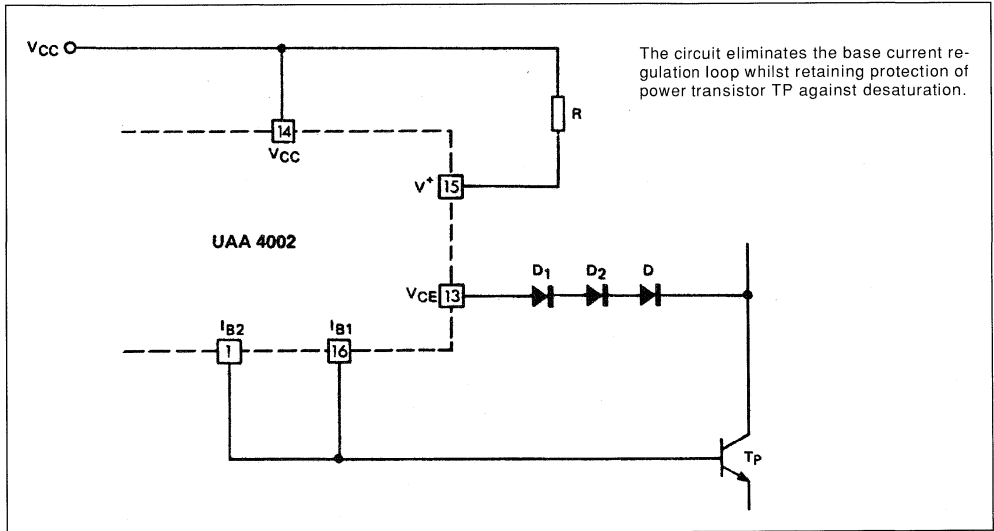
The base current is of constant amplitude, set by the value of resistor R.

The positive base current amplitude is given by the equation :

$$I_{B1} = \left(\frac{V_{CC} V_{BE TP} V_{CEsat T1}}{R} \right)$$

In this equation, $V_{BE TP}$ is the power transistor base-emitter voltage and $V_{CEsat T1}$ is the saturation voltage of the UAA4002 output stage.

Figure 23.



The addition of diodes D_1 and D_2 in series with diode D eliminates the base current regulation loop, and the UAA4002 produces a current whose value is determined by resistor R . The collector-emitter voltage is still monitored, but the difference between the voltage on pin V_{CE} and the collector voltage of power transistor T_P is equal to three diode threshold voltages. The effective threshold of the desaturation protection circuit is thus reduced by an amount equivalent to two diode threshold voltages, as compared with normal utilization of the circuit. This is not a problem since total saturation of the power transistor decreases the voltage V_{CEsat} .

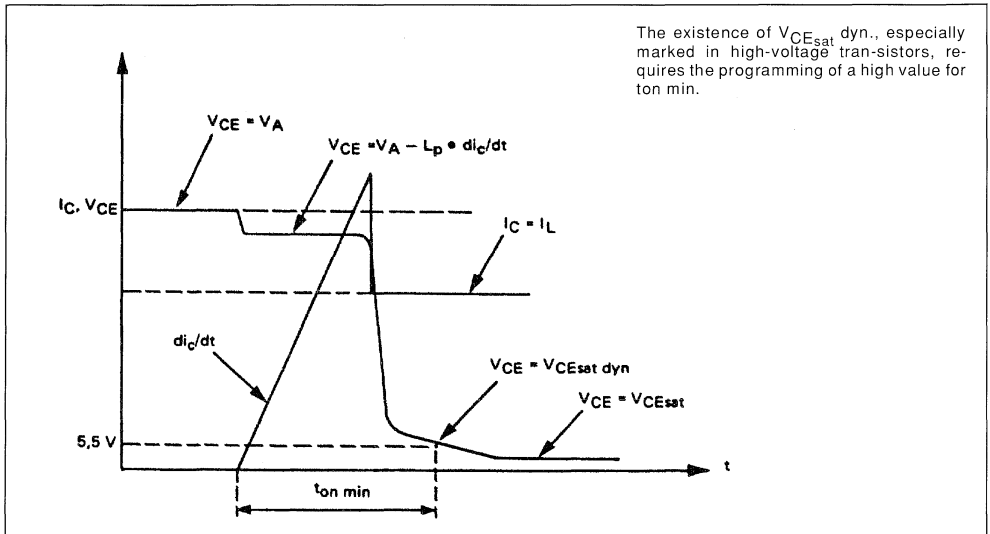
The solution just described has the advantage of being simplicity itself to apply. Its disadvantage is that it eliminates the protection of the power transistor against desaturation.

The circuit shown in figure 23 may be used if this protection function is to be retained.

3.3. PROTECTION AGAINST DESATURATION WITH THRESHOLD EXCEEDING 5.5V

It may be desirable to set a threshold for the circuit protecting the power transistor against desaturation which exceeds 5.5V. Consider, for example, a high-voltage switching transistor. When the transistor begins to conduct, the collector-emitter voltage falls in two stages : in the first stage it falls rapidly and then, in the second stage when the collector-emitter voltage is only a few volts, further decrease to the static saturation value is much slower. The corresponding value of voltage V_{CE} is designated "dynamic saturation voltage" ($V_{CEsat dyn}$).

Figure 24 : Turn-on with Inductive Load and Initial Current.

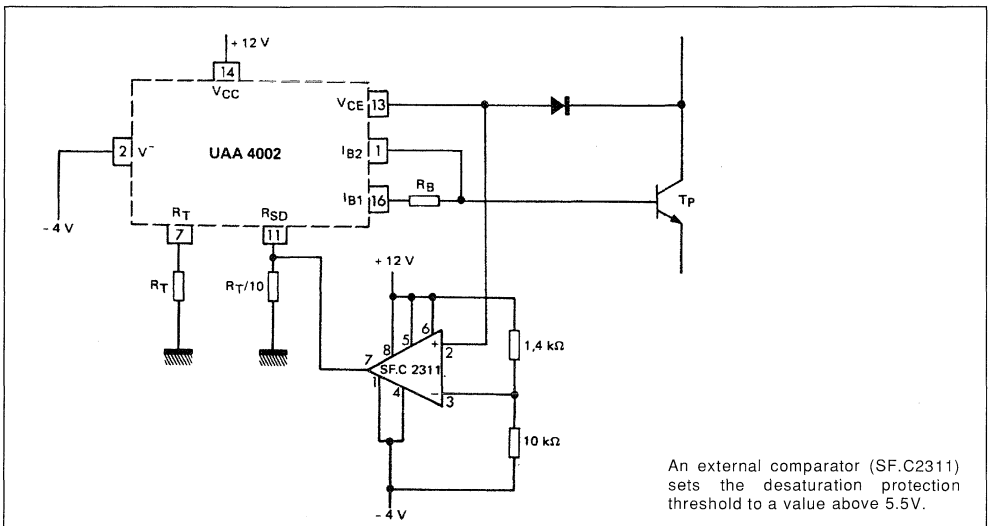


When the power transistor begins to conduct, the duration defined for $t_{on\ min}$ must be sufficient to permit the collector emitter voltage to drop below the desaturation detection threshold (see section 2.4.). The existence of $V_{CEsat\ dyn.}$ imposes values for $t_{on\ min}$ which can sometimes be excessive. This problem is overcome by setting a desaturation detection threshold above the usual value of 5.5V.

It then becomes possible to choose a value for $t_{on\ min}$ which enables the collector-emitter voltage to fall while securing a sufficiently short reaction time in the event of a collector current overload.

Figure 25 shows a simple and economic circuit for achieving this result.

Figure 25.



Operation

The detection threshold is programmed on the inverting input of the comparator. With the resistor values indicated on figure 25, the threshold is approximately 10V. As long as the voltage on pin V_{CE} is below 10V, the output of the comparator is "low", the voltage on pin R_{SD} is approximately 4V, and the protection against desaturation function is disabled. As soon as the voltage on pin V_{CE} exceeds 10V, the comparator changes state, the desaturation protection function is

not longer disabled, and the fault is detected.

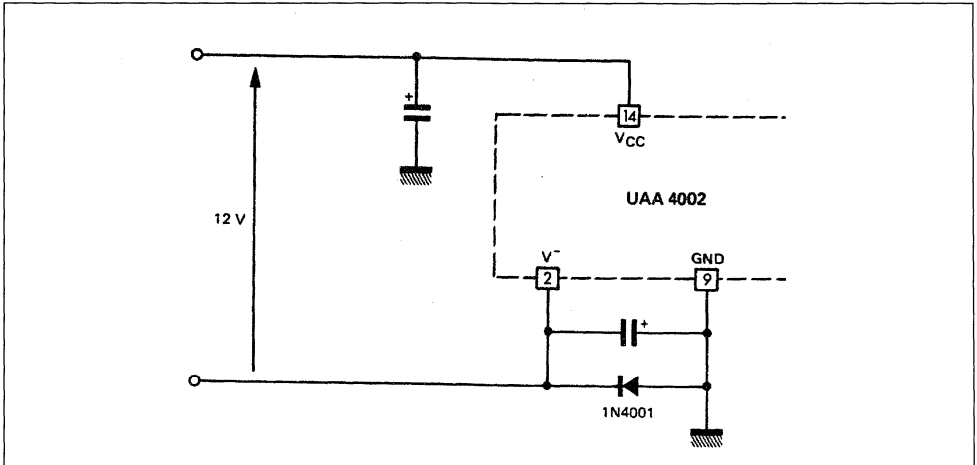
3.4. USING THE UAA4002 WITHOUT NEGATIVE POWER SUPPLY

To operate correctly, the UAA4002 requires a negative supply voltage not less than a diode threshold voltage :

$$|V_-| \geq V_D$$

If a negative supply is not used, the appropriate biasing may be achieved using a diode.

Figure 26 : UAA4002 Application without Negative Power Supply.



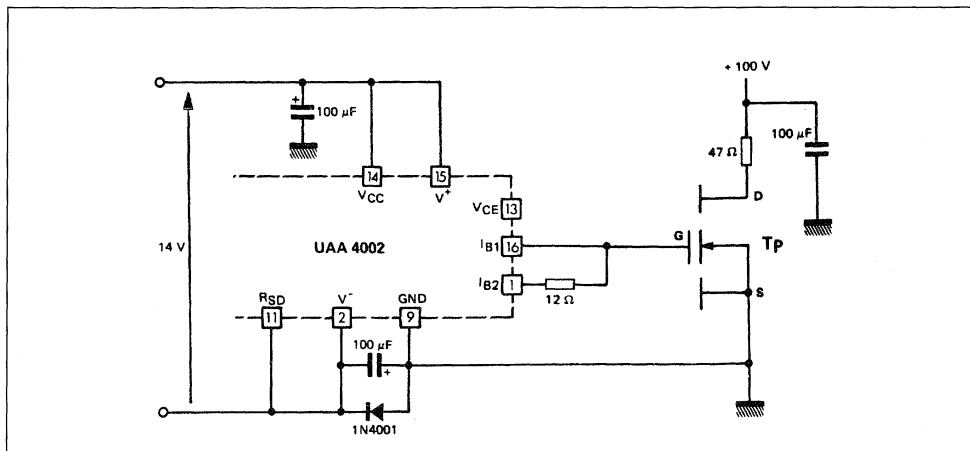
The voltage drop across the 1N4002 diode is sufficient to polarize the substrate of the integrated circuit.

3.5. CONTROL OF MOS POWER TRANSISTORS

Ideally, MOS power transistors should be voltage-controlled. In practice, in order to benefit from the high speed typical of this type of transistor it is

necessary to charge and discharge the spurious input capacitance at high speed, so that high currents flow. By virtue of the high current capability of its outputs stages, the UAA4002 is particularly suitable for controlling MOS power transistors.

Excellent results are obtained with the circuit shown in figure 27.

Figure 27 : UAA4002 Controlling N-Channel MOS Power Transistor.

The output of the positive stage is connected directly to the gate of the MOS transistor, to switch it into conduction very fast. The negative stage controls the turning off of the MOS transistor, by discharging the gate capacitance of the transistor. There is no

need for a high negative supply voltage, and the arrangement described in the previous section is therefore used.

Figure 28 and 29 show results achieved with this test circuit.

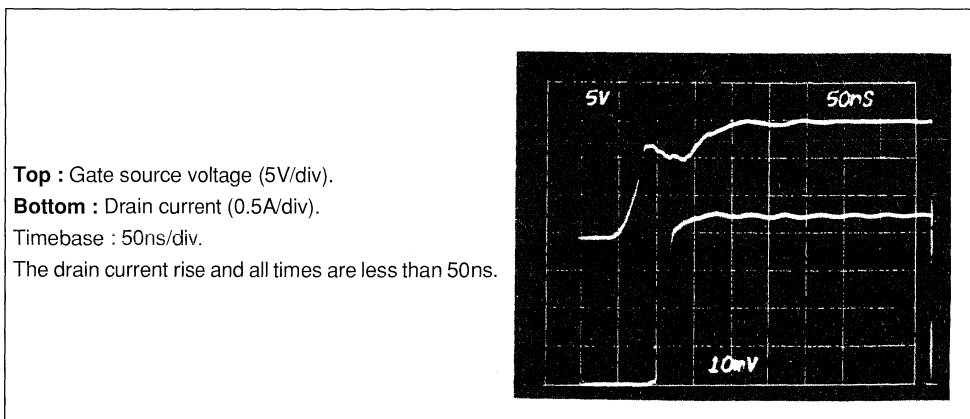
Figure 28 : Switching on the MOS Power Transistor.

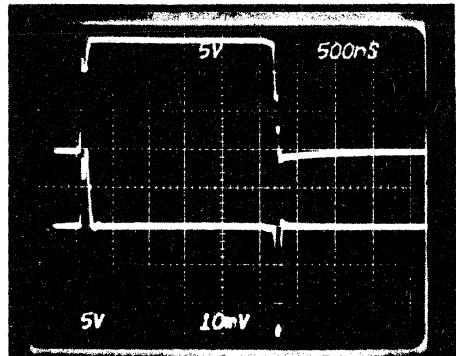
Figure 29.

Top : Gate-source voltage (5V/div).

Bottom : Gate current (0.2A/div).

Timebase : 500ns/div.

The output stages of the UAA4002 conduct only briefly, in order to charge and discharge the MOS transistor input capacitance.



It is thus possible to control a number of MOS transistors in parallel, the output current from the

UAA4002 being sufficient for fast control of devices with an input capacitance of a few nanofarads.

APPENDIX 1

OPTIMIZED BASE DRIVE USING THE UAA4002

Figure 1 illustrates a bridge-type configuration capable of handling **100A** peak-to-peak at **+450V** supply voltage.

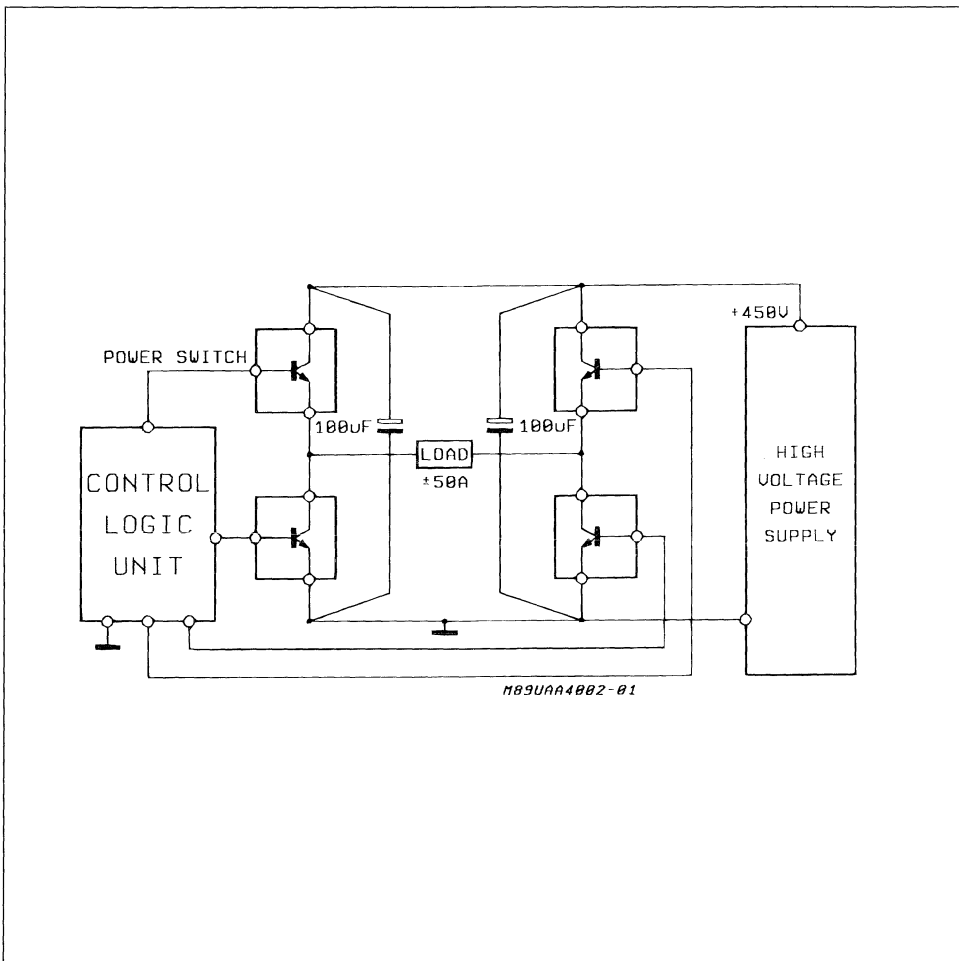
Figure 2 outlines in detail the strict arrangement of this configuration respecting the following guidelines of wiring and board layout :

- Star connection of ground links
- Low level signal inputs and power supplies decoupling.
- Very careful component and track layout so as to minimize the stray capacitances due to wiring.

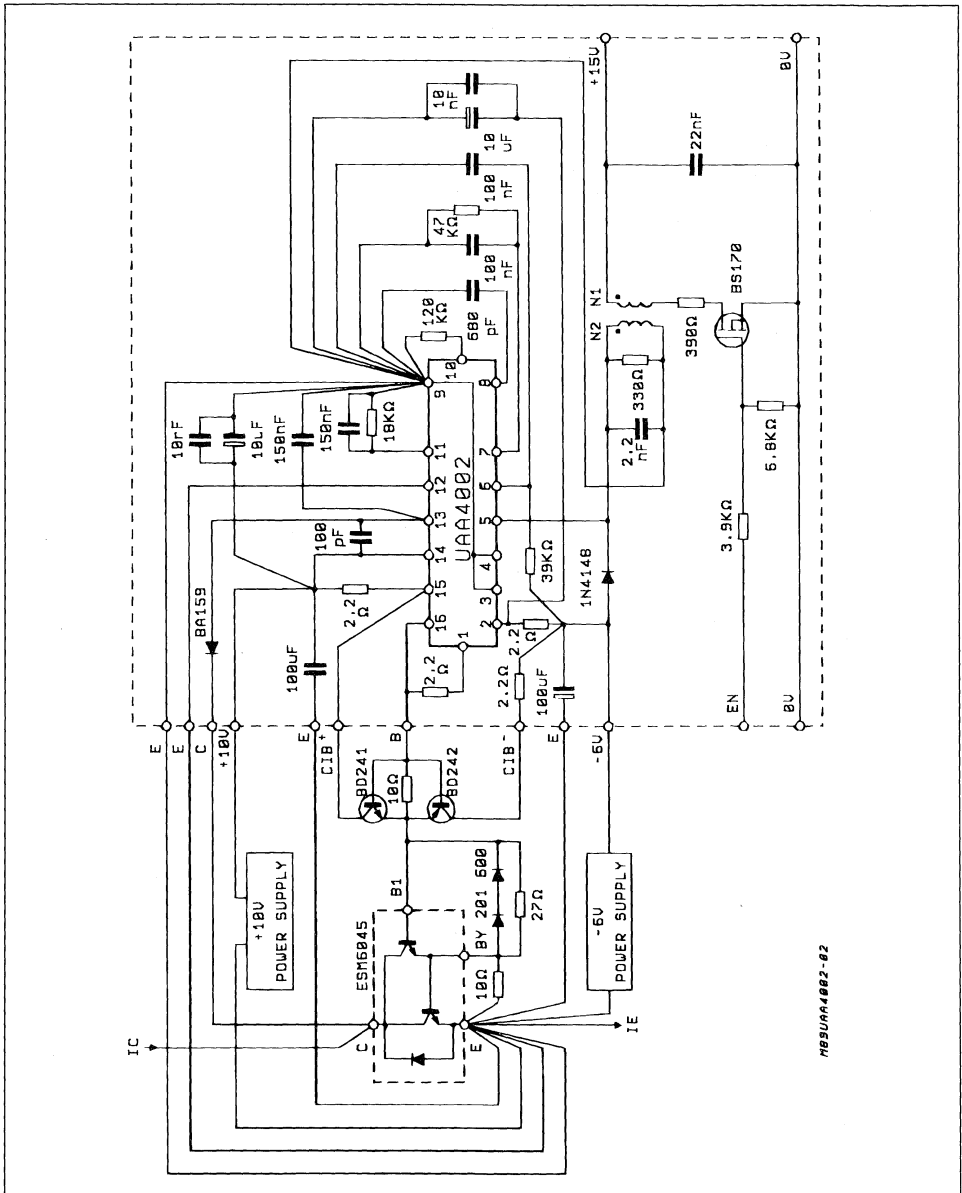
Figure 3 illustrates the board layout in strict conformance with the foregoing rules that we shall analyze next in order to pinpoint the problems which may be encountered in applications built around the UAA4002.

Figure 1 : Bridge Configuration (+ 450V · 100A peak-to-peak).

In a bridge-type configuration, power switches connected to + 450V supply are galvanically isolated from the ground. The 100 μ F filtering capacitors are directly connected across the power switches thereby preventing the occurrence of voltage spikes during switching due to wiring inductances.



The above configuration must be repeated 4 times in order to be used in a H-type arrangement. Care must be taken to galvanically isolate the + 10V and - 6V supplies between individual switches. Note the star connection on pin 9 and the emitter of the switching power transistor - both of which are measurement reference points.



APPENDIX 2

UAA4002 BASIC APPLICATION : 8A - 400V SWITCH

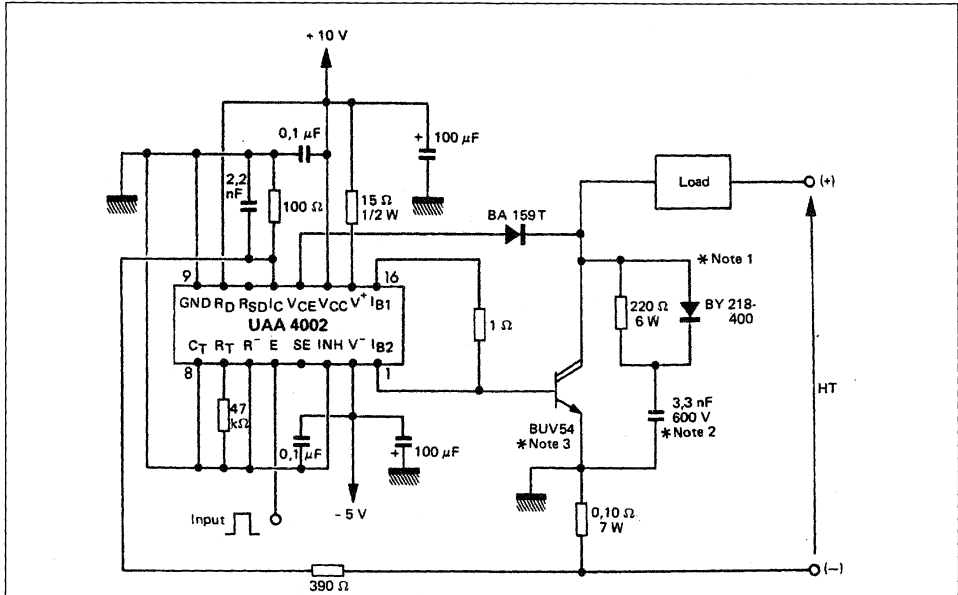
An extremely compact high performance switching circuit is obtained by associating the UAA4002 with

an integrated Darlington.

This appendix describes a module capable of switching 8A at 400V, using a high-voltage integrated Darlington : BUV54.

Figure 1 is a complete circuit diagram of the switching circuit.

Figure 1 : 8A – 400V Switch using UAA4002 and BUV54.



- Notes :**
1. Switching aid network.
 2. Polypropylene capacitor.
 3. With heatsink, R_{TH} 35/W.

In this circuit the UAA4002 is used in a completely conventional manner, in "level" control mode. The time constant $\tau_{on\ min}$ is set at $2.8\mu s$, which is four times the time constant of the snubber network associated with the BUV54 transistor. The positive output stage of the UAA4002 is connected to the V_{CC} rail through a 15 resistor. The maximum base current is approximately $0.45A$. The collector current is measured using a 0.10 shunt, and is limited to $10A$. The BUV54 Darlington, for which the specified value

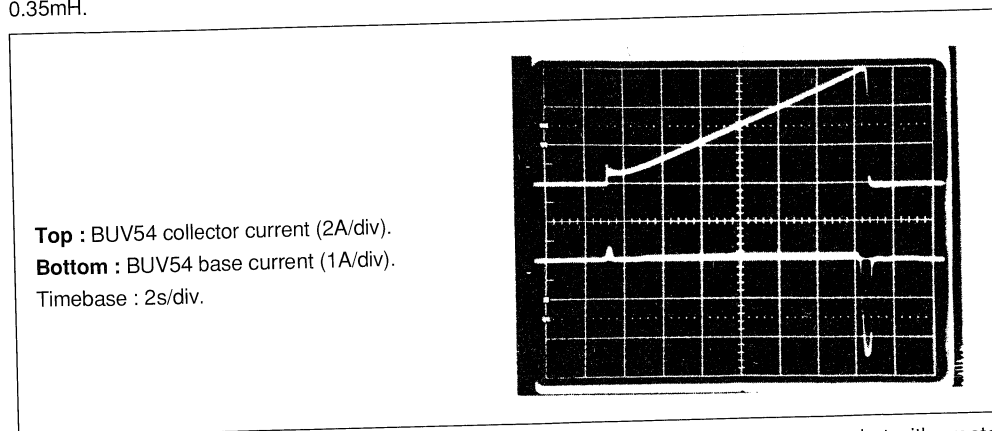
of I_{csat} is 12A, is thus operated with a considerable safety margin.

The resistor power dissipation figures and the thermal resistance of the heatsink are given by way of indication only, as they are highly dependent on operating conditions (ambient temperature, switching frequency, conduction cyclic ratio).

In this application, the disabling, time-delay, negative supply voltage monitoring and $t_{on\ max}$ functions are not used.

Figure 2 : Operation with Inductive Load.

Figure 2 shows the collector and base currents of the BUV54 transistor in the case of an inductive load of 0.35mH.



The amplitude of the positive base current is very much less than that of the negative base current. This is explained by the fact that it is a Darlington which is being switched : the positive base current is that of the driver transistor of the integrated Darlington, the negative current is that of the power transistor of the Darlington. This current flows through a diode connected in head-to-tail relationship to the base-emitter junction of the driver transistor.

Figure 3 shows the same currents, but with greater sensitivity in the case of the base current. This photograph clearly shows the proportional relationship between the base current and the collector current of the power transistor. Naturally, enough, the negative component of the base current is of the screen.

Figure 3.

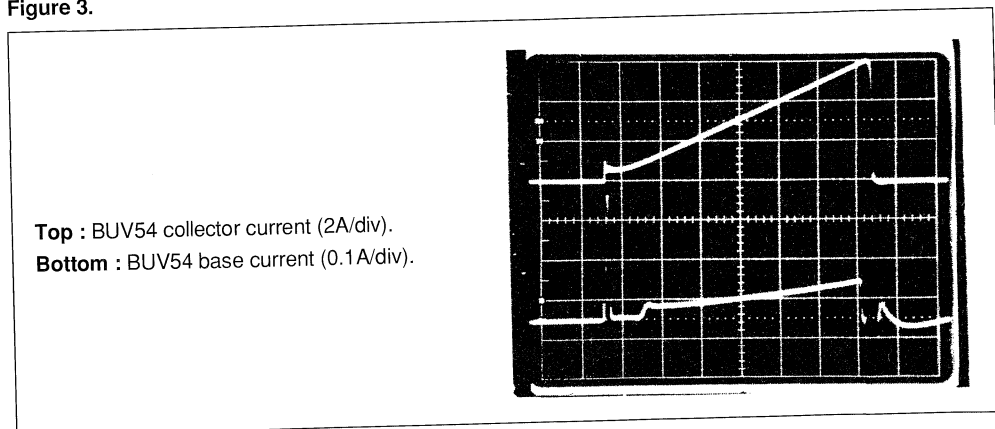
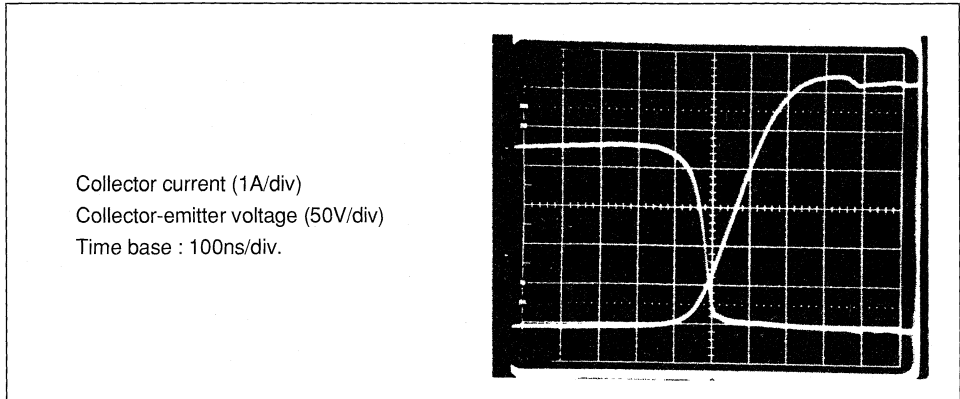


Figure 4 shows the waveform obtained on turning off. The collector current fall time (t_f) is approximately 100ns.

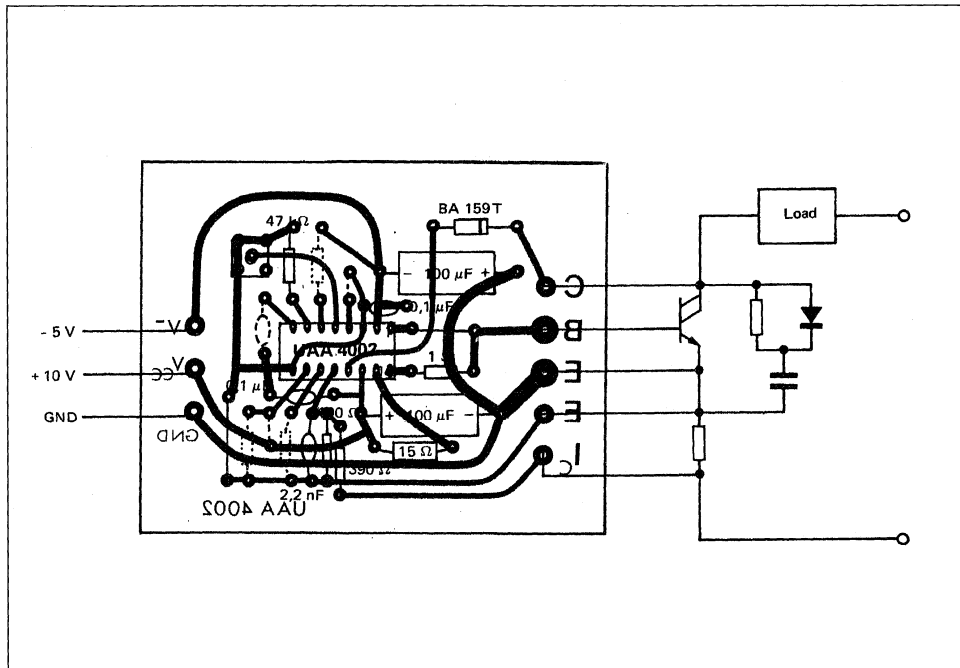
Figure 4 : Power Transistor Turn-off.



A typical implementation of this module on a printed circuit board is shown in figure 5. This implementation provides for utilization of the time-delay, $t_{on\ max}$

and V monitoring functions. The components associated with these functions are shown in dotted line in figure 5a.

Figure 5 : Switching Module printed Circuit Board and Connection to Power Transistor (view on component side).



APPENDIX 3

150W FORWARD TYPE POWER SUPPLY USING UAA4002

The implementation of a "forward" type power supply is considerably facilitated using the UAA4002. In this type of application, the UAA4002 is associated with a UAA494 regulator integrated circuit for switching mode power supplies.

The complementary functions of these two integrated circuits provide for the implementation of economic and high-performance power supplies offering a high level of operational security.

This appendix describes a power supply rated at 150W (25V, 6A) which operates from a 220V mains supply.

Figure 1 is a complete circuit diagram of the power supply.

DESCRIPTION

For good voltage regulation and precise output current limitation, the UAA494 is situated in the secondary part of the power supply. This circuit integrates an oscillator, a pulse width modulator, two error amplifiers and a stable reference voltage source. It therefore contains all components necessary for implementing the regulation and limitation functions with few external components. Also, the UAA494 has two complementary outputs and therefore may be used in power supplies with more than one

switching transistor. Only one output is used in the present application, which uses only one transistor.

The conduction pulses from the pulse width modulator of the UAA494 are transmitted to the UAA4002 via a pulse transformer which provides the vital galvanic isolation between the primary and secondary parts of the power supply. This transformer is implemented economically using a ferrite pot core.

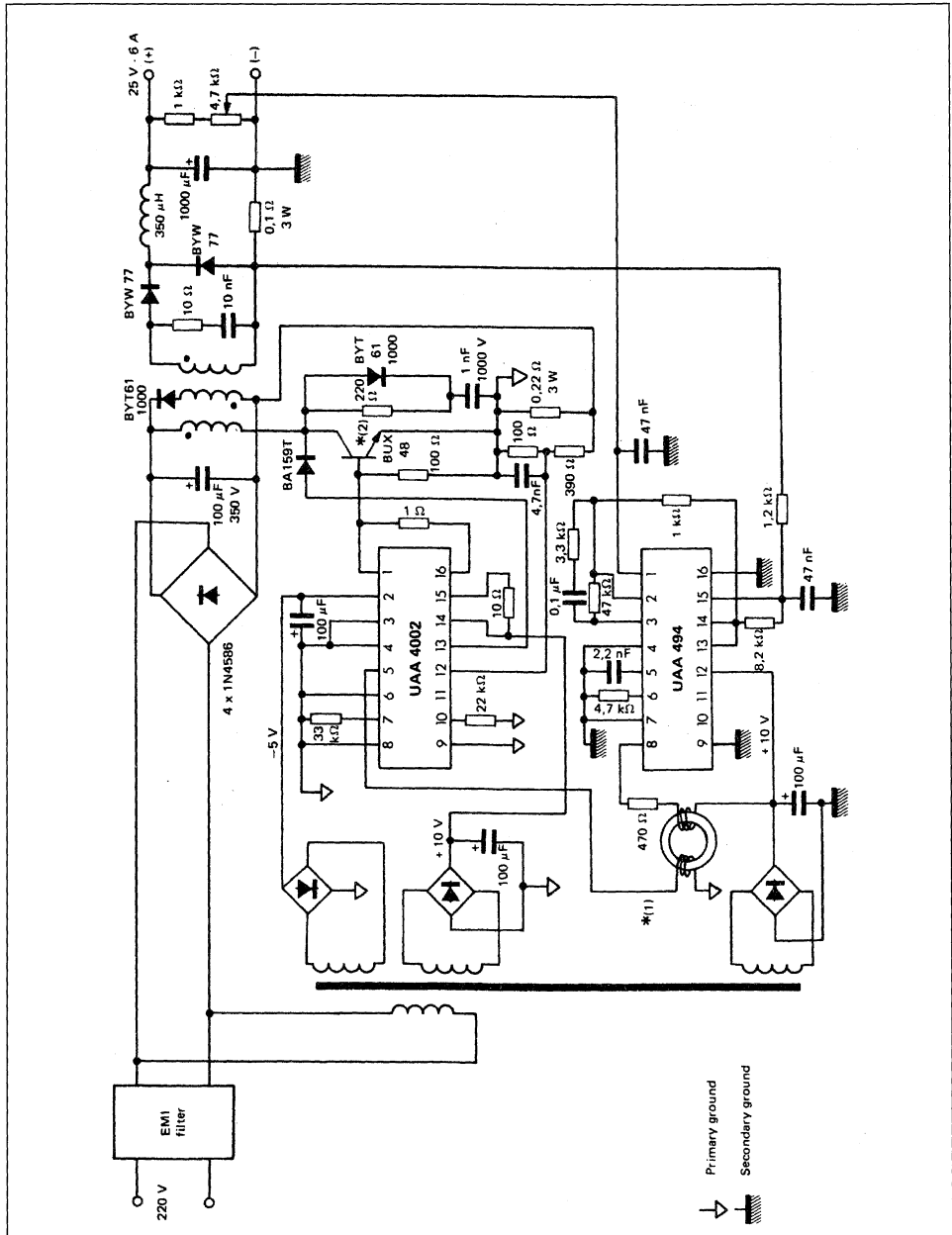
The UAA4002 is thus located in the primary part of the power supply, and generates the base current for the BUX48 high-voltage high-speed switching transistor. It also protects the BUX48, in particular by monitoring the collector current and the collector-emitter saturation voltage during conduction.

The transformer of the chopping circuit uses an EE42 magnetic circuit (material Ferriox B 50) manufactured by LCC. A demagnetization winding very closely coupled to the primary winding recovers the magnetizing energy and provides for limitation of the power transistor collector-emitter voltage on cutting off.

The output of the secondary winding is rectified by two BYW 77-200 high-efficiency fast recovery diodes. Filtering is effected by a 350 μ H inductor and a 1000 μ F electrolytic capacitor.

A low-power 50Hz transformer feeds the UAA4002 and the UAA494. No special starting arrangement is required, as safety is assured on powering and on powering off by the supply voltage monitoring devices in both integrated circuits.

Figure 1 : 150W Converter Operating at 40kHz.



(1) LCC FT10 - T6A ferrite core with 5 primary and 5 secondary turns.

(2) With heatsink.

Performance

- Output voltage stability :

For an input voltage varying from 190 to 245V, the maximum relative variation in the output voltage is 0.7% at nominal operating conditions ($V_{OUT} = 25V$, $I_{OUT} = 6A$).

For a variation in the load from 0 to 100%, the relative variation in the output voltage is 1.3%.

For a variation in the load from 10 to 100% ($I_{OUT} = 0.6$ to $6A$), the relative variation in the output voltage is 0.4%.

- Efficiency : 80% under nominal operating conditions.
- Behaviour on overload :

The power supply is fully protected against over-

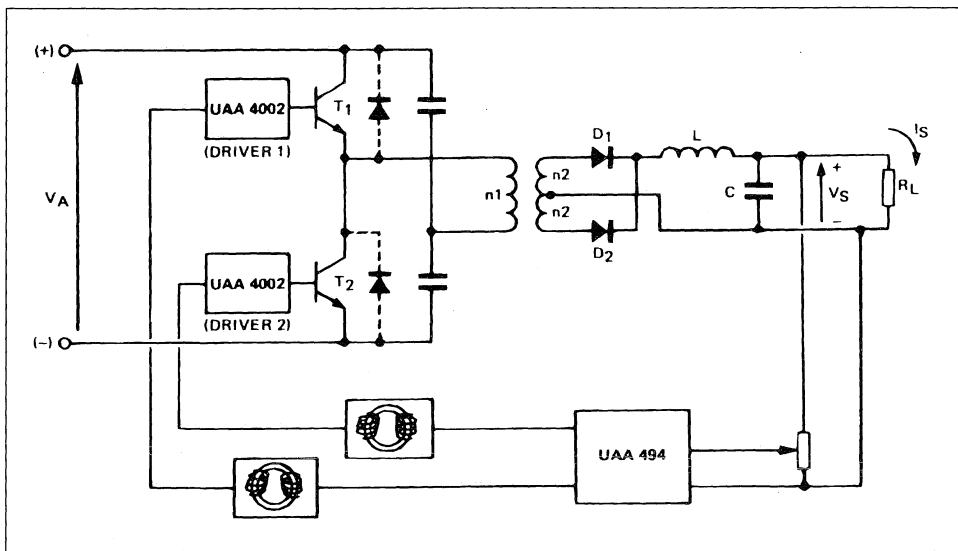
loads and short-circuits, the output current being limited to 7A.

Converter using more than one switching circuit

Where the power transmitted is high, converters using a number of transistors may be substituted with advantage for the direct type converter with a single transistor as described above. This category of devices includes half-bridge asymmetrical direct converters and symmetrical converters.

The combination of integrated circuits UAA4002 and UAA494 previously described is readily adapted to this type of converter. Figure 2 is a block schematic showing a half-bridge symmetrical converter (capacitor type) using a UAA494 and two UAA4002 integrated circuits.

Figure 2 : Capacitor Type Half-bridge Symmetrical Converter.



The UAA494 has its complementary outputs connected to two UAA4002 circuits through pulse transformers. The conduction signals are transmitted to the UAA4002 circuits alternately.

Conclusions :

The foregoing description indicates that the combination of integrated circuits for controlling switching

transistors and regulator integrated circuits considerably simplifies the design of transistorized switching circuits. The integration of security functions and optimum base current control circuits ensure optimum use of the power transistors and remarkably high levels of performance and reliability.

APPENDIX 4**A 200A, 70V TRANSISTORIZED SWITCH****Today power transistors can control several hundreds of kilowatts.**

Switching in high power electronic systems is not exclusively reserved to thyristors, because transistors carrying high currents and voltages have existed for several years.

Advantages of transistors are wellknown

- easy to turn off
- high frequency switching
- few components required for a switch

Transistors have become more performant

A few years ago, it was not possible to control more than ten kilowatts, today several hundreds of kilowatts can be controlled with transistors :

- This has been made possible by :
- increasing active areas of transistors
- higher blocking voltages
- optimization of transistor's technology
- simplification of parallel connection of transistors
- the Darlington connection
- base drive circuits highly suitable for high power

A 200A, 700V switch

This application example is a 200A, 700V switch, operating directly on the rectified 380V mains. Four parts can be distinguished :

- a) Input : the input level is TTL, the galvanic isolation is ensured by a pulse transformer.
- b) Interface and protection : these two functions are insured by the UAA4002.
- c) Boosters : the output current of the IC is amplified to a level necessary to drive a high power transistor.

For a fast switching of a power transistor :

- The driver stage which turns on the transistor must deliver a fast rising base current,
- the driver stage which turns off the transistor must carry a high negative base current and this with a slight negative bias on the base.

The booster proposed here ensures all these conditions.

- d) The power part : It uses 3 transistors ESM4017 housed in MU86 (Press pack) case.

Conclusion :

Technological progress made in the high power transistor area, now allow the realization of switches carrying high currents and voltages.

Experience shown that high power transistors are as easy to use as low power transistors under the condition that care is taken for wiring and using a good base drive.

UC3842 PROVIDES LOW-COST CURRENT-MODE CONTROL

The fundamental challenge of power supply design is to simultaneously realize two conflicting objectives: good electrical performance and low cost. The UC3842 is an integrated pulse width modulator (PWM) designed with both these objectives in mind. This IC provides designers an inexpensive controller with which they can obtain all the performance advantages of current-mode operation. In addition, the UC3842 is optimized for efficient power sequencing of off-line converters and for driving increasingly popular POWERMOS.

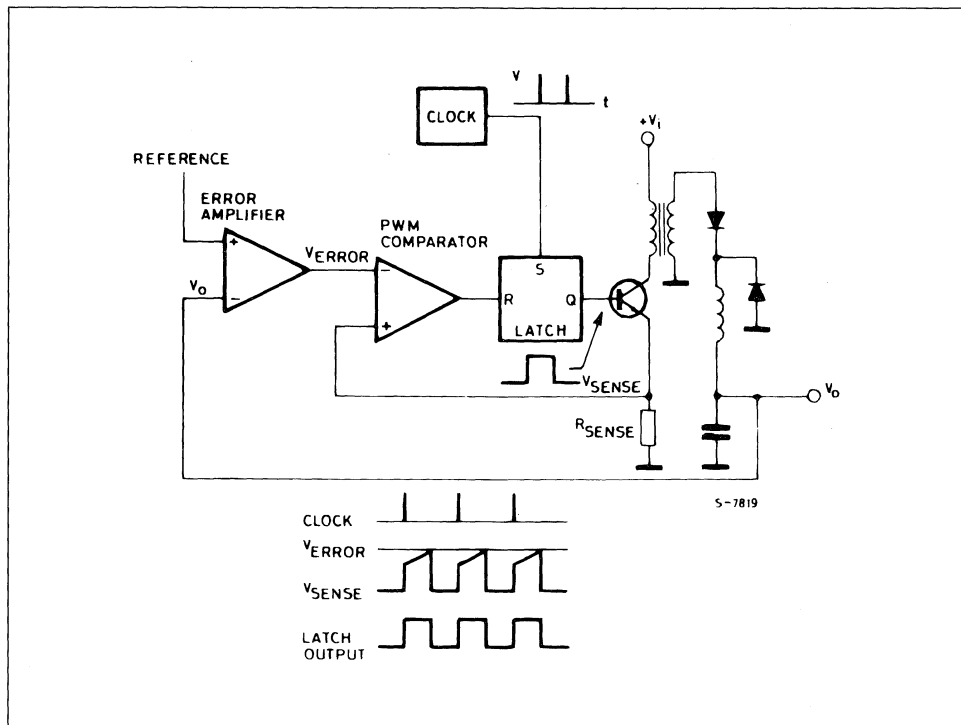
This application note gives a functional description of the UC3842 and suggests how to incorporate the IC into practical power supplies. A review of current-mode control and its benefits is included and meth-

ods of avoiding common pitfalls discussed. The final section presents designs of two power supplies utilizing UC3842 control.

CURRENT-MODE CONTROL

Figure 1 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

Figure 1 : Two-loop Current-mode Control System.



Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved ; i.e., the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an error-voltage-controlled-current-source for the purposes of small-signal analysis. This is illustrated by figure 2. The two-pole control-to-output frequency response of these converters is reduced to a single pole (filter capacitor in parallel with load) response.

One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gain-bandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler and better behaved, as illustrated in figure 3. Capacitor C_i and resistor R_{iz} in figure 3a add a low frequency zero which cancels one of the two control-to-output poles of non-current-mode converters. For large-

signal load changes, in which converter response is limited by inductor slew rate, the error amplifier will saturate while the inductor is catching up with the load. During this time, C_i will charge to an abnormal level. When the inductor current reaches its required level, the voltage on C_i causes a corresponding error in supply output voltage. The recovery time is $R_{iz} C_i$, which may be milliseconds. However, the compensation network of figure 3b can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_i .

Figure 2 : Inductor Looks Like a Current Source to Small Signals.

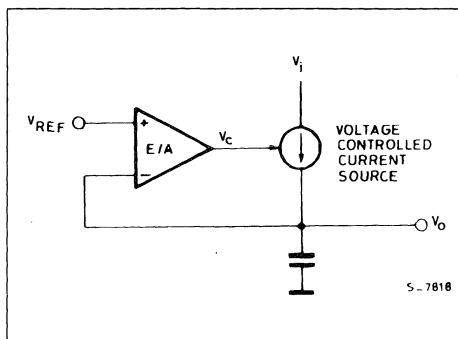


Figure 3 : Required Error Amplifier Compensation for Continuous Inductor Current Designs using (a) Duty-cycle Control and (b) Current-mode Control.

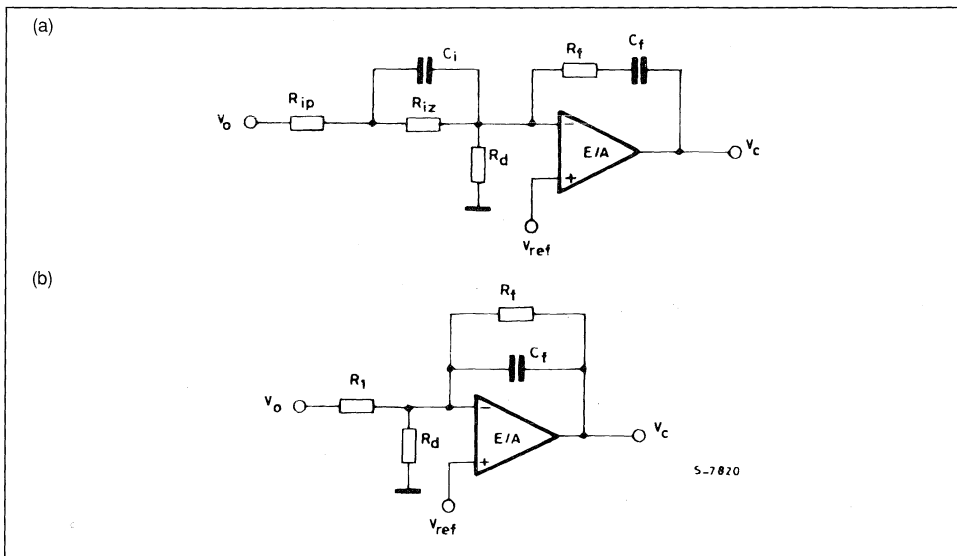
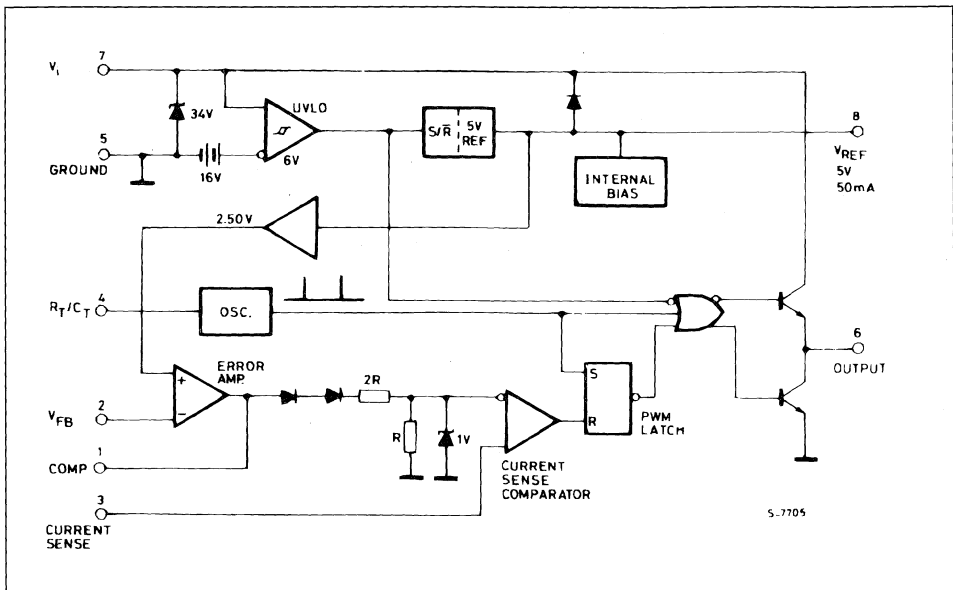


Figure 4 : UC3842 Block Diagram.



Current limiting is simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

FUNCTIONAL DESCRIPTION

A block diagram of the UC3842 appears in figure 4. This IC will operate from a low impedance DC source of 10 V to 30 V. Operation between 10 V and 16 V requires a start-up bootstrap to a voltage greater than 16 V in order to overcome the under-voltage lockout. V_{CC} is internally clamped to 34 V for operation from higher voltage current-limited sources ($I_{CC} \leq 30$ mA).

UNDER-VOLTAGE LOCKOUT (UVLO)

This circuit insures that V_{CC} is adequate to make the UC3842 fully operational before enabling the output

stage. Figure 5a shows that the UVLO turn-on and turn-off thresholds are fixed internally at 16 V and 10 V respectively. The 6 V hysteresis prevents V_{CC} oscillations during power sequencing. Figure 5b shows supply current requirements. Start-up current is less than 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by figure 6. During normal circuit operation, V_{CC} is developed from auxiliary winding W_{AUX} with D_1 and C_{IN} . At start-up, however, C_{IN} must be charged to 16 V through R_{IN} . With a start-up current of 1 mA, R_{IN} can be as large as 100 k Ω and still charge C_{IN} when $V_{AC} = 90$ V RMS (low line). Power dissipation in R_{IN} would then be less than 350 mW even under high line ($V_{AC} = 130$ V RMS) conditions.

During UVLO, the UC3842 output driver is biased to a high impedance state. However, leakage currents (up to 10 μ A), if not shunted to ground, could pull high the gate of a POWERMOS. A 100 k Ω shunt, as shown in figure 6, will hold the gate voltage below 1 V.

Figure 5 : (a) Under-voltage Lockout and (b) Supply Current Requirements.

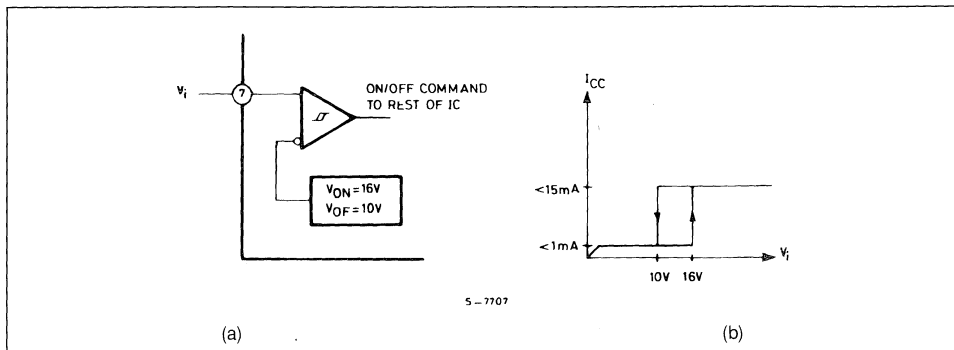
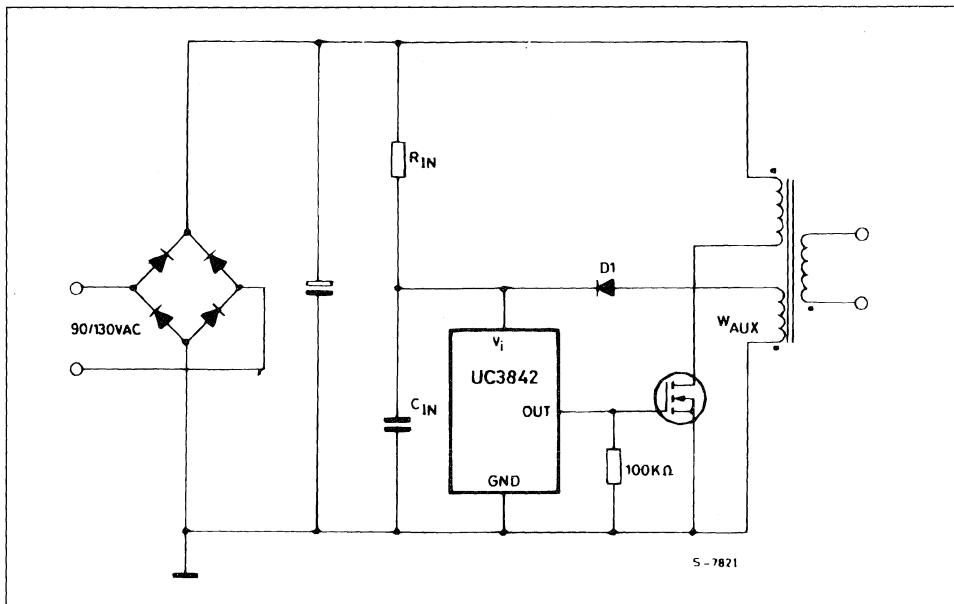


Figure 6 : Providing Power to the UC3842.



OSCILLATOR

The UC3842 oscillator is programmed as shown in figure 7a. Oscillator timing capacitor C_T is charged from V_{REF} (5 V) through R_T , and discharged by an internal current source. Charge and discharge times are given by :

$$t_c \approx 0.55 R_T C_T$$

$$t_d \approx R_T C_T \ln \left(\frac{0.0063 R_T - 2.7}{0.0063 R_T - 4.0} \right)$$

frequency, then, is : $f = \frac{1}{t_c + t_d}$

For $R_T > 5 \text{ k}\Omega$, t_d is small compared to t_c , and :

$$f \approx \frac{1}{0.55 R_T C_T} \approx \frac{1.8}{R_T C_T}$$

During the discharge time, the internal clock signal blanks the output to the low state. Therefore, t_d limits maximum duty cycle (D_{MAX}) to :

$$D_{MAX} = \frac{t_c}{t_c + t_d} = 1 - \frac{t_d}{\tau}$$

where $\tau = 1/f =$ switching period.

The timing capacitor discharge current is not tightly controlled, so t_d may vary somewhat over tempera-

ture and from unit to unit. Therefore, when very precise duty cycle limiting is required, the circuit of figure 7b is recommended.

One or more UC3842 oscillators can be synchronized to an external clock as shown in figure 8. Noise immunity is enhanced if the free-running oscillator frequency ($f = 1/(t_c + t_d)$) is programmed to be ~ 20 % less than the clock frequency.

Figure 7 : (a) Oscillator Timing Connections and (b) Circuit for Limiting Duty Cycle.

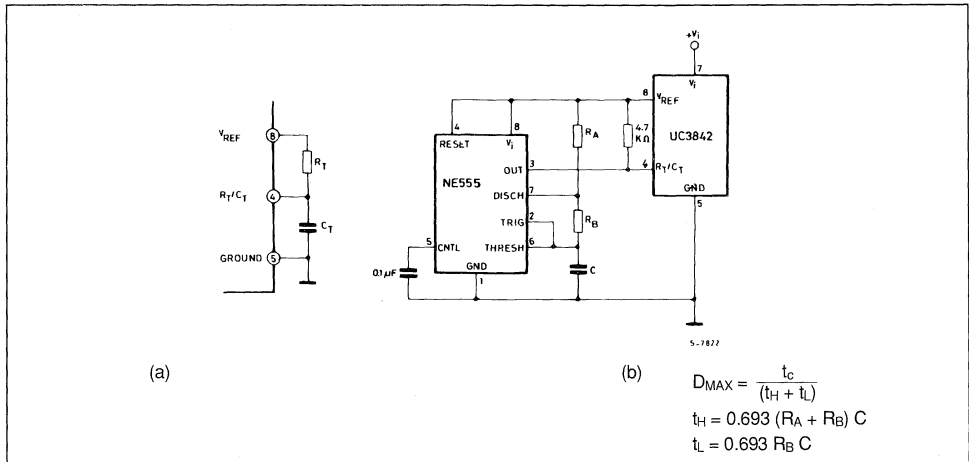
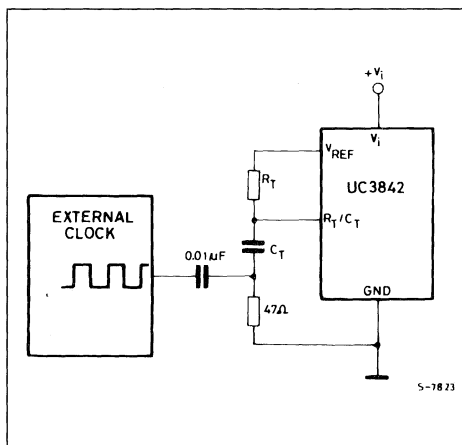


Figure 8 : Synchronization to an External Clock.



ERROR AMPLIFIER

The error amplifier (E/A) configuration is shown in figure 9. The non-inverting input is not brought out

to a pin, but is internally biased to $2.5\text{ V} \pm 2\%$. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 10a shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with continuous inductor current. The feedback components add a pole to the loop transfer function at $f_p = 1/2\pi R_i C_i$. R_i and C_i are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_i and R_f fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to unity (0dB) at $f \approx f_{\text{switching}}/4$. This technique insures converter stability while providing good dynamic response.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_p and C_p in the circuit of figure 10b provide this pole.

APPLICATION NOTE

The E/A output will source 0.5 mA and sink 2 mA. A lower limit for R_f is given by :

$$R_f(\text{MIN}) \approx \frac{V_{E/A \text{ OUT}(\text{max})} - 2.5 \text{ V}}{0.5 \text{ mA}} = \frac{6 \text{ V} - 2.5 \text{ V}}{0.5 \text{ mA}} = 7 \text{ k}\Omega$$

E/A input bias current ($2 \mu\text{A}$ max) flows through R_i , resulting in a DC error in output voltage (V_o) given by :

$$\Delta V_{o(\text{max})} = (2 \mu\text{A}) R_i$$

Figure 9 : UC3842 Error Amplifier.

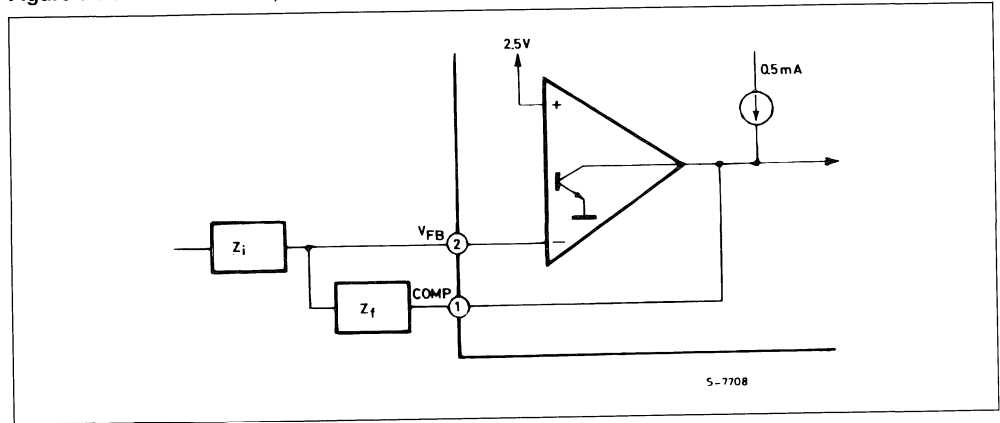
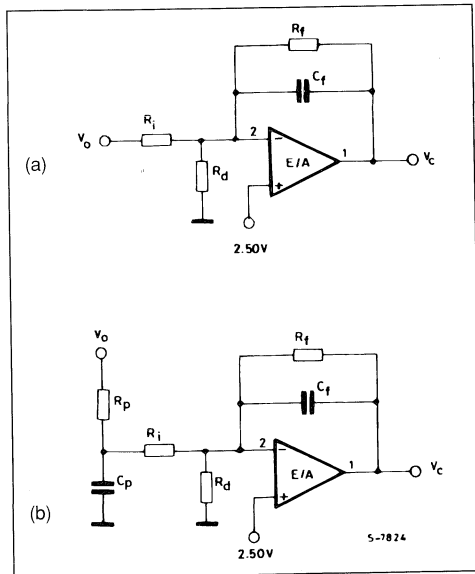


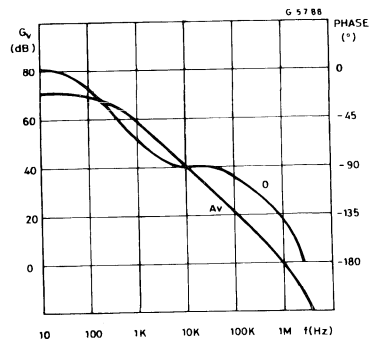
Figure 10 : (a) Error Amplifier Compensation Addition Pole and (b) Needed for Continuous Inductor-current Boost and Flyback.



It is therefore desirable to keep the value of R_i as low as possible.

Figure 11 shows the open-loop frequency response of the UC3842 E/A. The gain represent an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1 MHz due to second-order poles at $\sim 10 \text{ MHz}$ and above.

Figure 11 : Error Amplifier Open-loop Frequency Response.



CURRENT SENSING AND LIMITING

The UC3842 current sense input is configured as shown in figure 12. Current-to-voltage conversion is done externally with ground-referenced resistor R_S . Under normal operation the peak voltage across R_S is controlled by the E/A according to the following relation :

$$V_{RS}(\text{pk}) = \frac{V_C - 1.4 \text{ V}}{3}$$

where : V_C = control voltage = E/A output voltage.

R_S can be connected to the power circuit directly or through a current transformer, as figure 13 illustrates. While a direct connection is simpler, a transformer can reduce power dissipation in R_S , reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-reference sensing. The relation between V_C and peak current in the power stage is given by :

$$i(\text{pk}) = N \left(\frac{V_{RS}(\text{pk})}{R_S} \right) = \frac{N}{3 R_S} (V_C - 1.4)$$

where : N = current sense transformer turns ratio.
= 1 when transformer not used.

For purposes of small-signal analysis, the control-to-sensed-current gain is :

$$\frac{i(\text{pk})}{V_C} = \frac{N}{3 R_S}$$

When sensing current in series with the power transistor, as shown in figure 13, current waveform will often have a large spike at its leading edge. This is due to rectifier recovery and/or interwinding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC3842 current-sense comparator is internally clamped to 1 V (figure 12). Current limiting occurs if the voltage at pin 3 reaches this threshold value, i.e. the current limit is defined by :

$$i_{\text{MAX}} = \frac{N \cdot 1 \text{ V}}{R_S}$$

Figure 12 : Current Sensing.

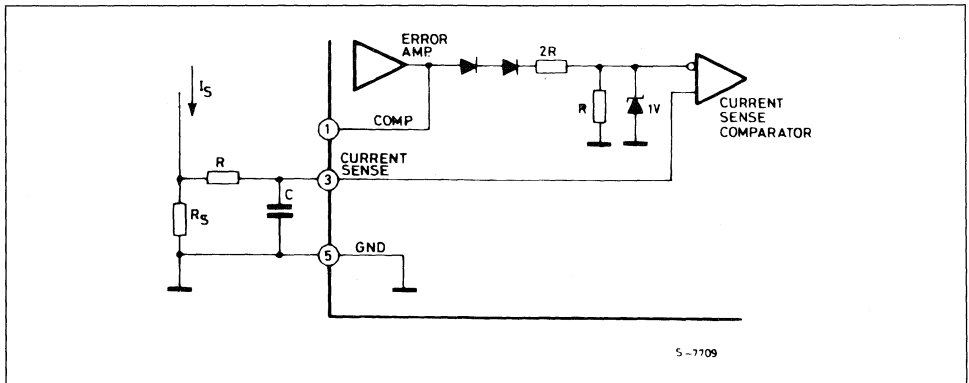
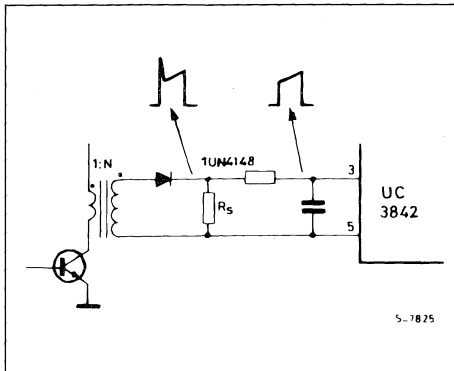


Figure 13 : Transformer-coupled Current Sensing.



TOTEM-POLE OUTPUT

The UC3842 has a single totem-pole output. The output transistors can be operated to ± 1 A peak current and ± 200 mA average current. The peak current is self-limiting, so no series current-limiting resistor is needed when driving a power MOS gate.

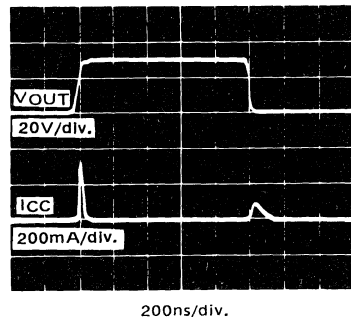
Cross-conduction between the output transistors is minimal, as figure 14 shows. The average added power due to cross-conduction with $V_i = 30$ V is only 80 mW at 200 kHz.

Figures 15-17 show suggested circuits for driving POWERMOS and bipolar transistors with the UC3842 output. The simple circuit of figure 15 can be used when the control IC is not electrically isolated from the power MOS. Series resistor R_1 provides damping for a parasitic tank circuit formed by the power MOS input capacitance and any series wiring inductance. Resistor R_2 shunts output leakage currents ($10 \mu\text{A}$ maximum) to ground when the under-voltage lockout is active. Figure 16 shows an isolated power MOS drive circuit which is appropriate when the drive signal must be levelshifted or transmitted across an isolation boundary. Bipolar transistors can be driven effectively with the circuit of figure 17. Resistors R_1 and R_2 fix the on-state base current. Capacitor C_1 provides a negative base current pulse to remove stored charge at turn-off.

PWM LATCH

This flip-flop, shown in figure 4, ensures that only a single pulse appears at the UC3842 output in any one oscillator period. Excessive power transistor dissipation and potential saturation of magnetic elements are thereby averted.

Figure 14 : Output Cross-conduction.



SHUTDOWN TECHNIQUES

Shutdown of the UC3842 can be accomplished by two methods ; either raise pin 3 above 1 V or pull pin 1 below 1 V. Either method causes the output of the PWM comparator to be high (refer to block diagram, figure 4). The PWM latch is reset dominant so that the output will remain low until the first clock pulse following removal of the shutdown signal at pin 1 or pin 3. As shown in figure 18, an externally latched shutdown can be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower under-voltage lockout threshold (10 V). At this point all internal bias is removed, allowing the SCR to reset.

Figure 15 : Direct POWERMOS Drive:

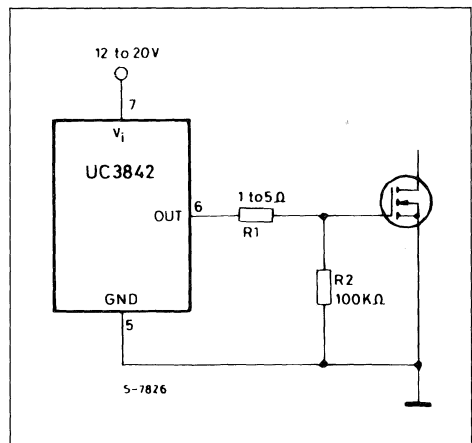


Figure 16 : Isolated POWERMOS Drive.

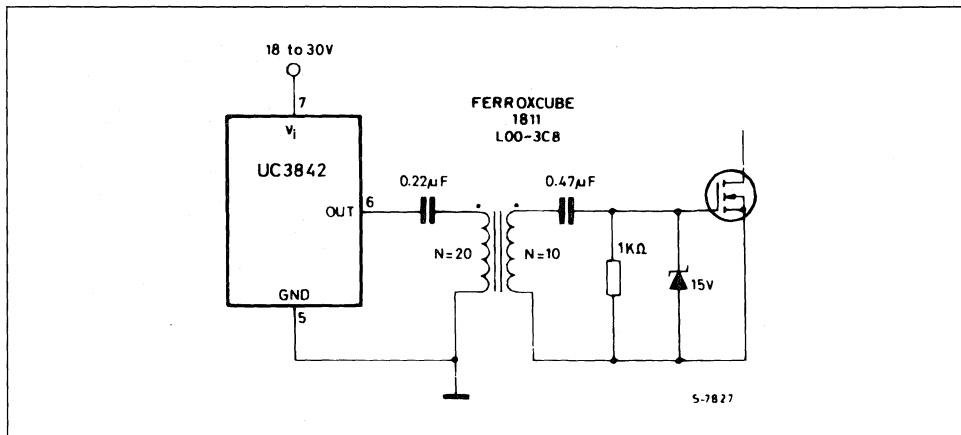
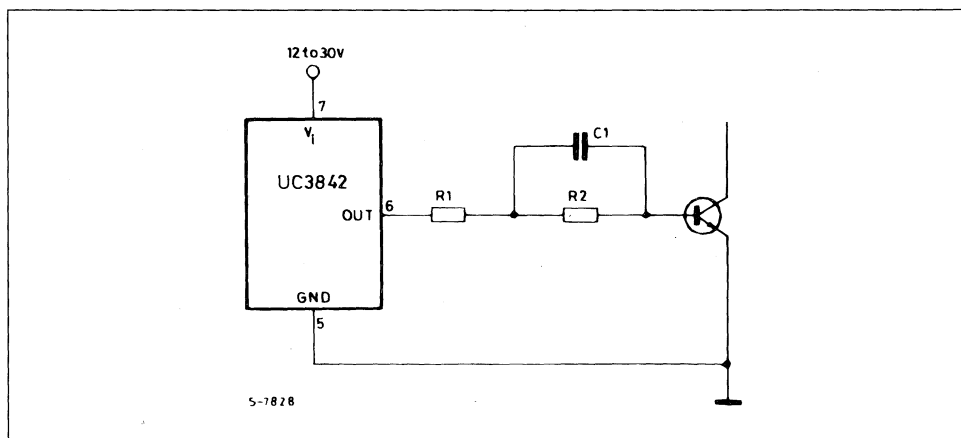


Figure 17 : Bipolar Drive with Negative Turn-off Bias.



AVOIDING COMMON PITFALLS

Current-mode controlled converters can exhibit performance peculiarities under certain operating conditions. This section explains these situations and how to correct them when using the UC3842.

SLOPE COMPENSATION PREVENTS INSTABILITIES

It is well documented that current-mode controlled converters can exhibit subharmonic oscillations when operated at duty cycles greater than 50 %.

Fortunately, a simple technique (usually requiring only a single resistor to implement) exists which corrects this problem and at the same time improves converter performance in other respects. This "slope compensation" technique is described in detail in Reference 6. It should be noted that "duty cycle" here refers to output pulse width divided by oscillator period, even in push-pull designs where the transformer period is twice that of the oscillator. Therefore, push-pull circuits will almost always require slope compensation to prevent subharmonic oscillation.

Figure 18 : Shutdown Achieved by
 (a) Pulling Pin 3 High
 (b) Pulling Pin 1 Low.

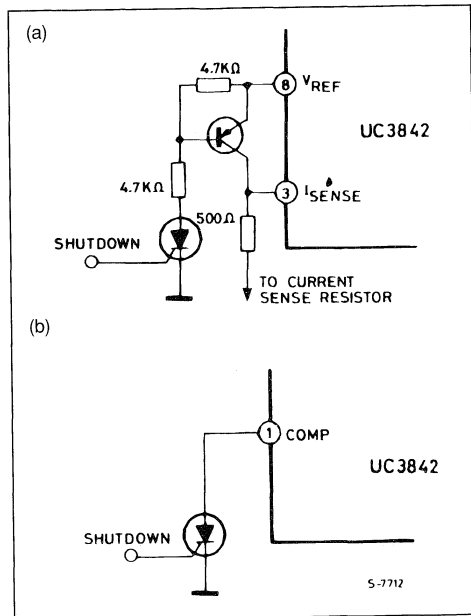


Figure 19 illustrates the slope compensation technique. In figure 19a the uncompensated control voltage and current sense waveforms are shown as a reference. Current is often sensed in series with the switching transistor for buck-derived topologies. In this case, the current sense signal does not track the decaying inductor current when the transistor is off, so dashed lines indicate this inductor current. The negative inductor current slope is fixed by the values of output voltage (V_o) and inductance (L) :

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{-V_F - V_o}{L} = \frac{-(V_F + V_o)}{L}$$

where : V_F = forward voltage drop across the freewheeling diode. The actual slope (m_2) of the dashed lines in figure 19a is given by :

$$m_2 = \frac{R_s}{N} \cdot \frac{di_L}{dt} = \frac{-R_s (V_F + V_o)}{NL}$$

where : R_s and N are defined as the "Current Sensing" section of this paper.

In figure 19b, a sawtooth voltage with slope m has been added to the control signal. The sawtooth is synchronized with the PWM clock, and practice is

most easily derived from the control chip oscillator as shown in figure 20a. The sawtooth slope in figure 19b is $m = m_2/2$. This particular slope value is significant in that it yields "perfect" current-mode control ; i.e. with $m_2/2$ the average inductor current follows the control signal so that, in the small-signal analysis, the inductor acts as a controlled current source. All current-mode controlled converters having continuous inductor current therefore benefit from this amount of slope compensation, whether or not they operate above 50 % duty.

More slope is needed to prevent subharmonic oscillations at high duty cycles. With slope $m = m_2$, such oscillations will not occur if the error amplifier gain ($A_{V(E/A)}$) at half the switching frequency ($f_s/2$) is kept below a threshold value (reference 6) :

$$A_{V(E/A)} \left| \begin{array}{l} m = m_2 \\ f = f_s/2 \end{array} \right. < \frac{\pi 2 C_o}{4 \tau}$$

where : C_o = sum of filter and load capacitance
 $\tau = 1/f_s$

Slope compensation can also improve the noise immunity of a current-mode controlled supply. When the inductor ripple current is small compared to the average current (as in figure 19a), a small amount of noise on the current sense or control signals can cause a large pulse-width jitter. The magnitude of this jitter varies inversely with the difference in slope of the two signals. By adding slope as in figure 19b, the jitter is reduced. In noisy environments it is sometimes necessary to add slope $m > m_2$ in order to correct this problem. However, as m increases beyond $m = m_2/2$, the circuit becomes less perfectly current controlled. A complex trade-off is then required ; for very noisy circuits the optimum amount of slope compensation is best found empirically.

Once the required slope is determined, the value of R_{SLOPE} in figure 20a can be calculated :

$$3 m = \frac{\Delta V_{RAMP}}{\Delta T_{RAMP}} \cdot A_{V(E/A)} = \frac{0.7 V}{T/2} \left(\frac{R_{SLOPE}}{Z_F | f_s} \right) = \frac{1.4}{\tau} \left(\frac{R_{SLOPE}}{Z_F | f_s} \right)$$

$$R_{SLOPE} = \frac{3 m \tau}{1.4} (Z_F | f_s) = 2.1 \cdot m \cdot \tau \cdot Z_F | f_s$$

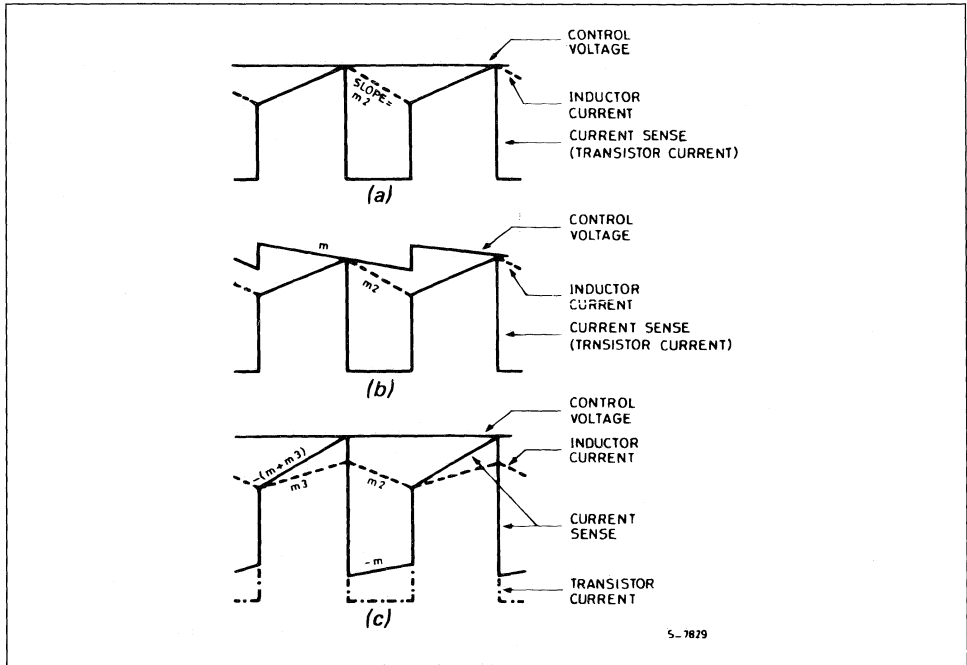
where : $Z_F | f_s$ is the E/A feedback impedance at the switching frequency.

For $m = m_L : \Delta T_{RAMP}$

$$R_{SLOPE} = 1.7 \tau \left(\frac{R_s (V_F + V_o)}{NL} \right) Z_F | f_s$$

Figure 19 : Slope Compensation Waveforms :

- (a) No Comp.
 (b) Comp. Added to Control Voltage.
 (c) Comp. Added to Current Sense.



S-7829

Note that in order for the error amplifier to accurately replicate the ramp, Z_F must be constant over the frequency range f_s to at least $3 f_s$.

In order to eliminate this last constraint, an alternative method of slope compensation is shown in figures 19c and 20b. Here the artificial slope is added to the current sense waveform rather than subtracted from the control signal. The magnitude of the added slope still relates to the downslope of inductor current as described above. The requirement for R_{SLOPE} is now :

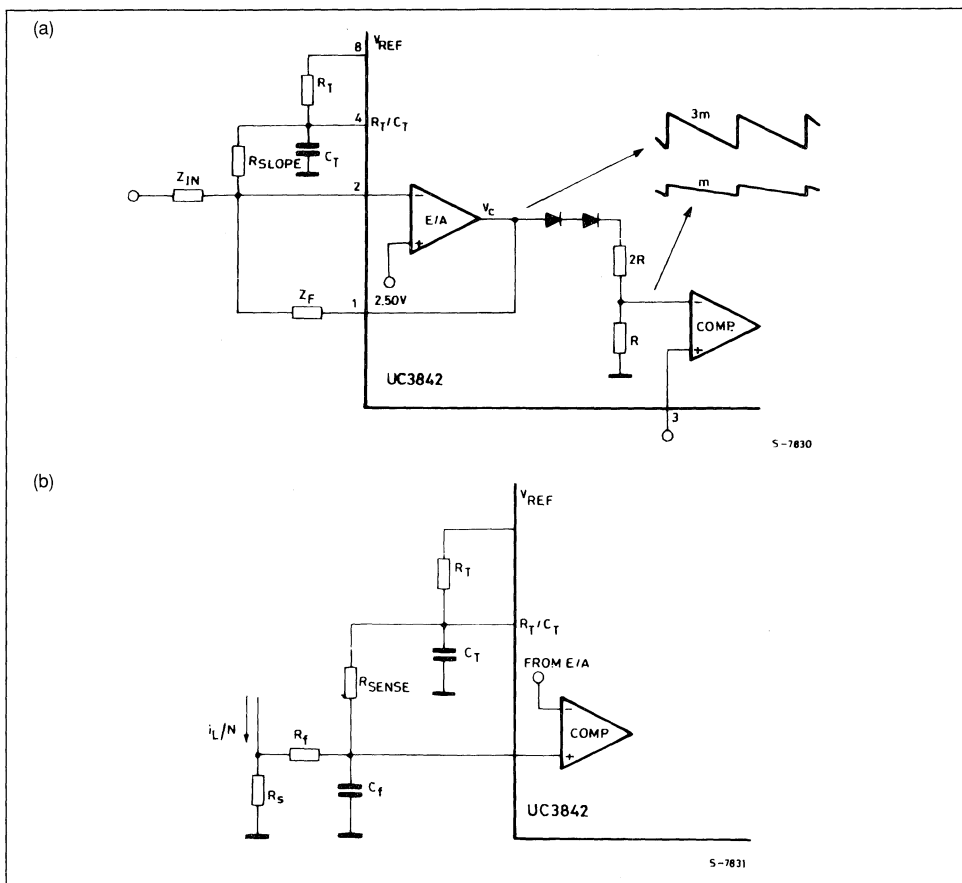
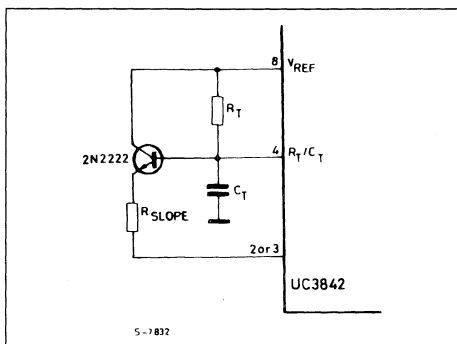
$$m = \frac{\Delta V_{RAMP}}{\Delta t_{RAMP}} \left(\frac{R_f}{R_f + R_{SLOPE}} \right) = \frac{0.7}{\tau/2} \left(\frac{R_f}{R_f + R_{SLOPE}} \right)$$

$$R_{SLOPE} = \frac{1.4 R_f}{m\tau} - R_f = R_f \left(\frac{1.4}{m\tau} - 1 \right)$$

For $m = m_2$:

$$R_{SLOPE} = R_f \left(\frac{1.4 NL}{R_s (V_F + V_O) \tau} - 1 \right)$$

R_{SLOPE} loads the UC3842 R_T/C_T terminal so as to cause a decrease in oscillator frequency. If $R_{SLOPE} \gg R_T$ then the frequency can be corrected by decreasing R_T slightly. However, with $R_{SLOPE} \leq 5 R_T$ the linearity of the ramp degrades noticeably, causing over-compensation of the supply at low duty cycles. This can be avoided by driving R_{SLOPE} with an emitter-follower as shown in figure 21.

Figure 20 : Slope Compensation Added (a) to Control Signal or (b) to Current Sense Waveform.**Figure 21 :** Emitter-follower Minimizes Load at R_T/C_T Terminal.

NOISE

As mentioned earlier, noise on the current sense or control signals can cause significant pulse-width jitter, particularly with continuous-inductor-current designs. While slope compensation helps alleviate this problem, a better solution is to minimize the amount of noise. In general, noise immunity improves as impedance decrease at critical points in a circuit.

One such point for a switching supply is the ground line. Small wiring inductances between various ground points on a PC board can support common-mode noise with sufficient amplitude to interfere with correct operation of the modulating IC. A copper ground plane and separate return lines for high-current paths greatly reduce common-mode noise.

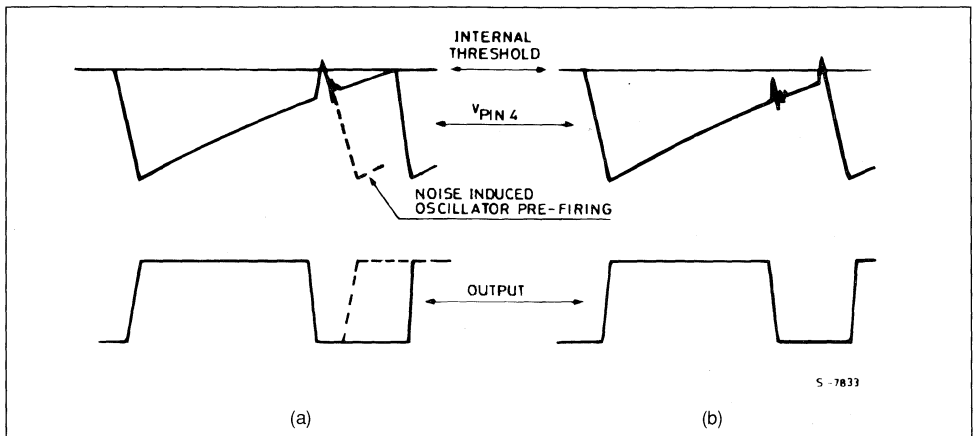
Note that the UC3842 has a single ground pin. High sink currents in the output therefore cannot be returned separately.

Ceramic bypass capacitors ($0.1\ \mu\text{F}$) from V_I and V_{REF} to ground will provide low-impedance paths for high frequency transients at those points. The input to the error amplifier, however, is a high-impedance point which cannot be bypassed without affecting the dynamic response of the power supply. Therefore, care should be taken to lay out the board in such a way that the feedback path is far removed from noise generating components such as the power transistor(s).

Figure 22a illustrates another common noise-induced problem. When the power transistor turns off, a noise spike is coupled to the oscillator R_T/C_T terminal. At high duty cycles the voltage at R_T/C_T is approaching its threshold level ($\sim 2.7\ \text{V}$, established by

the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude will prematurely trip the oscillator as shown by the dashed lines. In order to minimize the noise spike, choose C_T as large as possible, remembering that deadtime increases with C_T . It is recommended that C_T never be less than $\sim 1000\ \text{pF}$. Often the noise which causes this problem is caused by the output (pin 6) being pulled below ground at turn-off by external parasitics. This is particularly true when driving POWERMOS. A diode clamp from ground to pin 6 will prevent such output noise from feeding to the oscillator. If these measures fail to correct the problem, the oscillator frequency can always be stabilized with an external clock. Using the circuit of figure 8 results in an R_T/C_T waveform like that of figure 22b. Here the oscillator is much more immune to noise because the ramp voltage never closely approaches the internal threshold.

Figure 22 : (a) Noise on Pin 4 Can Cause Oscillator to Pre-trigger.
(b) With External Sync. Noise Does not Approach threshold Level.



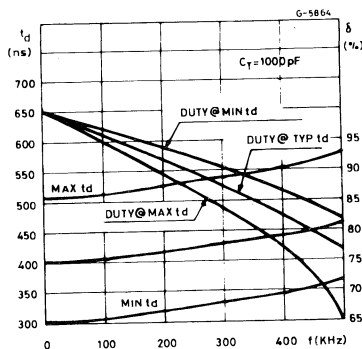
MAXIMUM OPERATING FREQUENCY

Since output deadtime varies directly with C_T , the restraint on minimum C_T ($1000\ \text{pF}$) mentioned above results in a minimum deadtime varies for the UC3842. This minimum deadtime varies with R_T and therefore with frequency, as shown in figure 23. Above $100\ \text{kHz}$, the deadtime significantly reduces the maximum duty cycle obtainable at the UC3842 output (also show in figure 23). Circuits not requiring large duty cycles, such as the forward converter and flyback topologies, could operate as high as $500\ \text{kHz}$. Operation at higher frequencies is not recom-

mended because the deadtime become less predictable.

The speed of the UC3842 current sense section poses an additional constraint on maximum operating frequency. A maximum current sense delay of $400\ \text{ns}$ represents $10\ \%$ of the switching period at $250\ \text{kHz}$ and $20\ \%$ at $500\ \text{kHz}$. Magnetic components must not saturate as the current continues to rise during this delay period, and power semiconductors must be chosen to handle the resulting peak currents. In short, above $\sim 250\ \text{kHz}$, many of the advantages of higher-frequency operation are lost.

Figure 23 : Deadtime and Maximum Obtainable Duty-cycle vs. Frequency with Minimum Recommended C_T .



CIRCUIT EXAMPLES

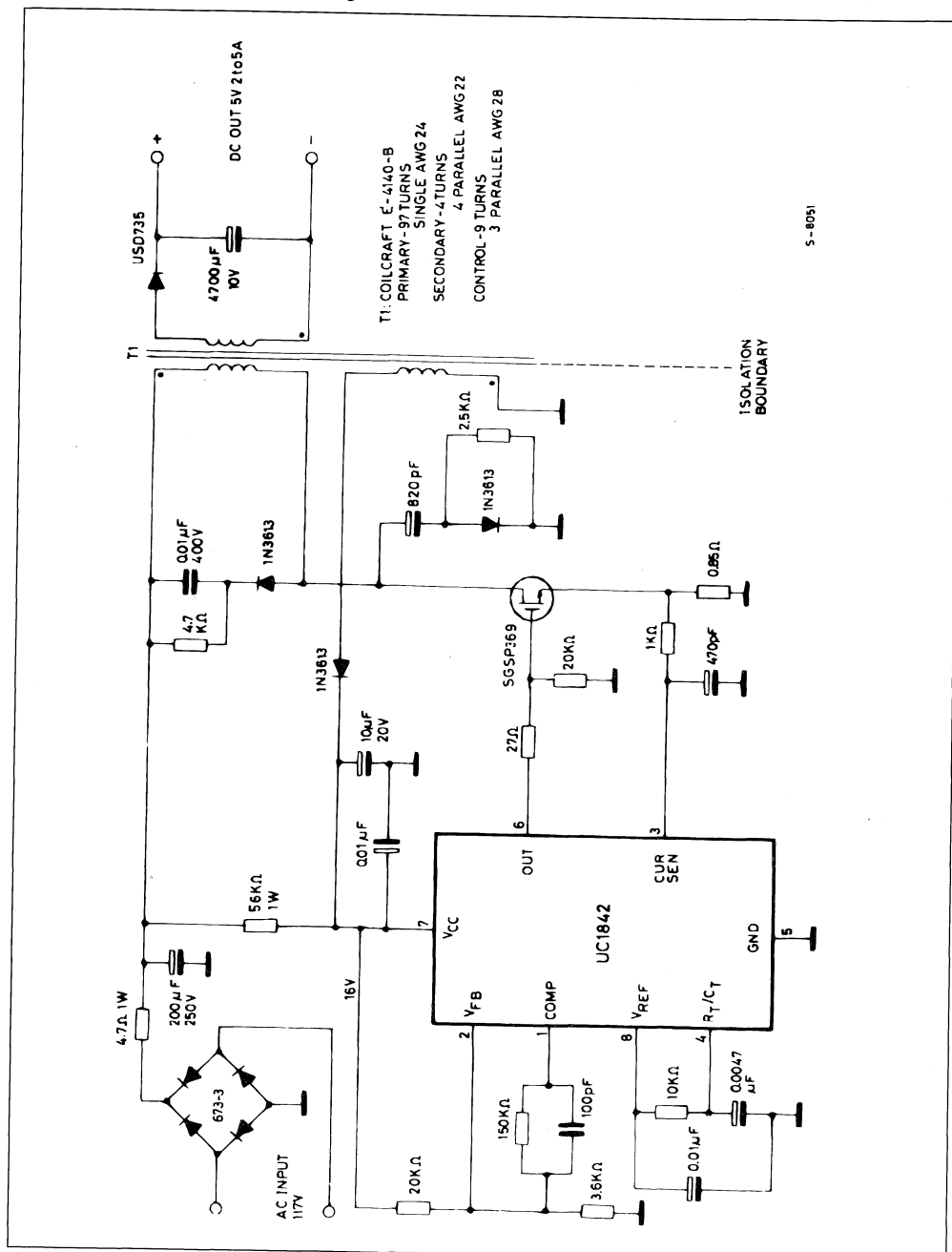
1. OFF-LINE FLYBACK

Figure 24 shows a 25 W multiple-output off-line fly-back regulator controlled with the UC3842. This regulator is low in cost because it uses only two magnetic elements, a primary-side voltage sensing technique, and an inexpensive control circuit. Specifications are listed below.

SPECIFICATIONS :

Line Isolation :	3750 V
Switching Frequency :	40 kHz
Efficiency @ full load :	70 %
Input Voltage	95 VAC to 130 VAC (50Hz/60Hz)
Output Voltage :	A. + 5 V, 5 % : 1 A to 4 A load Ripple voltage : 50 mV P-P Max.
	B. + 12 V, 3 % : 0.1 A to 0.3 A load Ripple voltage : 100 mV P-P Max
	C. - 12 V, 3 % 0.1 A to 0.3 A load Ripple voltage : 100 mV P-P Max

Figure 24 : 25W off-line Flyback Regulator.



A 25W OFF-LINE FLYBACK SWITCHING REGULATOR

INTRODUCTION

This note describes a low cost switching power supply for applications requiring multiple output voltages, e.g. personal computers, instruments, etc... The discontinuous mode flyback regulator used in this application provides good voltage tracking between outputs, which allows the use of primary side voltage sensing. This sensing technique reduces costs by eliminating the need for an isolated secondary feedback loop.

The low cost, (8 pin) UC1842 current mode control chip employed in this power supply provides performance advantages such as :

- 1) Fast transient response
- 2) Pulse by pulse current limiting
- 3) Stable operation

To simplify drive circuit requirements, a TO-220 power MOS SGSP369 is utilized for the power switch. This switch is driven directly from the output of the control chip.

POWER SUPPLY SPECIFICATIONS

1. Input voltage : 95VAC to 130VAC (50 Hz/60 Hz)
2. Output voltage :
 - A. + 5 V, $\pm 5\%$: 1 A to 4 A load
Ripple voltage : 50 mV P-P Max
 - B. + 12 V, $\pm 3\%$: 0.1 A to 0.3 A load
Ripple voltage : 100 mV P-P Max
 - C. - 12 V, $\pm 3\%$: 0.1 A to 0.3 A load
Ripple voltage : 100 mV P-P Max
3. Line Isolation : 3750 V
4. Switching Frequency : 40 KHz
5. Efficiency @ Full Load : 70 %

BASIC CIRCUIT OPERATION

The 117VAC input line voltage is rectified and smoothed to provide DC operating voltage for the circuit. When power is initially applied to the circuit, capacitor C2 charges through R2. When the voltage

across C2 reaches a level of 16 V the output of IC1 is enabled, turning on power MOS Q1.

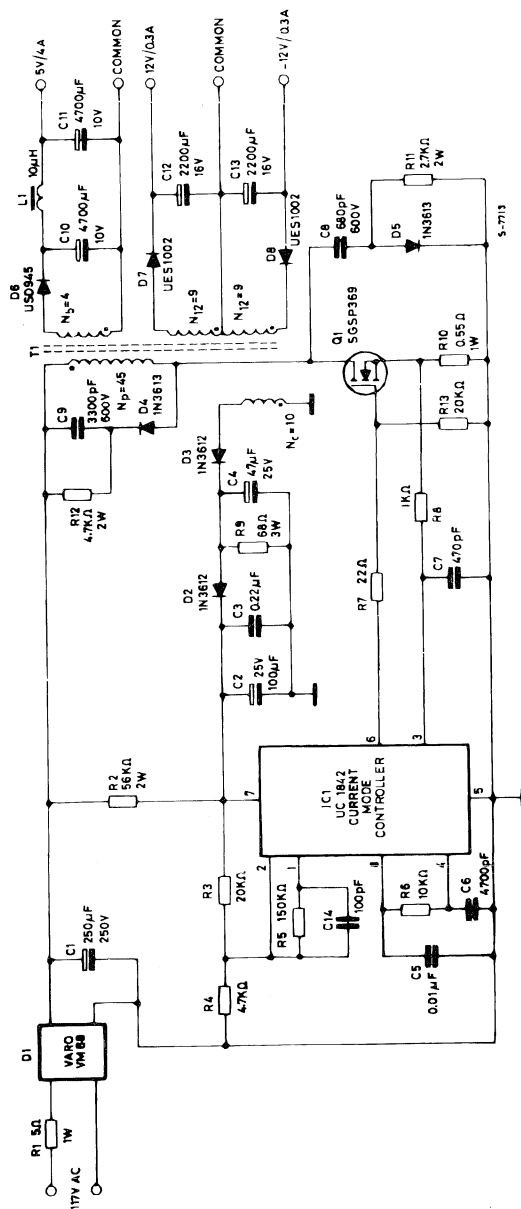
During the on time of Q1, energy is stored in the air gap of transformer (inductor) T1. At this time the polarity of the output windings is such that all output rectifiers are reverse biased and no energy is transferred. Primary current is sensed by a resistor, R10, and compared to a fixed 1 V reference inside IC1. When this level is reached, Q1 is turned off and the polarity of all transformer windings reverses, forward biasing the output rectifiers. All the energy stored is now transferred to the output capacitors. Many cycles of this store/release action are needed to charge the outputs to their respective voltages. Note that C2 must have enough energy stored initially to keep the control circuitry operating until C4 is charged to a level of approximately 13 V. The voltage across C4 is fed through a voltage divider to the error amplifier (pin 2) and compared to an internal 2.5 V reference.

Energy stored in the leakage inductance of T1 causes a voltage spike which is added to the normal reset voltage across T1 when Q1 turns off. The clamp consisting of D4, C9 and R12 limits this voltage excursion from exceeding the BVDSS rating of Q1. In addition, a turn-off snubber made up of D5, C8 and R11 keeps power dissipation in Q1 low by delaying the voltage rise until drain current has decreased from its peak value. This snubber also damps out any ringing which may occur due to parasitics.

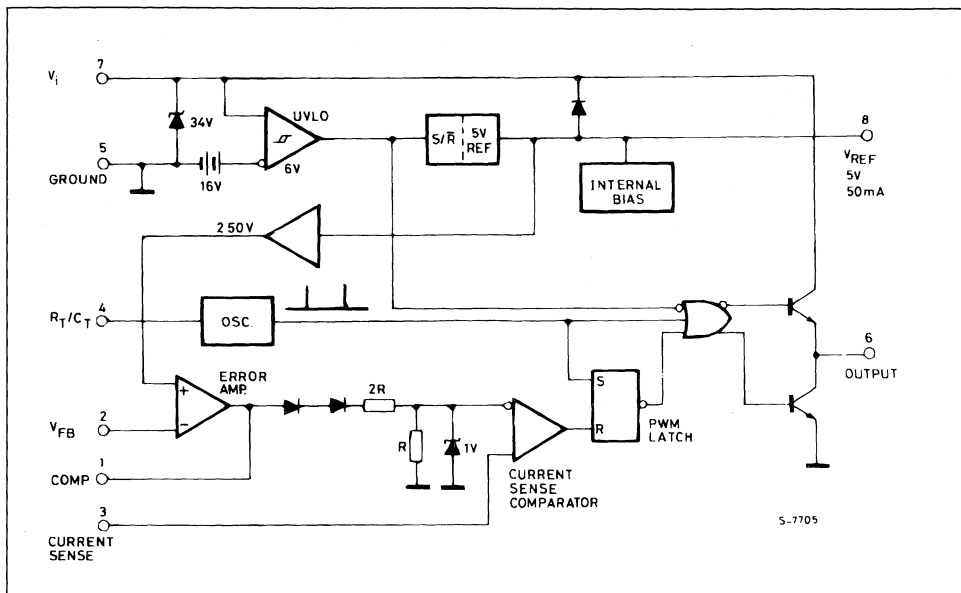
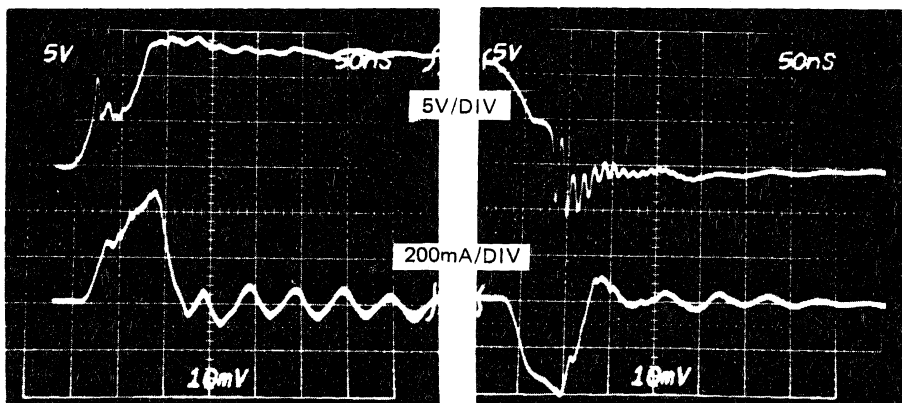
Less than 3.5 % line and load regulation is achieved by loading the output of the control winding Nc, with R9. This resistor dissipates the leakage energy associated with this winding. Note that R9 must be isolated from R2 with diode D2, otherwise C2 could not charge to the 16 V necessary for initial start-up.

A small filter inductor in the 5 V secondary is added to reduce output ripple voltage to less than 50 mV. This inductor also attenuates any high frequency noise.

Figure 1 : 25W Off-line Flyback Regulator.

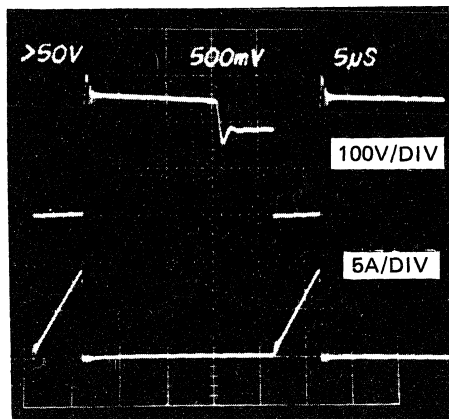


- Notes :** 1. All resistors are 1/4 W unless noted.
2. See appendix for construction details.
3. L1 = Ferroxcube 204T50-3C8 (Toroid), N° turns : 4, Wire Gauge : 1 mm. (18 AWG).

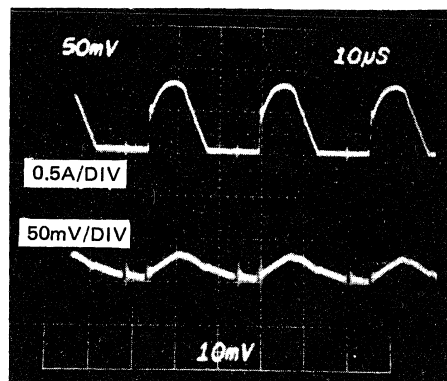
Figure 2 : Block Diagram : UC1842 Current Mode Controller.**TYPICAL SWITCHING WAVEFORMS**

Upper trace : Q1 - Gate to source voltage
 Lower trace : Q1 - Gate Current

TYPICAL SWITCHING WAVEFORMS



Upper trace : Q1 - Drain to source voltage
Lower trace : Primary current - I_D



Upper trace : +5V charging current
Lower trace : +5V output ripple voltage

PERFORMANCE DATA

Conditions		5 V out	12 V out	- 12 V out
Low Line (95 VAC)				
± 12 @ 100 mA	+ 5 V @ 1.0 A	5.211	12.05	- 12.01
	4.0 A	4.854	12.19	- 12.14
± 12 @ 300 mA	+ 5 V @ 1.0 A	5.199	11.73	- 11.69
	4.0 A	4.950	11.68	- 11.63
Nominal Line (120 VAC)				
± 12 @ 100 mA	+ 5 V @ 1.0 A	5.220	12.07	- 12.03
	4.0 A	4.875	12.23	- 12.18
± 12 @ 300 mA	+ 5 V @ 1.0 A	5.208	11.73	- 11.68
	4.0 A	4.906	11.67	- 11.62
High Line (130 VAC)				
± 12 @ 100 mA	+ 5 V @ 1.0 A	5.207	12.06	- 12.02
	4.0 A	4.855	12.21	- 12.15
± 12 V @ 300 mA	+ 5 V @ 1.0 A	5.200	11.71	- 11.67
	4.0 A	4.902	11.66	11.61
Overall Line and Load Regulation		± 3.5 %	± 2.3 %	± 2.4 %

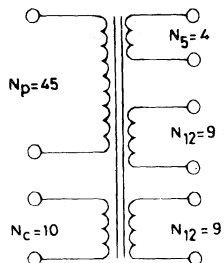
APPENDIX POWER TRANSFORMER - T1

Core : Ferroxcube EC-35/3C8

Gap : 0.25mm. in each outer leg

Note : For reduced EMI put gap in center leg only.

Use 0.5mm.



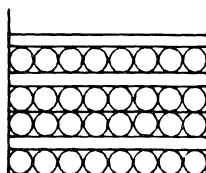
S - 7931

TRANSFORMER CONSTRUCTION

CONTROL WINDING
N=10, AWG 30 (0.25mm)
2 IN PARALLEL

+5V OUT, N=4, AWG 26 (0.4mm)
6 IN PARALLEL

2 LAYERS 3M MYLAR TAPE



BOBBIN - 35PCB1

2 LAYERS, 3M MYLAR TAPE

±12V WINDINGS N=9, AWG30 (0.25mm)
2 WIRES IN PARALLEL.
BIFILAR WOUND

PRIMARY N=45, AWG 26 (0.4mm)

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APPLYING THE UC1840 TO PROVIDE TOTAL CONTROL FOR LOW-COST, PRIMARY-REFERENCED SWITCHING POWER SYSTEMS

INTRODUCTION

There are many potential approaches to be considered in switch mode power supply design ; however, the contradictory requirements of minimum cost and compatibility with ever more demanding line isolation specifications make primary control very attractive. Application of the UC1840 as a primary-side, off-line controller presents an extremely cost-effective approach to supplying isolated power from a widely varying input line while maintaining a high degree of efficiency.

Primary control means referencing all of the control electronics along with the power switching device on the input line side of an isolation transformer. An obvious advantage to this approach is the simplified interface between the control and power switch. This eliminates many of the transitions across the isolation boundary which significantly increase the cost of the magnetics portion of the power supply's budget.

There are two disadvantages to primary control : (1) operating or at least starting, the control electronics from the line voltage (typically 300 VDC), and (2) providing adequate regulation (which requires feedback from the secondary across the isolation boundary). The capability of the UC1840 Control IC to solve these problems while providing all of the regulating, sequencing, monitoring, and protection functions referenced to the primary side, makes this device very attractive.

THE UC1840 CONTROLLER

The overall block diagram of the UC1840, shown in figure 1, includes the following features :

- (1) Fixed-frequency operation set by user-selected components.
- (2) A variable-slope ramp generator for constant volt-second operation providing open-loop line regulation and minimizing, or in some cases even eliminating, the need for feedback control.
- (3) A drive switch for low current start-up off the high-voltage line.
- (4) A precision reference generator with internal over-voltage protection.
- (5) Complete under-voltage, over-voltage, and over-current protection including programmable shut-down and restart.
- (6) A high-current, single-ended PWM output optimized for fast turn-off of an external power switch.
- (7) Logic control for pulse-commandable or DC power sequencing.

For an understanding of how these individual blocks work together in a typical, medium-power flyback power supply, reference should be made to figure 2 and the functional description which follows.

Figure 1 : The Overall Block Diagram of the UC1840, an Integrated Circuit Optimized for Primary-side Control of Off-line Switching Power Supplies.

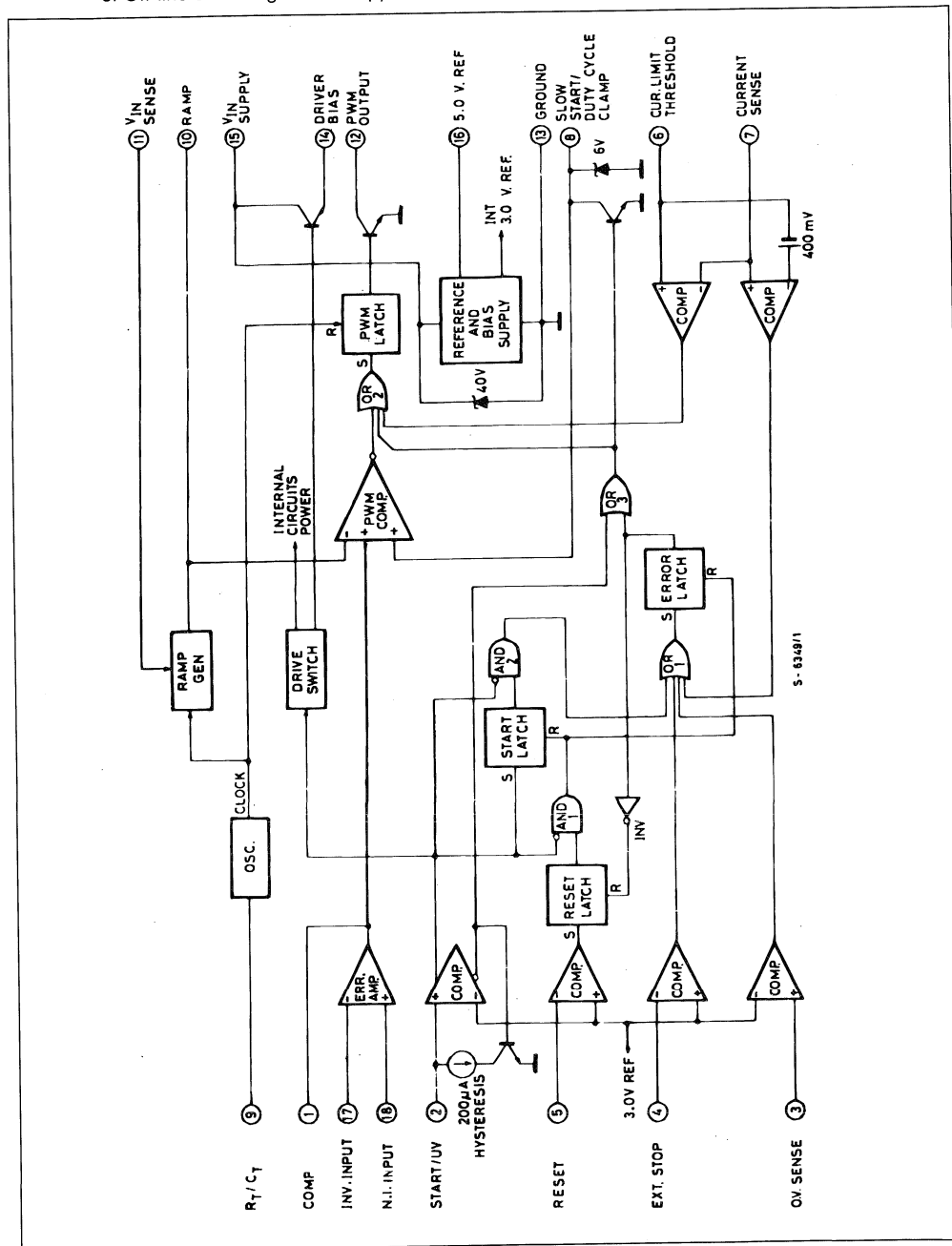


Figure 2 : A fully protected, isolated flyback power supply can be implemented with the UC1840, a high-voltage power switch, the transformer, and a small handful of passive components.

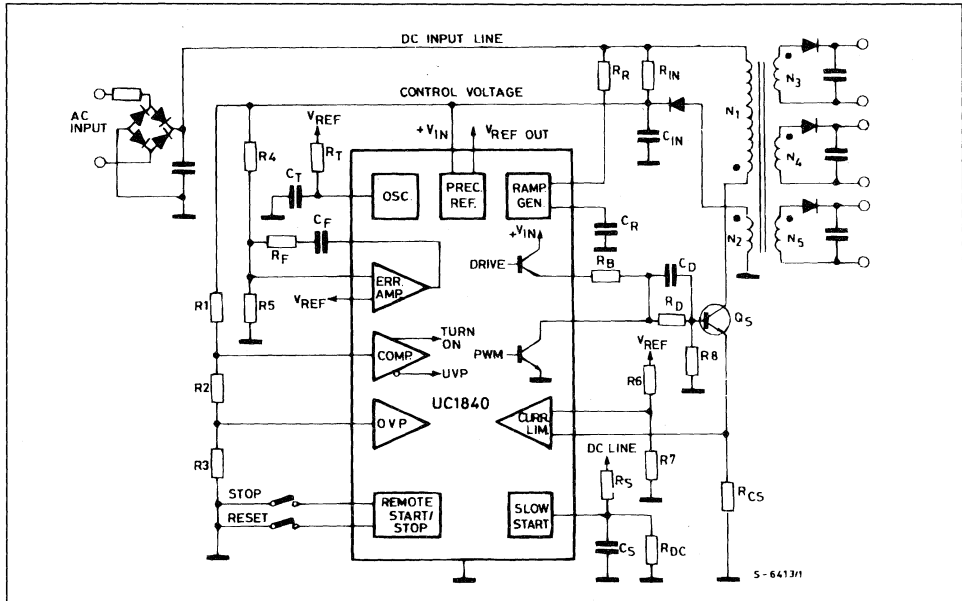
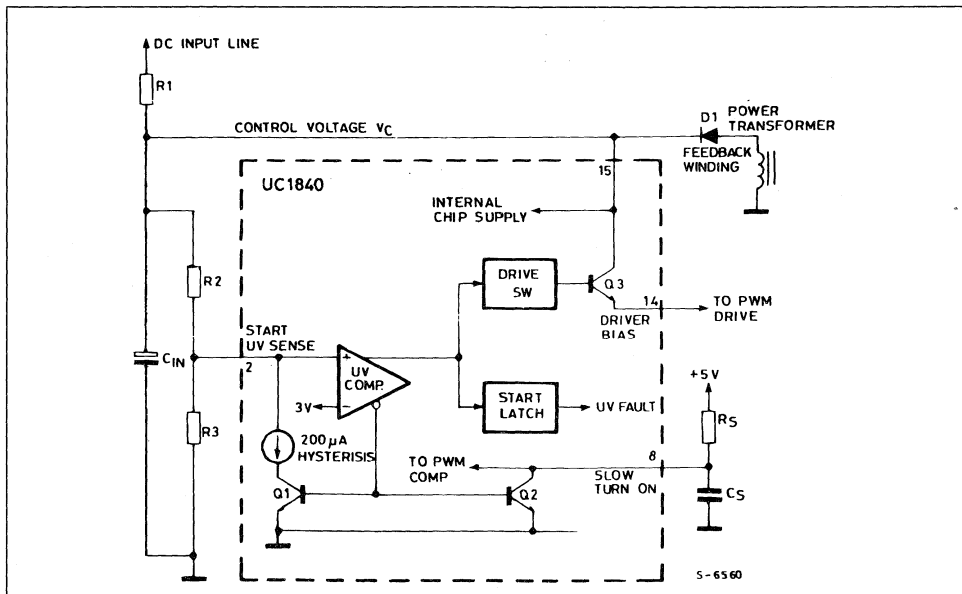


Figure 3 : The UC1840's start circuitry requires low starting current from the DC input line with normal operating current supplied from a low-voltage feedback winding on the power transformer.



UC1840 FUNCTIONAL DESCRIPTION

POWER SEQUENCING

A simplified schematic of the UC1840's internal power turn-on circuitry is shown in figure 3. The key elements of this function are : (1) the Driver Bias Switch, Q3, which keeps the loading on the control voltage, V_C , to a minimum during start up ; (2) the Under-voltage Comparator which also functions as a Start Threshold Detector with programmable hysteresis ; and (3) an auxiliary, primary-referenced, low-voltage winding on the main power transformer which provides normal control power after turn-on. The sequence of events is as follows :

- (1) While the control voltage, V_C , is low enough so that the voltage on pin 2 is less than 3 V, the Start/UV Comparator does the following :
 - (a) A 200 μ A hysteresis current is flowing into pin 2 through Q1 causing an added drop across R2.
 - (b) The drive switch is holding the Driver Bias transistor, Q3, OFF. This insures that the only current required through R1 is the start-up current of the UC1840, plus external dividers (R2, R3, R_S , etc.).
 - (c) The Slow Turn-on transistor, Q2, is ON, holding pin 8 and C_S low.
 - (d) The Start Latch keeps the under-voltage signal from being defined as a fault.

- (2) The start level is defined by :

$$V_C(\text{start}) = 3 \left(\frac{R_2 + R_3}{R_3} \right) + 0.2 R_2.$$

When V_C rises to this level, the Start/UV.

Comparator then does the following :

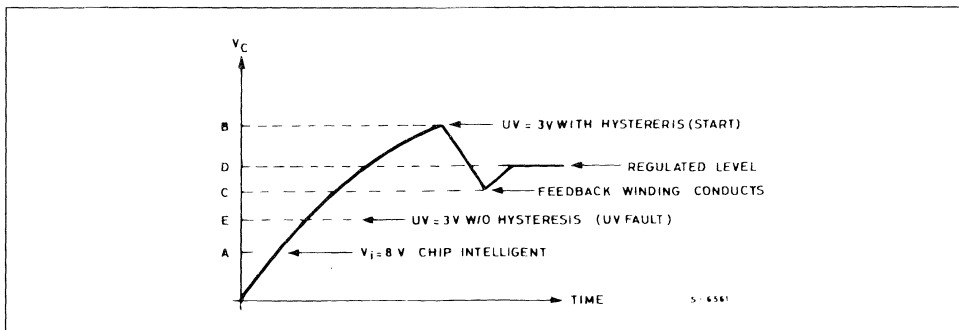
- (a) Turns off Q1, eliminating the 200 μ A hysteresis current. This allows the voltage on V_C to drop before reaching the under-voltage fault level defined by :

$$V_C(\text{U.V. fault}) = 3 \left(\frac{R_2 + R_3}{R_3} \right)$$
- (b) Sets the Start Latch to monitor for an under-voltage fault.
- (c) Activates Q3 providing Driver Bias to the power switch, pulling the added current out of C_{IN} .
- (d) Turns off Q2 allowing for programmed slow turn-on defined by R_S and C_S .
- (3) A normal start-up occurs with the control voltage, V_C , following the path shown in figure 4. If the power supply does not start, V_C will fall to an under-voltage fault which will then either initiate a restart attempt or hold the power switch off, depending upon the status of the Reset terminal as defined under Fault Sequencing. If start-up does not occur because of some fault in the Driver Bias line, V_C will continue to rise until the 40 V zener across the reference circuit conducts. This will then clamp V_C to that level, protecting the control chip.

After start-up occurs, current will continue to flow in R1 providing a power loss of :

$$P_d = \frac{(V_{line} - V_C)^2}{R_1}$$

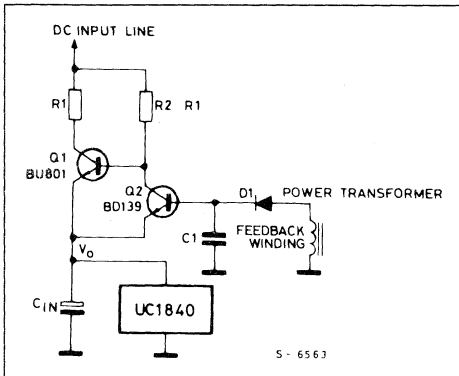
Figure 4 : Under a normal turn-on, the supply voltage to the UC1840, would rise lightly loaded to the start level, fall under the turn-on load, and then regulate at some intermediate level.



If this loss is objectionable, it can be reduced more than an order of magnitude by the addition of a two-transistor switch shown in figure 5. In this circuit, Q1 is initially driven on by current through R2. When the

feedback winding starts to conduct through D1 however, Q2 turns on leaving only R2 conducting from the input line.

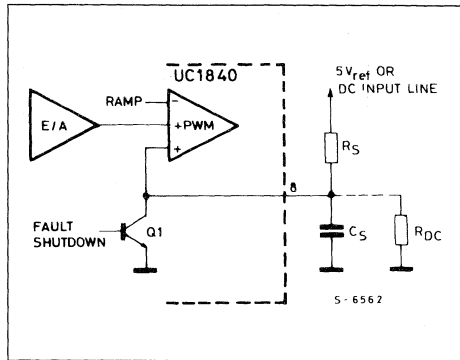
Figure 5 : The addition of Q1 and Q2 can eliminate the steady-state current through R1 after turn-on. Q2 is selected to pass all control current through its base-emitter junction.



SLOW TURN-ON CIRCUIT

The PWM comparator input connected to pin 8 accommodates several programming functions, shown in figure 6. Since this comparator will only follow the lowest positive input, holding pin 8 low will effectively eliminate a PWM signal, regardless of the status of the Error Amplifier output. Prior to turn-on, and at all times when a fault has been sensed, Q1 is ON, holding pin 8 low.

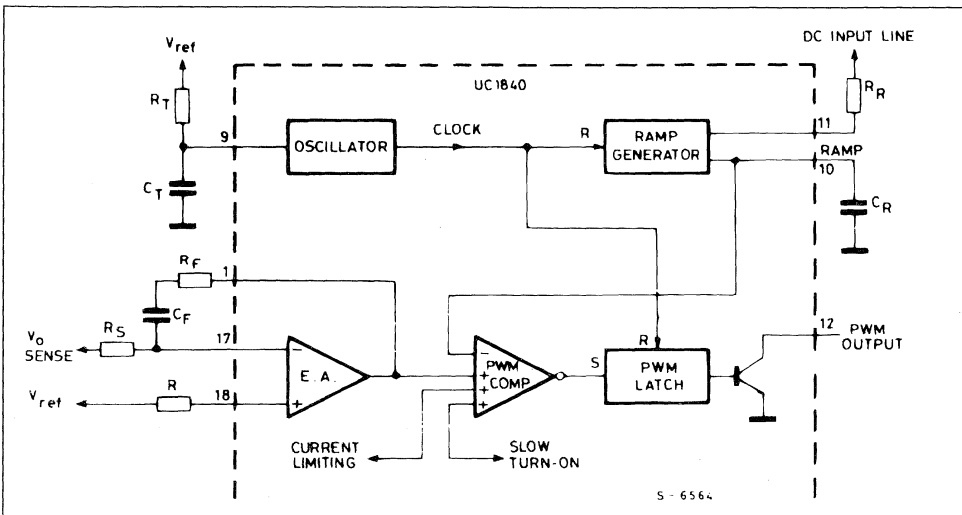
Figure 6 : Pin 8 on the UC1840 can be used for both slow turn-on and duty-cycle limiting as well as a PWM shutdown port.



When Q1 turns off, allowing pin 8 to rise with a controlled rate will cause the output pulses to increase from zero to nominal widths at the same rate. This is accomplished by the addition of C_S and a charging source, such as R_S , to the 5 V reference.

Note that where starting energy is stored in an input capacitor, the time for PWM turn-on must be less than the time required for the added Driver Bias load current to discharge the input capacitor to the under voltage fault level. In other words, referring back to figure 4, the slow turn-on must be faster than the time required for V_C to fall from level B to level E.

Figure 7 : The pulse-width modulator within the UC1840 separates the ramp function from the fixed-frequency oscillator.



Another function of pin 8 is to establish a maximum duty cycle limit. This is achieved by clamping the voltage on pin 8 with a divider formed by adding R_{DC} to ground. If R_S is taken to the 5 V reference, the clamp voltage will be fixed, which is desirable if the ramp slope is also fixed. If the ramp slope is varied with the input line - for constant volt-second operation - then the clamp voltage on pin 8 must also vary. This is readily accomplished by connecting R_S to the DC input line. The divider voltage :

$$V_{Pin\ 8} = \left(\frac{R_{DC}}{R_S + R_{DC}} \right) V\ DC\ input$$

should be equal to the ramp voltage level that yields the desired maximum duty cycle, at the same DC input level.

PWM CONTROL

Pulse-Width Modulation within the UC1840 consists of the blocks shown in figure 7. This architecture, with the possible exception of the separation between the time-base and ramp functions, is fairly conventional. It is described in greater detail in the paragraphs which follow.

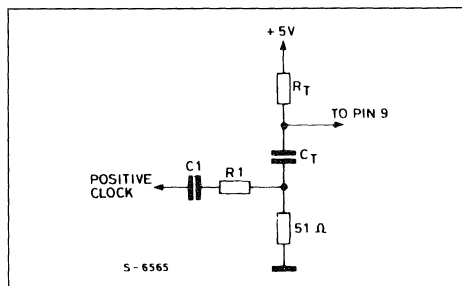
OSCILLATOR

A constant clock frequency is established by connecting R_T from pin 9 to the 5 V reference and C_T from pin 9 to ground. The frequency is approximated by :

$$f \approx \frac{1}{R_T C_T}$$

where the value of R_T can range from 1 k Ω to 100 K Ω and C_T from 300 pF to 0.1 μ F. The best temperature coefficients occur with C_T in the range of 1000 to 3000 pF. Although the clock output pulse is not available external to the UC1840, synchronization to an external clock can still be accomplished with the circuit of figure 8, where R_1 and C_1 are selected to provide a 0.5 V, 200 ns pulse across the 51 Ω resistor, and R_T and C_T define a frequency slightly lower than the synchronizing source.

Figure 8 : Synchronization to an external time base can be accomplished by adding a 51 Ω resistor in series with C_T .

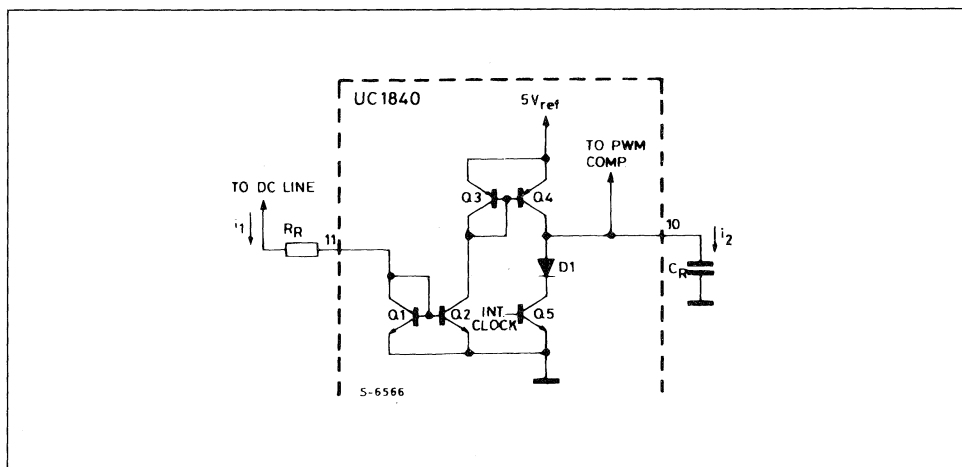


To achieve minimum start-up current, the oscillator is not activated until the input voltage is high enough to give a start command to the drive switch.

RAMP GENERATOR

The ramp generator function of the the UC1840 is shown in simplified form in figure 9.

Figure 9 : Current mirrors Q1-Q4 are used to make the ramp charging current i_2 , linearly proportional to the DC input line.



The NPN and PNP current mirrors provide a charging current to C_R of :

$$i_2 = i_1 = \frac{V_{line} - 0.7 \text{ V}}{R_R} \cong \frac{V_{line}}{R_R}$$

The current mirrors are useful over a current range of 1 μA to 1 mA, but optimum tracking occurs between 30 μA and 300 μA . Since the voltage across $Q1$ is very small, i_2 accurately represents the input line voltage. The ramp slope, therefore, is :

$$\frac{dv}{dt} = \frac{V_{line}}{R_R C_R}$$

The peak voltage across C_R is clamped to approximately 4.2 V while the valley, or low voltage, is determined by the on-voltage of the discharge network, D1 and Q5. This is typically 0.7 V.

If line sensing is not required, R_R should be connected to the 5 V reference for constant ramp slope.

ERROR AMPLIFIER

This is a voltage-mode operational amplifier with an uncommitted NPN differential input stage and an output configuration as shown in figure 10.

The 1 K Ω output resistor, R_o , is used both for short circuit protection and to limit the peak output voltage to less than 4.0 V so it cannot rise above the clamped ramp waveform. At sink currents less than 300 μA , the low output level will be within 200 mV of ground but it rises to 1 V at higher current levels.

The input common mode range is from 1 V to within 2 V of the input supply voltage. V_{in} , and thus either input can be connected directly to the 5 V reference.

Figure 10 : The output of the error amplifier operates class A to 300 μA , but can source and sink more than 1 mA for fast response.

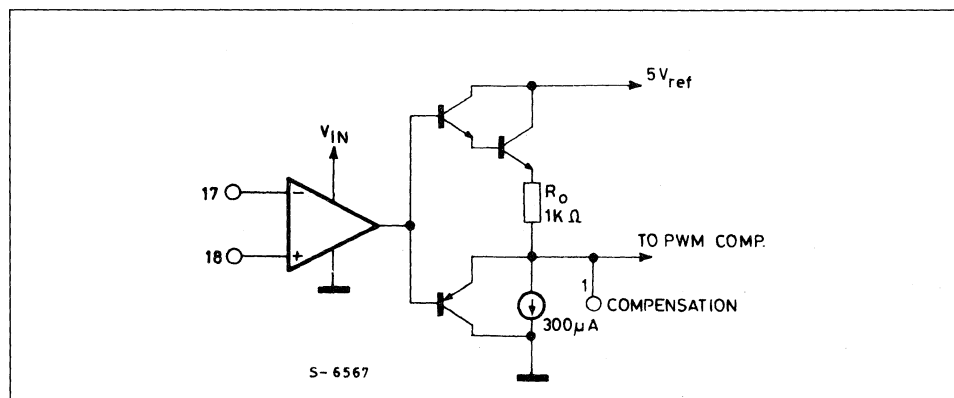
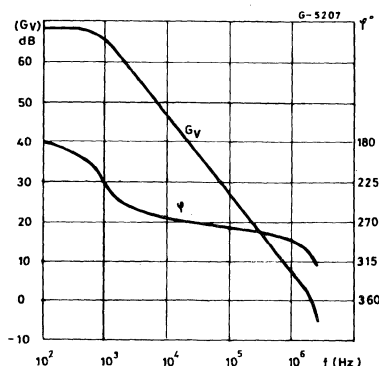


Figure 11 : The UC1840 error amplifier has a DC gain of 67 dB, a 2 MHz bandwidth, and phase margin of approximately 45°.



APPLICATION NOTE

The small signal, open-loop gain characteristics are shown in figure 11. The amplifier is unity-gain stable and has a maximum slew rate of just under 1 V/ μ s.

PWM COMPARATOR AND LATCH

This comparator (see figure 7) generates the output pulse which starts at the termination of the clock pulse and ends when the ramp waveform crosses the lowest of the three positive inputs. The clock forms a blanking pulse which keeps the maximum duty cycle less than 100 %. The PWM latch insures there will be only one pulse per period and eliminates oscillation at comparator cross-over.

PWM OUTPUT STAGE

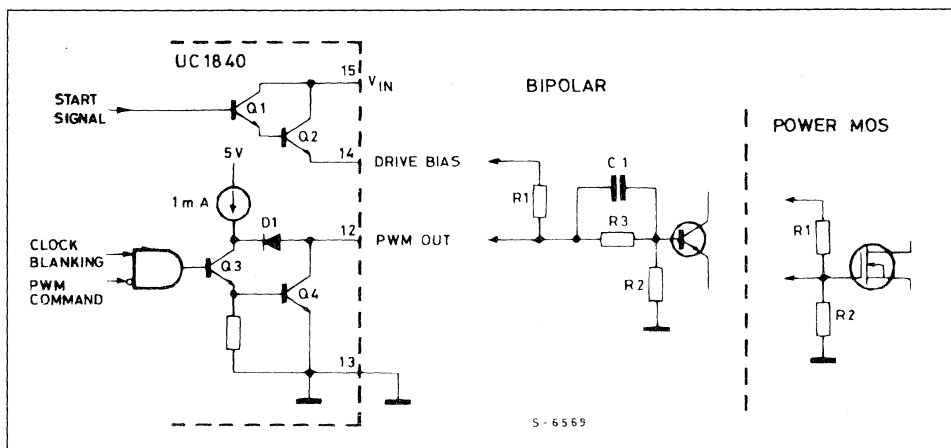
In addition to the PWM output signal on pin 12, the UC1840 also includes an output gating, or arming

function as Driver Bias on pin 14. Both functions should be considered together in interfacing to the external high-voltage power switch. These are illustrated in simplified form in figure 12.

At very low input voltages ($V_{IN} < 3$ V), both Q2 and Q4 are OFF. This may necessitate the use of R2, but its value can be high since it does not have to turn the output switch off. It merely holds it in the off state during the early portion of start-up.

Between $V_{IN} = 3$ V and the start threshold (pin 2 = 3 V with hysteresis on), Q2 is OFF and Q4 is ON, clamping the power switch off with a low impedance. A start command (UV high) turns on Q2, applying ($V_{IN} - 2$ V) to R1. This provides a source for power switch activation; however, since Q4 is still conducting, the current through R1 is shunted to ground and the power switch remains held off.

Figure 12 : Interfacing the UC1840 PWM output stage to either Bipolar or Power MOS switches.

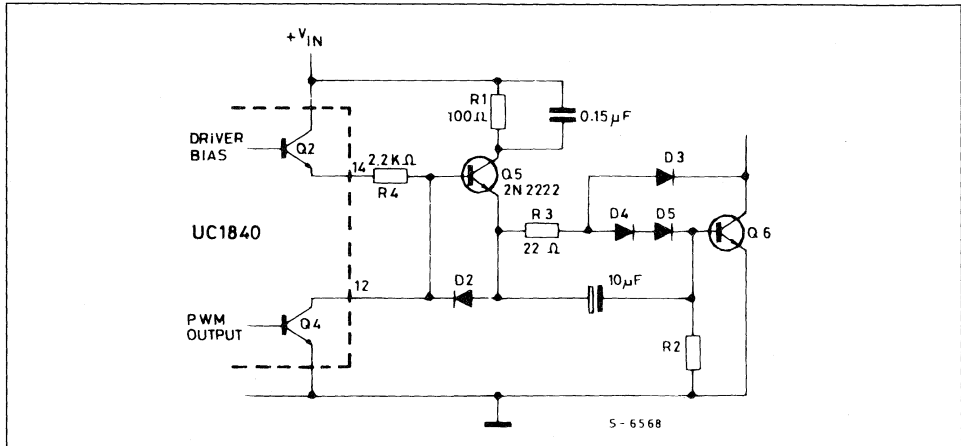


At the same time Q2 turns on, the clamping transistor at the slow-start terminal, pin 8, turns off allowing the voltage on pin 8 to rise according to the external slow-start time constant described earlier. This allows PWM pulses to begin to activate Q4 - narrow at first and widening to the point where the error amplifier takes command.

The interface between the UC1840 and the primary power switch may be implemented in several different ways to meet varying system requirements. One obvious application is when the use of a bipolar tran-

sistor switch requires more drive current than the Driver Bias output can provide. Figure 13 shows a more typical bipolar drive scheme where Q5 has been added to boost the turn-on current with the UC1840 still providing the high speed turn-off. The circuit now serves as a more efficient "totem-pole" driver since Q5 turns off when Q4 conducts. It also illustrates the use of a Baker Clamp to minimize storage time in Q6 and the capacitors for rapid turn-on and high-current pulse turn-off.

Figure 13 : Adding Q5 as a switched, drive-boost transistor provides added base drive for Q6 while reducing the steady-state current through both Q2 and Q4.



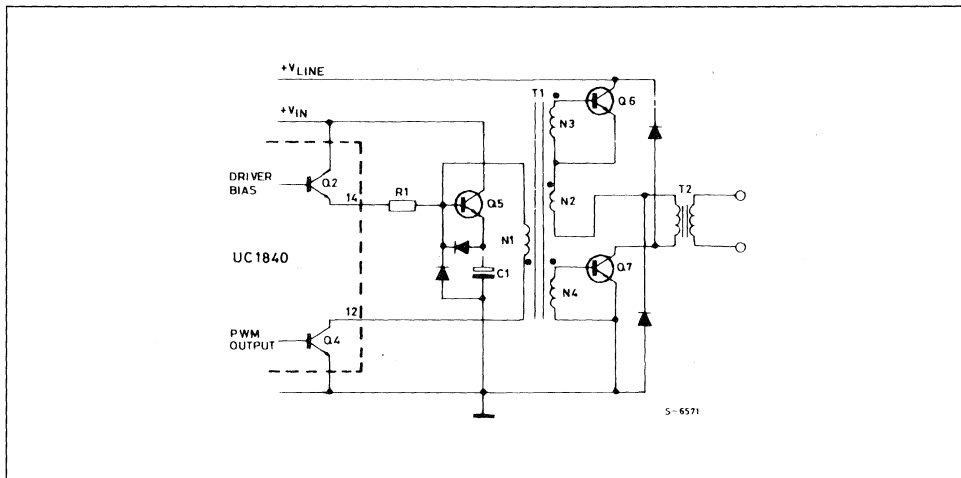
Another application is the two-transistor, off-line, forward converter topology shown in figure 14. This circuit uses proportional base drive where the UC1840 need only supply a short, turn-off current pulse with transformer regeneration through T1 providing the steady-state drive. The magnetizing current is controlled by R1, with Q5 added to rapidly recharge C1 from which the turn-off current is supplied.

FAULT PROTECTION

A significant benefit in using the UC1840 is the multi-

faceted fault-sensing and programming capability built into the device. With the intent to provide complete control to the power system under all types of potential malfunctions, fault-sensing circuitry has been included to sense over-voltage, under-voltage, or over-current conditions. Additionally, high-speed, pulse-by-pulse digital current limiting is included as a separate function. The operation of these circuits is described below.

Figure 14 : Interfacing the UC1840 single PWM output to a two-transistor off-line forward converter which uses proportional base drive.

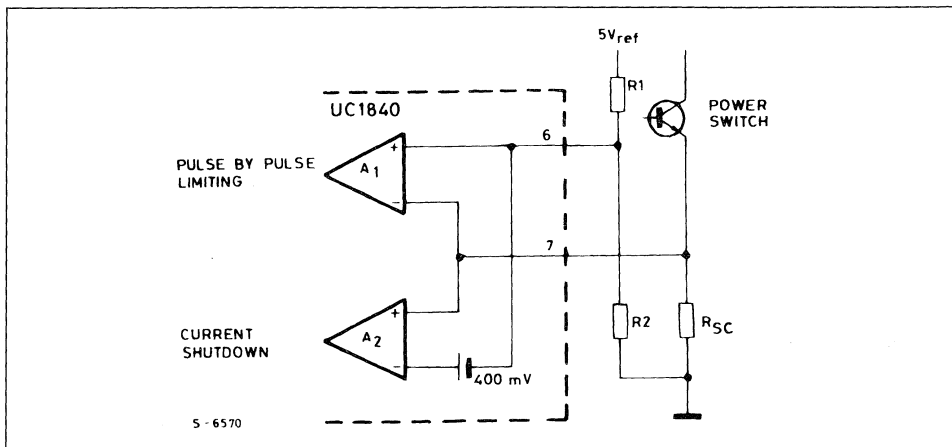


CURRENT LIMITING

The current limit comparators have differential inputs for noise rejection but are intended to be used with ground-referenced current sensing as in figure 15. Comparator A1 is delegated to pulse-by-

pulse current limiting. The output of this comparator drives the PWM comparator, where it activates the PWM latch, terminating each pulse when the current sensed by R_{SC} reaches a threshold defined by divider R1, R2, and the 5 V reference.

Figure 15 : Current limiting and overcurrent shutdown are implemented with comparators of different thresholds and a single current sense resistor.



Since V_C is intended to track the supply's output voltage, the addition of a resistor from pin 6 to V_C will provide some foldback to the current limit characteristic. Since comparator A1 has zero offset voltage, it is activated when the voltage across R_{SC} equals that across R2. Comparator A2, with an offset voltage of 400 mV, will activate for over-current shutdown when the voltage across R_{SC} rises to 400 mV higher than the voltage across R2. Since the input bias to both comparators is less than 5 μ A, a low-pass filter for noise rejection may be inserted between R_{SC} and the sense inputs. Activation of comparator A2 is defined as an over-current fault and it triggers the Error Latch. Its operation follows.

FAULT SEQUENCING

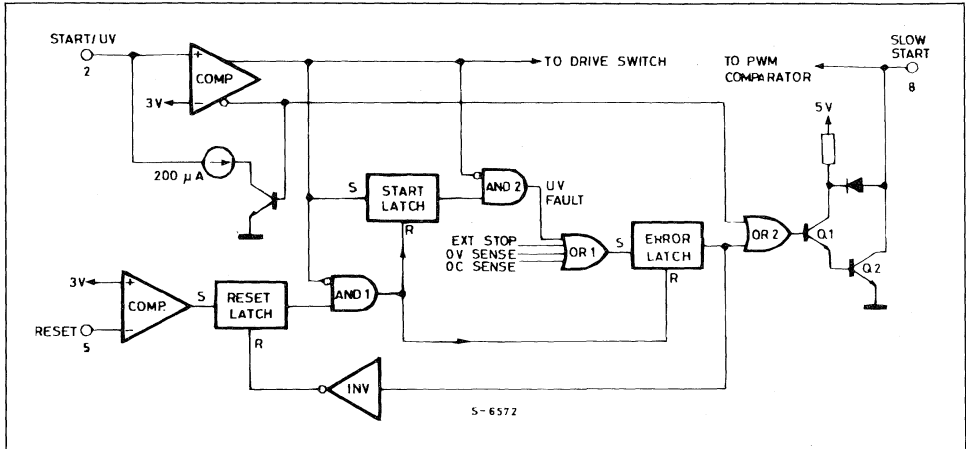
The fault sequencing logic of the UC1840 is shown in figure 16. Since a fault is defined by this device as an activation of the Error Latch, it makes sense to start here in an attempt to understand this portion of the circuitry. Setting the Error Latch immediately

turns on Q1 and Q2, discharging the slow-start capacitor and terminating the PWM output. Note that there is an additional path from the inverted output of the Start/UV comparator through OR2 which keeps pin 8 low. This is to keep the slow-start low during initial turn-on which is not intended to be classified as a fault.

The input to the Error Latch is from OR1 which triggers on signals resulting from four possible events :

- (1) A voltage less than 3 V (after prior turn-on) at the Start/UV sense terminal, pin 2.
- (2) A voltage greater than 3 V at the Over-Voltage Sense terminal, pin 3.
- (3) A voltage of less than 3 V on the Ext. Stop terminal, pin 4.
- (4) An over-current signal resulting in a differential voltage between pins 7 and 6 of greater than 400 mV.

Figure 16 : Fault sequence logic is designed to insure a complete shutdown and fully controlled restart upon any of four possible fault conditions.



Any of these inputs need only be momentary to set the Error Latch. Transient protection may be necessary to eliminate false triggering, but it can be readily accomplished as all the comparator inputs are high impedances requiring less than $2\ \mu\text{A}$ of input current, and the 3.0 V reference yields a high noise immunity.

The Start Latch can be understood by recognizing that at initial turn-on it is reset with a low output. This prevents AND2 from transmitting a UV fault signal from the Start/UV non-inverting output to the Error Latch. At the start voltage level, defined by a high level on the Start/UV non-inverting output, the Start Latch sets but AND2 still provides no output. Only when the Start/UV input goes low again, with the Start Latch output held high, will AND2 yield an output into the Error Latch.

The status of the Reset terminal, pin 5, determines what happens after the Error Latch is set. The choices are :

- (1) Latch off and require a recycle of input voltage to restart.
- (2) Continuously attempt to restart.
- (3) Attempt some number of restarts and then latch off.

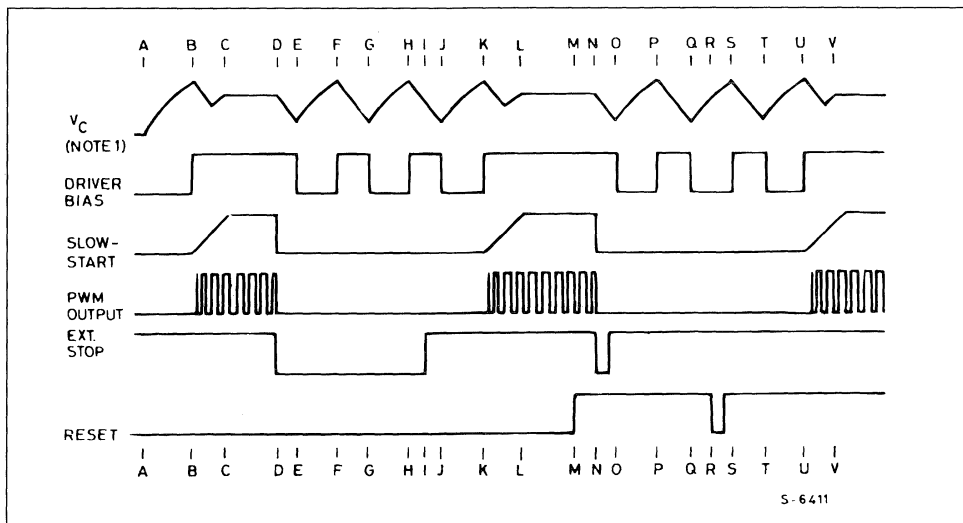
- (4) Latch off and await a momentary reset pulse to restart.

To examine the operation of the Reset Latch, note that prior to setting the Error Latch, its low output is inverted to hold the reset input to the Reset Latch high. This forces the Reset Latch's output low, regardless of the voltage on pin 5, and, thus, insures no signal out of AND1. With the setting of the Error Latch, the Reset Latch is free to take the state commanded by pin 5 : high if pin 5 is low and vice-versa. The latch allows merely a pulse to set the Reset Latch ; the voltage on pin 5 need not be steady state.

With a high Reset Latch output, the Error Latch still does not reset until a low signal is sensed on the Start/UV sense terminal. At that point, AND1 then resets both the Error Latch and the Start Latch re-establishing the initial conditions for a normal start after fully charging the input capacitor. Of course, if the fault is still present, when the Start/UV input reaches the start level terminating the Error Latch reset signal, this latch will immediately set again.

To aid in the understanding of this logic, figure 17 gives a pictorial representation of its operation with both steady-state and momentary signals on both the Ext. Stop and Reset terminals.

Figure 17 : The interrelationship between the functions controlled by the fault sequence logic is illustrated with both static and pulse commands on the ext. stop and reset terminals.



Notes : 1. V_C represents an analog of the supply output voltage generated by a primary - referenced secondary winding on the power transformer. It is the voltage monitored by the start/UV comparator and in most cases is the supply voltage V_{IN} for the UC1840.

Time	Event
A	Initial turn-on V_C rises with light load.
B	Start threshold driver bias loads V_C .
C	Operating PWM regulates V_C .
D	Stop input sets. Error latch turning off PWM.
E	UV low threshold. Error latch remains set.
F	Start turns on driver bias but error latch still set.
G	V_C and driver bias continue to cycle.
H	
I	Stop command removed.
J	Error latch reset at UV low threshold.
K	Start threshold now removes slow-start clamp.
L	Return to normal run state.
M	Reset latch set signal removed.
N	Error latch set with momentary fault.
O	Error latch does not reset as reset latch is reset.
P	V_C and driver bias recycle with no turn-on.
Q	
R	Reset latch is set with momentary reset signal.
S	V_C must complete cycle to turn on.
T	Start and error latches reset.
U	Normal start initiated.
V	Return to normal run state.

If Driver Bias turn-on is used to pump an increment of charge into an integrating capacitor, and that capacitor voltage is applied to the Reset Terminal, some number of retries could be programmed to take place before the Reset voltage rises to 3 V, which would then lock the output OFF. Since Driver Bias continues to cycle in the latched-off state, the Reset terminal will remain high until it is either remotely pulled low or the input voltage to the controller is interrupted.

Note that an important element in any restart after a shutdown is the lowering of the voltage at the Start/UV terminal below its UV threshold. While this will occur normally in bootstrap-driven applications, this device can also be used with a constant driving voltage by externally applying a momentary pull-down signal to the Start/UV input after a fault shutdown.

CONCLUSION

With the UC1840, power supply designers now have a device specifically developed for off-line, primary control and one which has addressed the problems of operation under less than "ideal" or normal conditions. Not only does this device make it easier to comply with stringent isolation requirements by requiring a minimum of communication between primary and secondary, but it is also ideally suited for powering systems in remote locations where only a simple transmitted pulse is available for power sequencing.

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50 W OFF-LINE SWITCHING POWER SUPPLY USING THE UC3840

INTRODUCTION

This power supply has been designed to provide an easy way to gain familiarity with the operating characteristics of the UC3840 PWM Control Circuit in a practical off-line power supply application. As any switching power supply represents a series of compromises between size, cost, efficiency, performance, and many other variables; no claim is made that this supply optimizes any particular characteristics; only that it provides an easy means to gain an understanding which, hopefully, the designer can use to extrapolate to many specific applications.

This power supply, shown schematically in fig. 4 implements a 50 Watt discontinuous mode flyback power supply with multiple outputs, and features primary-side control with full protection from fault conditions. Additional performance characteristics include simple off-line starting, voltage feed-forward for good line regulation (without feedback across the isolation boundary), pulse-by-pulse current limiting, over-and under-voltage sensing with protective shut-down and automatic restart, and freedom from the need for any circuit adjustments.

For additional information on the operation of the UC3840, reference should be made to AN248 and data sheet.

POWER SUPPLY SPECIFICATIONS

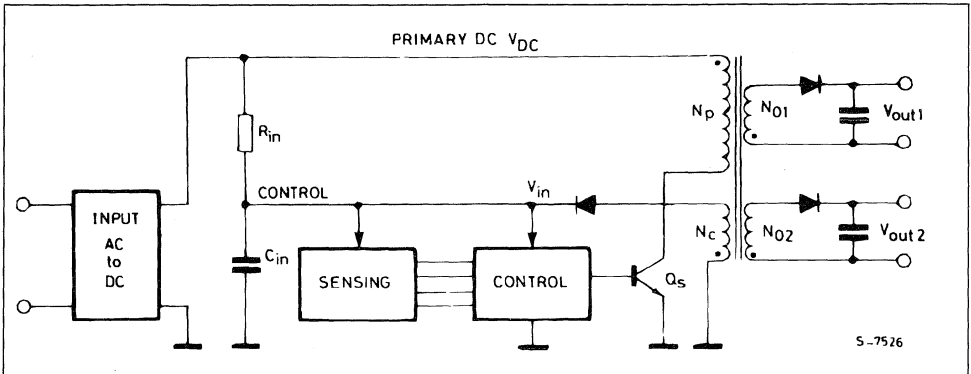
Input line voltage :	
With 110 V jumper :	90 VAC to 130 VAC
With jumper removed :	180 VAC to 260 VAC
Input frequency :	50 or 60 Hz
Switching frequency :	40 KHz $\pm$ 10 %
Output power :	50 W maximum
Output voltages :	5 V $\pm$ 5 % 12 V $\pm$ 5 %
Output current :	2.5 to 5 A (5 V) 1 to 2 A (12 V)
Line regulation :	5 V, 0,07 %/V 12 V, 0,04 %/V
Load regulation :	5 V, 2,5 %/A 12 V, 2,5 %/A
Efficiency @ 50 watts	
V_{in} = 90 VAC :	70 %
V_{in} = 130 VAC :	65 %

Output ripple :	5 V @ 5 A = 200 mV 12 V @ 2 A = 300 mV
-----------------	---

OPERATING PRINCIPLES

In an off-line switching power supply, the input voltage is immediately rectified and filtered, and the resulting DC voltage is chopped at a high frequency. Where 110/220 VAC operation is required, an input voltage doubler configuration is used for 110 VAC input, resulting in a nominal DC input voltage of 310 V. The same nominal input voltage is obtained with full wave rectification of a 220 VAC line input. High frequency switching allows a very small transformer to be used to efficiently step down to lower output voltages. In the configuration shown in figure 1 an additional low-voltage winding, N_c , is used to provide continuous operating power for the control and base drive circuits. However, initial energy to start the supply is taken from the line via R_{in} and C_{in} . An additional function on N_c is to provide a primary-referenced feedback voltage that is proportional to the output voltages. This feedback voltage is sensed and regulated by the control circuitry, thereby eliminating the need for feed-back across the isolated boundary.

The polarity of the transformer windings identifies this configuration as a flyback supply. When transistor Q_s conducts, all output diodes are reverse biased and the energy is stored in the primary inductance. When Q_s turns off, the voltage polarity of winding N_p reverses (flies back) and the energy is delivered to the output circuits. This circuit operates in the discontinuous mode in which all the energy stored in the transformer inductance is completely transferred to the load during every cycle, i.e. transformer current goes to zero before the end of each cycle. Although this approach yields higher peak current compared to other topologies, it is usually chosen because of its less stringent requirements on the transformer, its faster transient response, and its easier stabilization. To insure discontinuous operation and core reset, the volt-second product across the transformer primary during reset must be allowed to equal or exceed the volt-seconds applied during the on-time of Q_s .

Figure 1 : Simplified Block Diagram of a Flyback Power Supply with Primary Control.

DESIGN CONSIDERATIONS

The following description of the design decisions made for this power supply will be with respect to the complete schematic shown in fig. 4. No significant theoretical discussion is offered and only nominal values are used in the analysis, but hopefully the equations given can be used to either extrapolate to other design problems or to optimize the supply to a particular characteristics.

INPUT SECTION

Input bridge D1 rectifies the line voltage while resistors R1 and R2 are used to limit the peak charging current to capacitors C1 and C2. The values for C1 and C2 are usually determined by either the ripple voltage allowable for V_{DC} or the minimum hold-up time.

Ripple calculations are worse-case for the 110 V voltage doubler configuration where :

RMS line voltage = 90 to 130 VAC
peak no-load input = 253 to 368 Volts.

At the minimum line voltage, each capacitor alternately charges to a peak of 126 Volts. Allowing for a total input voltage sag at full load of 50 volts, the minimum capacitor voltage must be held to 92 volts. Since each capacitor must provide one-half the energy requirements of the power supply, the required energy for each line cycle is :

$$W_{in} = \frac{\text{Power out}}{\text{Efficiency} \times \text{Frequency}} = \frac{50}{0.7 \times 60} = 1.2 \text{ Joule}$$

and the capacitor value can be calculated from :

$$\frac{1}{2} W_{in} = \frac{1}{2} C_1 (V_{pk}^2 - V_{min}^2) \text{ or}$$

$$C_1 = \frac{W_{in}}{V_{pk}^2 - V_{min}^2} = \frac{1.2}{126^2 - 92^2} = 162 \mu F$$

If, instead of ripple voltage, we choose the input capacitors to hold the input DC above 200 volts for a least two cycles of line drop-out, then :

$$C_1 = \frac{2 (P_o/2) (\text{no. of cycles drop-out}) 1/f}{\text{Efficiency} (V_{pk}^2 - V_{min}^2)}$$

$$= \frac{2 (25) (2) 1/60}{0.7 (126^2 - 92^2)} = 331 \mu F$$

In this application, 470 μF was picked as a standard size which would allow loose tolerances.

TRANSFORMER

A major task with any flyback power supply is the design of the transformer as many tradeoffs are normally required between regulation, leakage inductance (and corresponding transistor stress), isolation, size, and cost. In this application, the core selected is a Ferroxcube EC35-3C8 which has the following characteristics :

Effective core area, $A_e = 0.84 \text{ cm}^2$
Max flux density, $B_{sat} = 2800 \text{ gauss}$
Bobbin = 35 PC B I

The design starts with a calculation of maximum duty cycle which is defined by the voltage capability of the power switch. This voltage was allocated as follows :

VDC max	= 370 V
Reset voltage	= 120 V
Leakage inductance spike	= 100 V
Max total voltage	= 590 V

With a reset voltage of 120 V, at minimum input voltage,

$$D_{max} = \frac{120 \text{ V}}{120 \text{ V} + 200 \text{ V}} = 37.5 \%$$

The primary inductance can then be calculated as :

$$L_p = \frac{\text{Efficiency}}{2 P_o f} (V_{in \min} \times D_{\max})^2 =$$

$$= \frac{0.7 (200 \times 0.375)^2}{2 \times 50 \times 40 \times 10^3}$$

$$L_p \approx 1 \text{ mH}$$

The peak current at full load is :

$$I_p = \frac{2 P_o}{\text{eff} (V_{in \min} \times D_{\max})} =$$

$$= \frac{2 \times 50}{0.7 \times 200 \times 0.375} = 1.9 \text{ A}$$

The maximum energy storage requirement within the primary is calculated on the basis of maximum current, in this case assumed to be short circuit current = 120 % $\times I_p$ or 2.3 A.

$$W = 1/2 L I_{SC}^2 = 1/2 (1 \times 10^{-3}) (2.3)^2 = 2.65 \text{ m Joule}$$

The equation defining energy storage in an inductor is :

$$W = 1/2 \frac{B A_c H_{\phi e} \times 10^{-8}}{0.4 \pi} \text{ Joules}$$

Therefore

$$H_{\phi e} = (0.4 \pi) \frac{2 W \times 10^8}{B A_c} =$$

$$= \frac{0.4 \pi \times 2 \times 2.65 \times 10^{-3} \times 10^8}{2800 \times 0.84} = 282 \text{ Gilberts}$$

Since $H_{\phi e} = 0.4 \pi N I$, on the basis of $I_{SC} = 2.3 \text{ A}$

$$N_p = \frac{H_{\phi e}}{0.4 \pi I_{SC}} = \frac{282}{0.4 \pi \times 2.3} = 298 \text{ turns}$$

The air gap for the core is determined by knowing that

$$H = \frac{B}{\mu} = 2800 \text{ Oersteads}$$

And assuming that with an air gap

$$I_e \approx I_g, \text{ then}$$

$$I_g = 0.4 \pi \frac{N I}{H} = \frac{0.4 \pi (98) 2.3}{2800} = 0.1 \text{ cm}$$

With the primary turns defined, each secondary can be calculated from :

$$N_s = \frac{N_p (V_o + \text{rectifier } V_f) (1 - D_{\max})}{V_{in \min} D_{\max}}$$

With minor adjustments to give an integral number of turns, the final transformer winding specifications are :

First winding - primary - 97 turns, AWG 24

Second winding - 5 volt - 4 turns, 4 parallel AWG 22

Third winding - 12 volt - 9 turns, 2 parallel AWG 22

Last winding - control - 9 turns, AWG 24 evenly spaced along the full bobbin length.

POWER SWITCH AND DRIVERS

In this application, the peak switch current is 2.3 amps and the peak collector voltage will be approximately 590 Volts including the spike caused by leakage inductance. The switching transistor selected is the MJE13005 which has the following characteristics relative to this application :

BV_{ceo}	= 400 V
BV_{cer}	= 700 V
$I_c \text{ (cont)}$	= 4 A
h_{fe}	= 8 - 40 @ 2 A
t_s	= 1.5 μ s
t_r	= 0.28 μ s
t_f	= 0.25 μ s

While offering inexpensive, high-voltage switching, the MJE13005 needs some support to provide adequate base drive and minimize storage time. This is readily accomplished with the circuitry shown in figure 2. Prior to obtaining a start-up signal, the Drive Bias transistor in the UC3840 is off insuring that there is no quiescent current being drawn by any of this interface circuitry. At start-up, the Drive Bias switch turns on providing a pull-up for the UC3840's PWM output. The current through R16 is multiplied by the gain of Q1 to provide a forward base drive in excess of 250 mA for the power switch Q3. Diodes D5 and D6 form a Baker clamp to keep Q3 out of hard saturation and improve turn-off, especially at lower collector currents.

Transistor Q2, driven on by the turn-off of Q1, provides a low-impedance path for reverse base current of Q3, and together with the use of the Baker clamp, results in a storage time for Q3 of less than 800 nsec.

The power loss in R26 comes from the energy stored in the leakage inductance which is

$$P = 1/2 L_e I_{sc}^2 f = 1/2 50 \times 10^{-6} (2.3)^2 40 \times 10^3$$

$$P \approx 5.3 \text{ Watts}$$

but here again, second order effects tend to reduce this value to less than 3 Watts in this power supply.

OPERATING FREQUENCY

The frequency is set by R14 and C4 as

$$f = \frac{1}{R_T C_T} = \frac{1}{R_{14} C_4} = \frac{10^3}{12 \times 0.0022} \approx 40 \text{ kHz}$$

SUPPLY START-UP

The supply must reliably start with V_{DC} minimum = 250 V. The value of R3 + R4 is defined by the total current requirement of the control electronics prior to start. If a start threshold of 12 volts is assumed, total control current is :

UC3840 max	= 7.0 mA
R7 + R8	= 0.70 mA
R10 + R11	= 0.27 mA
C4 charging current	= 0.40 mA
R17 + R18	= 0.22 mA
Total Turn-on Current	8.59 mA

$$\text{and } R3 + R4 = \frac{250 - 12}{8.59} = 27 \text{ k}\Omega$$

Note that R3 and R4 also provide a bleeder path to discharge C1 and C2.

Once start-up is initiated, the control current becomes :

UC3840 max	= 15 mA
R16	= 6 mA
Q3 Ib (x 0.375 duty cycle)	= 94 mA
Total run current	= 115 mA

This current must come from C3 until power is available from control winding, N4. This, in conjunction with the start-up time, defines a minimum value for C3.

Although a small soft-start capacitor is incorporated in this supply, its time constant is much shorter than the time to charge the output capacitors with the duty cycle defined by the ramp waveform and the pulse-by-pulse current limit. With the supply fully loaded, start up takes approximately 5 msec. During this time, the voltage on C3 cannot fall below the under-voltage threshold.

In defining the start and UV thresholds, one other consideration is the state of the error amplifier. As defined further below, the error amplifier is going to

force V_C to 12 Volts. If the start threshold is set above this value, the start signal will release the soft-start clamp and arm the driver bias but no PWM output will appear until V_C droops below 12 Volts and the output of the error amplifier goes high. To insure soft-start action, the start threshold has been set at 11 Volts and the under-voltage level is 8 Volts.

Now the value for C3 can be determined from :

$$C3_{(min)} = \frac{I_{(start)} t_{on}}{\Delta V_C} = \frac{(115 \times 10^{-3}) (5 \times 10^{-3})}{(11 - 8)} = 192 \mu F$$

The start and under-voltage thresholds are defined by R7 and R8 conjunction with the 3 volt threshold and the hysteresis current of the comparator on pin 2 of the UC3840. As the voltage rises on pin 2, that pin is sinking 200 μA of current causing an added voltage drop across R7. When pin 2 reaches 3 volts, turn-on is initiated and - at the same time the hysteresis current is removed causing the voltage at pin 2 to jump above 3 volts.

Now, as the power supply attempts to start, the voltage on pin 2 falls and, if it reaches 3 volts from this direction, an under-voltage fault is sensed.

The start voltage at V_C is defined by :

$$V_C(\text{start}) = \frac{3 \text{ V } (R7 + R8)}{R8} + 0.2 \text{ mA } (R7) = 11 \text{ V}$$

while the under-voltage threshold is :

$$V_C (\text{UV fault}) = \frac{3 \text{ V } (R7 + R8)}{R8} = 8 \text{ V}$$

This second equation may be subtracted from the first to yield $R7 = 15 \text{ k}\Omega$, which then defines $R8$ 9.1 $\text{k}\Omega$.

An over-voltage fault in terms of V_{DC} can be calculated by equation :

$$V_{DC} (\text{OV fault}) = 3 \text{ V } \frac{(R5 + R6)}{R6} = 400 \text{ V, or}$$

$$R5 = 132 \text{ R}\Omega$$

Small capacitors (10 nF) have been added to both comparator inputs to minimize noise sensitivity.

FEED-FORWARD

This function provides a variable-slope ramp waveform on pin 10 which is one of the inputs to the PWM comparator. This signal is compared with the output from the error amplifier on pin 1, and the pulse width is defined by the time it takes the ramp to rise to the

level of the error amplifier's output. If the ramp slope is made proportional to the DC input voltage, a rising input voltage will immediately increase the ramp slope, and correspondingly reduce the pulse width with no change required from the error amplifier's output. The result will be a constant volt-second product delivered to the transformer primary resulting in good open-loop line regulation.

The design procedure used to define the ramp characteristics is to set the ramp slope such that it reaches its peak value at a time equal to the maximum pulse width allowed by the transformer design. This was set at 43 % with minimum input voltage and a potential shorted output. The time for the ramp to go from its minimum to maximum value is then :

$$t_{on(max)} = \frac{0.43}{f} = \frac{0.43}{40 \times 10^3} = 10.75 \mu\text{sec}$$

and the slope is :

$$\begin{aligned} \frac{dv}{dt} (\text{min}) &= \frac{V_{pk} - V_{valley}}{t_{on(max)}} = \\ &= \frac{4.2 - 0.5}{10.75} = 0.344 \text{ V}/\mu\text{sec} \end{aligned}$$

and since the slope is determined by :

$$\begin{aligned} \frac{dv}{dt} &= \frac{V_{DC}}{R15 \text{ C8}} \\ R15 \text{ C8} &= \frac{200 \text{ V}}{0.34 \text{ V}/\mu\text{s}} = 581 \mu\text{sec} \end{aligned}$$

With the knowledge that the ramp generator has greatest linearity with currents in the 100 μA to 300 μA range, we can pick :

$$R15 = 1.5 \text{ M}\Omega \text{ and } C8 \approx 390 \text{ pF.}$$

DUTY CYCLE CLAMP

The above analysis has provided a maximum duty cycle of 43 % at minimum operating voltage. When the AC line voltage is removed, however, the input voltage will fall below 200 volts with the supply still running. As this voltage falls, the ramp slope will reduce and at the same time the error amplifier output will increase in an attempt to maintain regulation. This could extend the pulse width beyond 43 % except for the action of the duty cycle clamp divider of R19 and R20 which is set to provide 3.9 V at pin 8 with $V_{DC} = 200 \text{ V}$. Therefore, as V_{DC} falls, the volt-

age on pin 8 will also fall, taking command away from the error amplifier and maintaining a constant pulse width until the Under-Voltage sensing circuit gives a shutdown command.

VOLTAGE CONTROL

In this power supply, output voltage regulation is controlled from the primary side by sensing V_C with R10 and R11 and closing a control loop with the error amplifier and 5 V reference in the UC3840. The output voltage is then :

$$V_o (5 \text{ V}) = \left(\frac{N2}{N4} \right) V_{ref} \left(\frac{R10 + R11}{R11} \right)$$

Although the UC3840 optimizes this approach by the use of feed-forward which provides first-order automatic line regulation, there will still be inaccuracies caused by inadequate coupling between the windings, IR drops within the windings, and unequal losses in the rectifiers. If greater voltage accuracy is required, the feedback loop must be connected directly to one of the outputs with either an optical coupler or the UC1901 isolated Feedback Generator used to maintain isolation.

The gain and phase plots for this supply are shown in figure 3. Overall loop stability is aided by the fact that a discontinuous-mode flyback topology is inherently a single pole system defined by the output load. Its transfer function, excluding the error amplifier, is shown by the dashed curve of figure 3. The DC gain from the modulator input V_C , to the output, V_O , is :

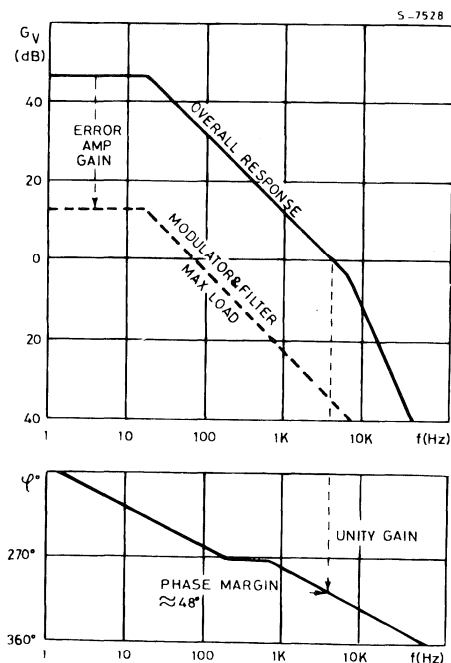
$$\frac{V_o}{V_C} = K \sqrt{\frac{TR_{L \text{ min}}}{2 L_P}}$$

where K is defined by the feed-forward slope as

$$K = \frac{(\text{Max duty cycle}) (V_{in \text{ min}})}{\text{Ramp peak} - \text{Ramp valley}} = \frac{0.43 \times 200}{4.2 - 0.5}$$

and the minimum load resistance reflected to the primary control supply is :

$$\begin{aligned} R_{L \text{ min}} &= \frac{V^2}{P_{o \text{ max}}} = \frac{12^2}{50} = 2.88 \Omega \\ \frac{V_o}{V_C} &= \frac{0.43 \times 200}{4.2 - 0.5} \sqrt{\frac{25 \times 10^{-6} \times 2.88}{2 \times 1 \times 10^{-3}}} = \\ &= 4.41 = 13 \text{ db} \end{aligned}$$

Figure 3 : Power Supply Loop Gain and Phase.

The effective output capacitance, also reflected to the control supply, is :

$$C_E = C_{14} \left(\frac{N_2}{N_4} \right)^2 + C_{13} \left(\frac{N_3}{N_4} \right)^2 + C_3$$

$$= 4700 \left(\frac{4}{9} \right)^2 + 2200 \left(\frac{9}{9} \right)^2 + 200$$

$$= 3328 \mu\text{F}$$

This yields an output pole at

$$f_1 = \frac{1}{2\pi R_L C_E} = \frac{10^6}{6.28 (2.88) 3328} = 16.6 \text{ Hz}$$

The error amplifier is set up for an added DC gain of approximately 35 dB and a second pole at 8 kHz - a frequency well above the overall unity gain point and yet below the roll-off frequency of the error amplifier.

CURRENT LIMITING

The UC3840 limits current through the power switch, Q3, by sensing the voltage across R25. Pulse-by-pulse current limiting is defined by the divider R17, R18, and the value of R25 as :

$$I_{SC} = \frac{V_{REF} R_{18}}{R_{25} (R_{17} + R_{18})}$$

$$= \frac{5.0 (10 \text{ k})}{1 \Omega (12 \text{ k} + 10 \text{ k})} = 2.2 \text{ amps.}$$

If the required pulse width becomes too narrow for the pulse-by-pulse circuitry to respond, the UC3840 contains a second level of protection by initiating a fault shut-down if the voltage across R25 rises to 400 mV above the voltage established by R17 and R18 on pin 6. Care must be taken that this threshold is not exceeded by a leading edge spike which might be present on the current waveform.

FAULT PROTECTION

The UC3840 defines four functions as faults.

1. An under-voltage signal on pin 2 (after a start command)
2. An over-voltage signal on pin 3
3. An external stop command on pin 4
4. An over current shut-down from pin 7

Any of these functions will initiate a complete shut-down of the controller with restart defined by the voltage on the reset terminal, pin 5.

If pin 5 is high or open, any fault will latch the supply off and it can only be restarted by reducing the input voltage to zero or by momentarily pulling pin 5 low. Alternatively, grounding pin 5 will cause an automatic restart after any fault shut-down.

CONSTRUCTING THE KIT

It is assumed that the user possesses reasonable electronic assembly skills and therefore detailed step-by-step instructions have not been considered necessary. Rather, a general assembly procedure is outlined below which, if followed carefully, should offer no problems. Assembly starts by properly orienting the PC board with the assembly drawing shown in figure 5. This drawing is of the component side of the board - etch side down - with the "Warning - High Voltage" label at the lower left hand edge.

TEST AND TIE POINTS

Pads have been provided on the PC board for input and output connections and for many internal test points so that complete operation of all portions of the control circuitry can be evaluated. These points are noted in figure 5 and are listed below :

AC input	(2 pads)
DC input	(2 pads each note that the commons may be separated for alternate polarities)
+ 12 V output.....	
+ 5 V output.....	
H.V. Switching	(3 pads)
Transistor	

Note : 600 V pulses will appear at the collector.

BE CAREFUL OF THIS TEST POINT.

Control Voltage V_C	IC pin 15
Primary Common	IC pin 13 (2 pads)
E/A Compensation	IC pin 1
5.0 V Reference	IC pin 16
E/A input	IC pin 17
Drive Bias	IC pin 14
PWM Control.....	IC pin 12
Ramp Waveform	IC pin 10
S/S Duty Cycle Limit.....	IC pin 8
Oscillator Frequency	IC pin 9
C/L Limit Sense.....	IC pin 7
C/L Threshold.....	IC pin 6
Reset input.....	IC pin 5
Ext. Stop Input.....	IC pin 4
OVP Sense Input	IC pin 3
UV/Start Input.....	IC pin 2

No connections to these points have been included in this kit. It is suggested that the user either supply terminals or solder in small stubs or loops of bus wire so that connections to these test points can easily be made on the component side of the PC board with scope probes or other test instrumentation leads.

JUMPERS

There are four jumpers required which are also not included in this kit. Use solid bus wire or a section clipped from the ends of the small resistors. These jumpers are :

- AC input jumper for 110 V operation (leave out if 220 VAC is to be used)
- PWM jumper to pin 12
- UV/start jumper to pin 2
- Reset jumper on pin 5 (leave out if it is desired to latch the supply off after any fault)

Note that there is nothing connected to pin 4. A low signal here will shut down the supply.

SMALL SIGNAL DIODES

The seven small axial lead diodes, D2 through D8 should next be installed insuring correct polarity as shown in figure 5.

PASSIVE DEVICES

Install the low-power resistors and small capacitors first. Follow with the four high-power resistors, R3, R4, R26 and R27. When inserting R26, keep the body of the resistor $\approx 3/4$ inch above the PC board. This resistor will get hot and it is best to have it above, rather than next to C11. At this time, the input diode bridge, D1, and the IC socket can be inserted. Note that pin 1 of the UC3840 is to the front of the PC board.

LARGE COMPONENTS

Assembly can be completed by installing the remaining components as follows :

- Two small signal transistors, Q1 and Q2
- Transformer
- Electrolytic capacitors : C1, C2, C3, C13 and C14. Check polarity against signs of foil side of PC board.
- Power transistor Q3 inserts with its front to the left, or input, inside of the PC board. Insertion is easier if the heat sink is clipped on first.

NOTE : THIS HEAT SINK IS AT THE SAME POTENTIAL AS THE COLLECTOR AND WILL HAVE UP TO 600 VOLTS PRESENT : KEEP IT CLEAR OF OTHER COMPONENTS, TEST LEADS, AND YOUR FINGERS.

- Install the 5 volt output rectifier, D9 with its front facing the right, or output side of the board. It also gets a clip-on heat sink.

Check to see that all components are installed and match the drawing of fig. 5. Insert the UC3840 into the socket.

CHECKOUT PROCEDURES

With the power supply fully assembled, the following checkout procedure is recommended before any input voltage is applied. This procedure is also useful for trouble-shooting a unit which is not operating properly. Checkout will be aided if the user has installed test points at all indicated positions in the PC board. Reference should be made to figure 5 for test point locations.

- Insure that there is no AC input voltage applied
- Double check all connections including diode and capacitor polarities. Insure that the UC3840 is correctly inserted into the socket.
- Connect a minimum load on one or both outputs equivalent to 25 watts total. i.e., $2\ \Omega$ on the 5 V

output and 12 on the 12 V output. Be careful of the heat from these loads.

4. Install a temporary jumper shorting the base and emitter of Q3 together. Use test points provided on PC board.
5. Connect a 0 to 30 volt, 500 mA lab supply to simulate the control voltage, V_C . Connect the positive lead to IC-15 and ground to IC-13. Note that IC-13 will be the ground reference point for all primary side measurements. Set V_C = Zero volts and add a 1 k Ω , 1/2 W resistor in shunt across the power supply terminals.
6. Increase V_C to 10 volts and check the following :
 - a. IC-16 : Should have 5 V if the reference is working.
 - b. IC-2 : Should be 2.3 V if hysteresis current is on.
 - c. IC-14 : Should be < 0.1 V as Driver Bias is off.
7. Increase V_C to 14 volts and check the following :
 - a. IC-2 : Should be 4.7 volts if hysteresis current is off.
 - b. IC-14 : Should be 12 volts with Driver Bias on.
 - c. IC-9 : Oscillator should show 40 kHz exponential waveform.
 - d. Return V_C to Zero volts but leave connected.
8. Apply the high voltage, V_{DC} . This can be done either with a DC lab supply with 300 V capability or the input AC line voltage.

A fuse rated at no more than two amps should be in series with the input line to prevent excessive damage in the event of a failure.

NOTE : BE SURE TO USE AN ISOLATION TRANSFORMER WHEN LINE POWER IS USED AS PRIMARY GROUND IS ONE SIDE OF THE LINE.

An AC variac will also be helpful in varying the input voltage.

If a DC power supply is used, connect the positive line to the V_{DC} test point at the top of the board. The negative line will connect to ground on IC-13. Insure that the base-emitter short is still connected to Q3.

9. With V_{DC} = 200 volts, set V_C = 10 volts and check the following :
 - a. IC-14 : Should be < 0.1 V if Driver Bias is off.
 - b. IC-8 : Should be < 0.1 V of Slow Start clamp is on.
 - c. IC-6 : Should be 2.3 V to establish current limit threshold.
10. With V_{DC} = 200 volts, increase V_C to 14 volts and check the following :
 - a. IC-14 : Should be 12 V with Driver Bias on.

- b. IC-8 : Should be > 3.9 V with Soft-Start clamp off.
 - c. IC-10 : Ramp waveform with linear rising slope extending for approximately 1/2 the total duty cycle. Note : scope probe input capacitance can affect this measurement.
 - d. IC-1 : Should be < 0.5 V at output of error amplifier.
 - e. IC-12 : Should be still clamped to < 1.0 V with no output pulses.
11. Reduce V_C to 10 volts and check the following :
 - a. IC-1 : Error amp output should now measure $\approx$ 4.1 V.
 - b. IC-12 : PWM output should have pulses of approximately 2 V amplitude with a duty cycle of $\approx$ 40 %.
 12. Reduce V_C to 7 volts and check the following :
 - a. IC-14 : Driver Bias should be off.
 - b. IC-8 : The soft-start clamp should be on.
 13. Check the fault protective measures by following the sequence below :
 - a. Start the supply by raising V_C above 14 volts and then returning it to 10 volts. Set high voltage to 200 volts. Monitor IC-12.
 - b. Simulate a fault by performing each of the following, in sequence :
 - (1) With an additional lab supply momentarily apply 3.5 V to the OVP on IC-3, or
 - (2) Again using an external supply, momentarily apply 3.0 V to the current sense point, IC-7 or
 - (3) Momentarily short the stop terminal, IC-4, to ground.
 - c. In each case, the signal on IC-12 should cease and IC-8 should clamp low.
 - d. To restart the supply after a fault, V_C must go below 8 volts to reset the error latch ; above 11 volts to restart ; and then slightly below 12 volts to obtain a PWM output.
 14. Remove all external supplies and remove the base-emitter shorting jumper on Q3. Reconnect the high voltage source and raise the voltage to obtain V_{DC} = 250 volts. The supply should be running. Q3 collector voltage can be monitored with the use of a high-voltage scope probe.

WARNING : PULSES UP TO 600 V ARE ON Q3'S COLLECTOR

Normal power supply evaluation tests of line and load regulation, etc., may now be conducted.

Note : In experimenting with this supply, the most probable mode of failure is the shorting of the high-voltage transistor, Q3. Should this occur, transistor Q2 will also go. A two amp input fuse will normally

APPLICATION NOTE

protect the input diodes, R1, R2 and the current sense resistor, R25, although these should be

checked before reapplying power. Diodes D5 and D6 are normally adequate to protect Q1 and the IC.

PARTS LIST

ICs		Resistors		Miscellaneous	
U1	UC3840N	R1, R2	1 Ω , 1/2 W	HS1, HS2, Heat Sink Thermalloy 6043	
Transistors		R3	15 k, 2 W	T1	Transformer
Q1, Q2	2N2222	R4	12 k, 2 W	Coilcraft, E- 4140 - B	
Q3	MJE 130005	R5	750 k		
Diodes		R6	5.6 k		
D1	VM68 Bridge	R7	15 k		
D2, D6, D7	1N3614	R8	9.1 k		
D3, D4	1N3612	R9	unused		
D5	1N4946	R10	26.7 k, 1 %		
D8	UES1103	R11	17.8 k, 1 %		
D9	USD735	R12	1.5 M		
Capacitors		R13, R14	12 k		
C1, C2	470 μ F, 250 V	R15	1.5 M		
C3	200 μ F, 25 V	R16	1.5 k		
C4	2200 pF, 10 %	R17	12 k		
C5, C6	10 nF, 50 V	R18	10 k		
C7	22 pF	R19	750 k		
C8	390 pF, 10 %	R20	15 k		
C9, C10	10 nF, 50 V	R21	33 Ω , 1/2 W		
C11	10 nF, 400 V	R22	15 k		
C12	680 pF, 800 V	R23	4.7 k		
C13	2200 μ F, 16 V	R24	2.0 k		
C14	4700 μ F, 10 V	R25	1.0 Ω , 1 W		
		R26	4.7 k, 4 W		
		R27	1.8 k, 2 W		

Figure 4 : UC3840 PWM Control Circuit.

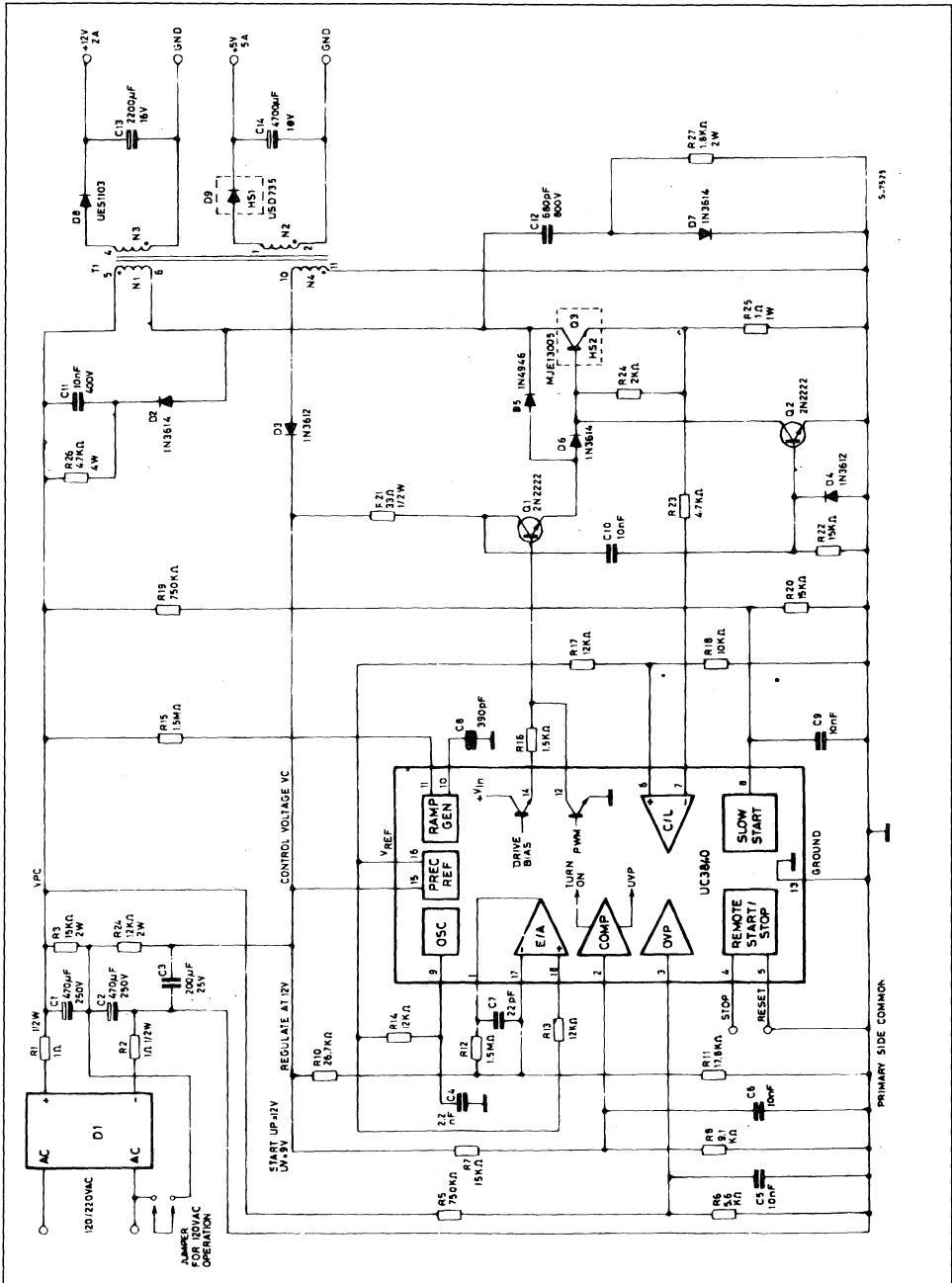
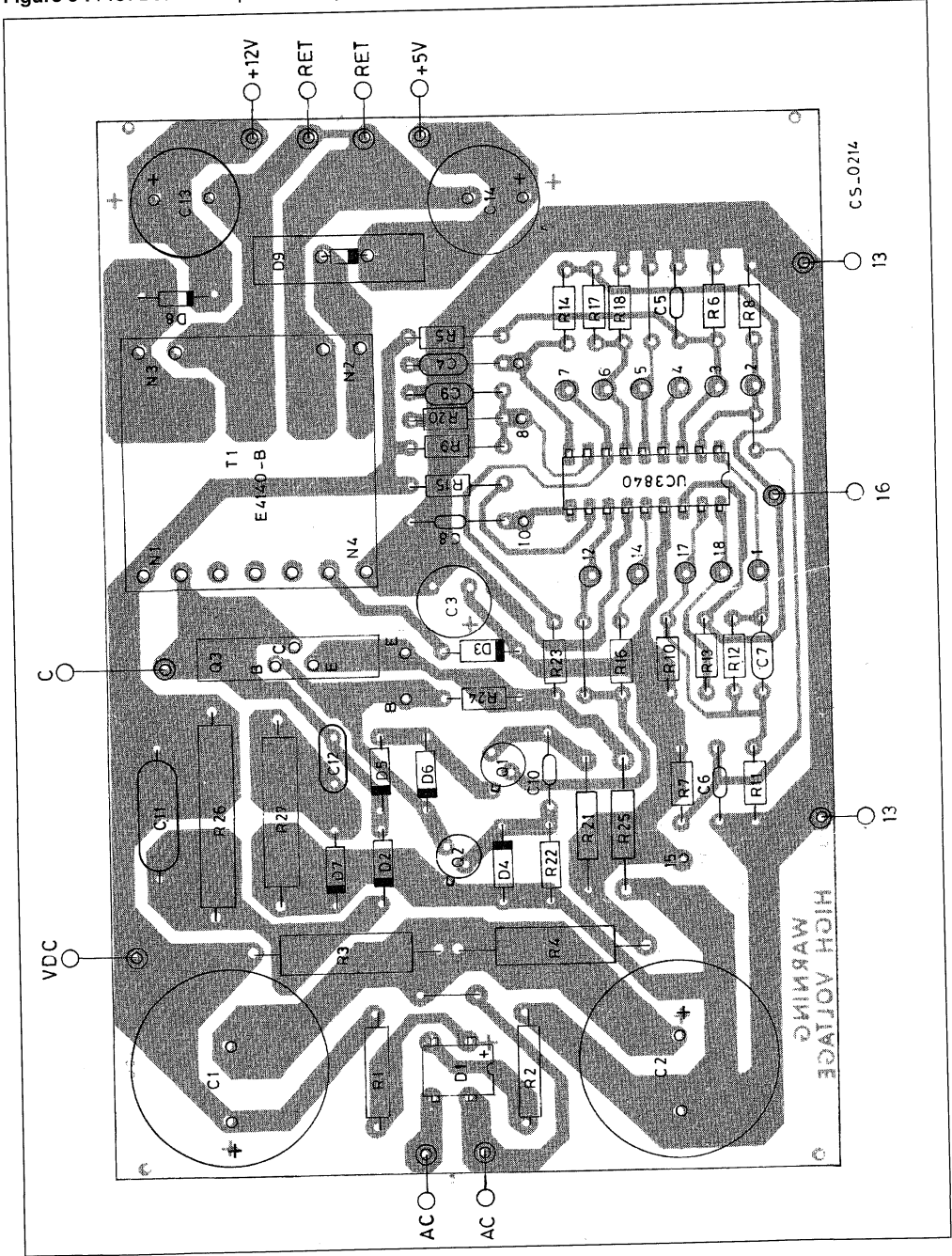


Figure 5 : P.C. Board Components Layout of the fig. 4 (1:1 scale).



A SECOND-GENERATION IC SWITCH MODE CONTROLLER OPTIMIZED FOR HIGH FREQUENCY POWER MOS DRIVE

INTRODUCTION

Since the introduction of the SG1524 in 1976, integrated circuit controllers have played an important role in the rapid development and exploitation of high-efficiency switching power supply technology. The 1524 soon became an industry standard and was widely second-sourced.

Although this device contained all the basic control elements required for switching regulator design, practical power supplies still required other functions which had to be implemented with additional external discrete circuitry.

An additional development within the semiconductor industry was the introduction of practical Power

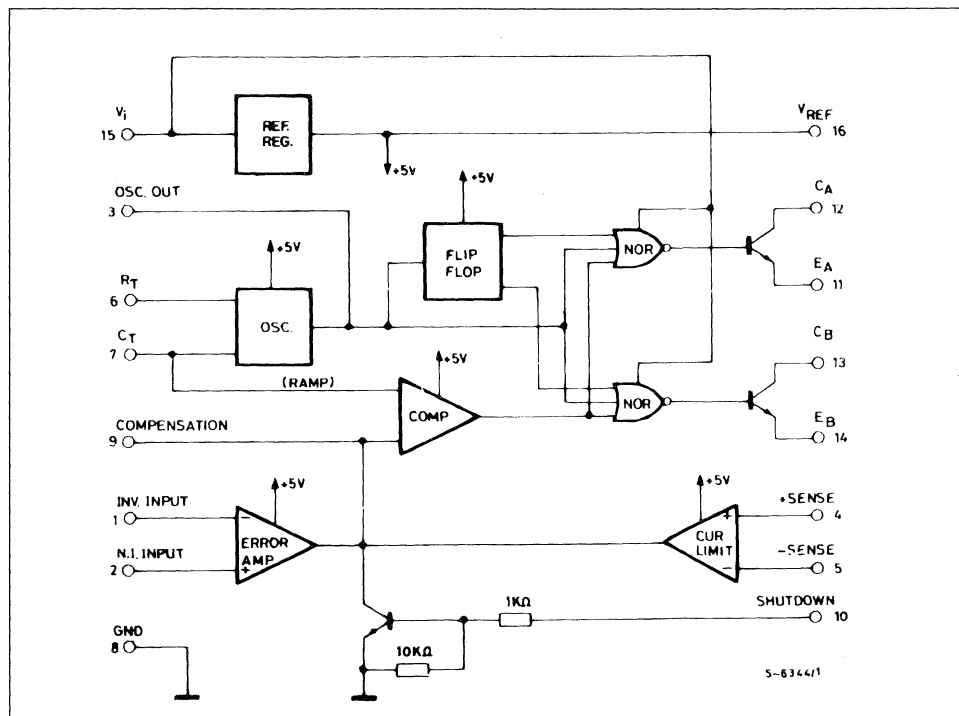
Mos which offered the potential of higher efficiencies at higher speeds with resultant lower overall system costs.

In order to be able to take full advantage of the speed capabilities of power MOS, it was necessary to provide high peak currents to the gate during turn-on and turn-off to quickly charge and discharge the gate capacitances of 800 to 2000 pF present in higher current units.

The development of a second-generation regulating PWM IC, the SG1525A, and its complimentary output version, the SG1527A, was a direct result of the desire to add more power supply elements to the control IC,

Figure 1 : The SG1524 relating PWM block diagram.

This design was the first complete I.C. control chip for switch mode power supplies.



as well as to optimize the interfacing of high current power devices.

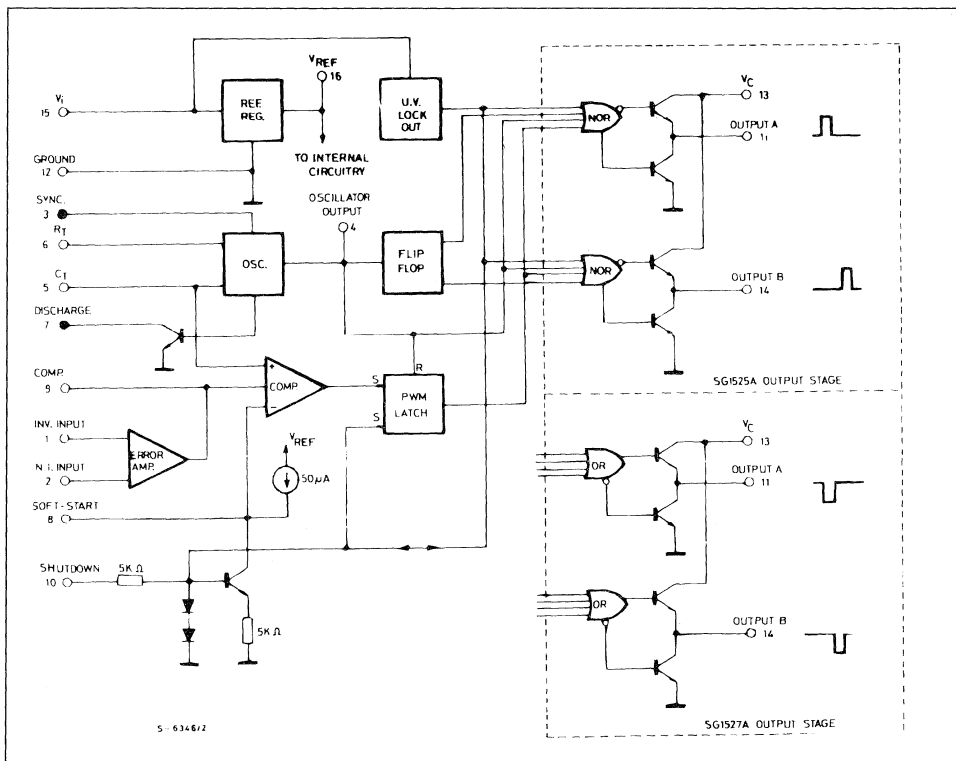
INTEGRATING MORE POWER SUPPLY FUNCTIONS

Having achieved the greatest level of acceptance among users of first generation control chips, the 1524 became the starting point for expanding IC controller capabilities. This early device, shown in figure 1, contains a fixed-voltage reference source, an oscillator which generates both a clock signal and a linear ramp waveform, a PWM comparator, and a toggle flip-flop with output gating to switch the PWM signal alternately between the two outputs.

With this circuitry already defined, a two pronged development effort was initiated : 1) to add additional features required by most power supply designs and 2) to improve the utility of features already included within the 1524. The resultant block diagram for the SG1525A is shown in figure 2. Two general comments should be made relative to the overall block

diagram. First, in optimizing the output stage for bi-directional, low impedance switching, commitments had to be made as to whether the output should be high or low during the active, or ON state. Since this is application defined there are needs for both output states, so both were developed with the SG1525A device defined by an output configuration which is high during the ON pulse, and the SG1527A configured to remain high during the OFF state. This difference is implemented by a mask option which eliminates inverter Q₄ (see figure 3) for the SG1527A. In all other respects, the 1525A and 1527A are identical and any description of the 1525A characteristics apply equally to the 1527A. Second, a major difference between this new controller and the earlier 1524 is the deletion of the current limit amplifier. There are so many system considerations in providing current control that it is preferable to leave this as a user-defined external option and allocate the package pins to other, more universally requested functions. Current limiting possibilities are discussed further under shutdown options.

Figure 2 : The SG1525A family represents a "second generation" of IC controllers.

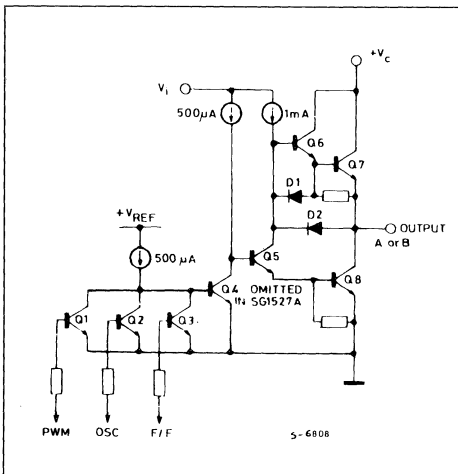


"TOTEM-POLE" OUTPUT STAGE

One of the most significant benefits in using the SG1525A is its output configuration. For the first time it has been recognized in an IC controller that it is more difficult to turn a power switch off than turn it on. With the SG1525A, a high-current, fast transition, low impedance drive is provided for both turn-on and turn-off of an external power transistor or Power MOS. The circuit schematic of one of the two output stages contained within the device is shown in figure 3. This is a two-state output, either Q₈ is on, forming a low saturation voltage pull-down, or Q₇ is on, pulling the output up to V_C. Note that V_C is a separate terminal from the V_I supply to the rest of the device.

This offers the benefits of potentially operating the output drive from a lower supply than the rest of the circuit for power efficiencies, decoupling of drive transients from more sensitive circuits, and a third terminal for extracting a drive signal. Note that even though V_C can be set either higher or lower than V_i , the output cannot rise higher than approximately $1\frac{1}{2}$ volts below V_i .

Figure 3: One of Two Power Output Stages Contained within the SG1525A which Conduct Alternately due to the Internal Flip-flop.

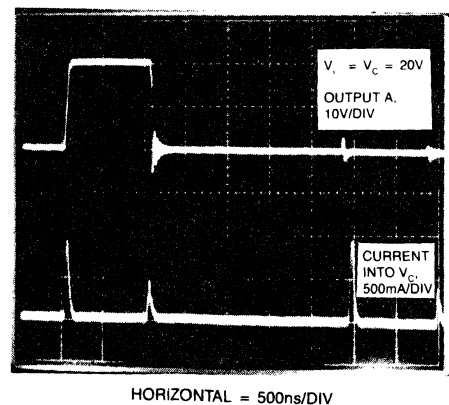


During the transition between states, there is a slight conduction overlap between source and sink which results in a pulse of current flowing from V_C to ground. However, due to the high-speed design configuration of this stage, this current spike lasts for only about 100ns. A typical current waveform at

V_C is shown in figure 4. This transient will normally be decoupled from the rest of the control power by a 0.1 μ F capacitor from V_C to ground but it should not, otherwise, cause a problem unless very high frequency operation is contemplated where it will contribute to overall device power dissipation, by becoming a significant portion of the total duty cycle.

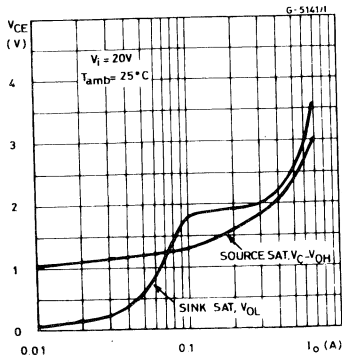
The output saturation characteristics of this stage are shown in figure 5. The source transistor, Q_7 is a straight forward Darlington and its saturation voltage remains between 1 and 2 V out to 400 mA under the assumption that $V_i \geq V_{CC}$. The sink transistor, Q_8 , however, has a non-uniform characteristic which needs explanation. At low sink currents, the 1 mA current source through Q_5 insures a very low saturation voltage at the output. As load current increases past 50 mA, Q_8 begins to come out of saturation for lack of base drive but only up to about 2 V. Here diode D_2 becomes forward biased shunting a portion of the load current through Q_5 to boost the base current into Q_8 . With this circuit, the sink transistor can both support high peak discharge currents from a capacitive load, as well as insure the low static hold-off voltage required for bipolar transistors.

Figure 4 : Current "spiking" on the V_C terminal caused by conduction overlap between source and sink is minimized by high-speed design techniques.



A typical output configuration for a push-pull bipolar transistor power stage is shown in fig. 6. With a steady state base drive current from the SG1525A of 100 mA, this stage should be able to switch 1 to 5 A of transformer primary current, depending upon the choice of transistors. The sum of R_1 and R_2

Figure 5 : The output saturation characteristics of the SG1525A provide both high drive current an low hold-off voltage.



determine the maximum steady state output current of the SG1525A while their ratio defines the voltage across C₂ which, at turn off, becomes the reverse V_{BE} for Q₁. With the values given, the output current and voltage waveforms are shown in figure 7 for a one microsecond pulse. If power MOS are used for the output switches as shown in figure 8, the interfacing circuitry can become even simpler with only a small series gate resistor potentially required to damp spurious oscillations within the power device.

Figure 6 : A Typical Push-pull Converter Power Stage Using External Bipolar Power Transistor Switches

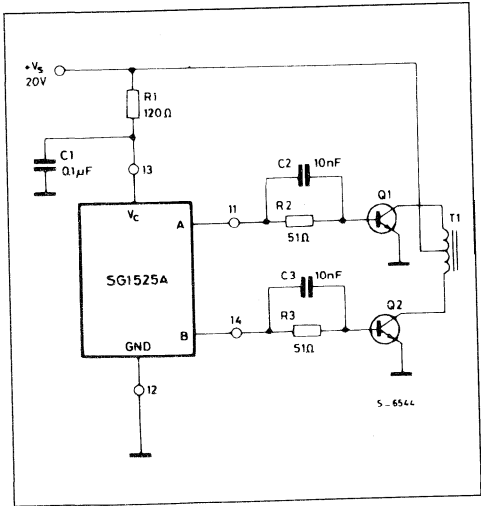
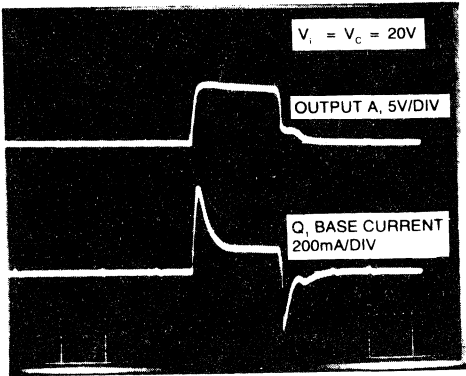


Figure 7 : Base current waveforms (figure 6 circuit) show the enhanced turn-on and turn-off current possible with the SG1525A.



HORIZONTAL = 500ns/DIV

Push-pull direct transformer drive is also particularly advantageous with SG1525A as shown in figure 9. A version of this configuration is required for isolation when the control circuit is referenced to the secondary side of an off-line power system, and to provide level shifting of drive signals for bridge and full bridge switching. The configuration of figure 9 has a couple of important advantages. First, by connecting the drive transformer primary directly between the outputs of the SG1525A, no center-tap is needed and the full primary is driven with opposite polarities. Secondly, between each output pulse, both outputs are pulled to ground which effectively shorts the two ends of the primary winding together coupling a low-impedance turn-off signal to the switching transistors.

A useful single-ended configuration, typical of buck regulators, is shown in figure 10. Here the SG1525A outputs are grounded and the PWM signal is taken from the V_c terminal which switches close to ground during each clock period as the internal source transistors are alternately sequenced.

Figure 8 : Replacing bipolar transistors with power MOS provides even greater simplicity due to the low driving impedances of the SG1525A in each transition.

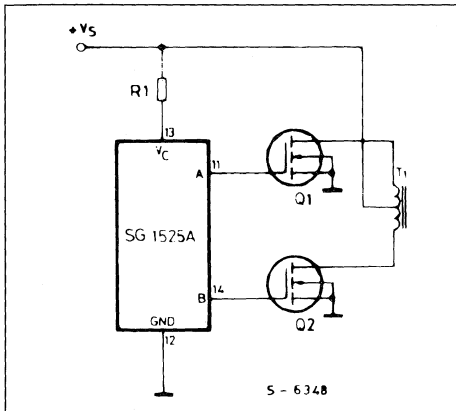


Figure 9 : The SG1525A is ideally suited for driving a low-power base drive transformer and eliminates the need for a primary center-tap.

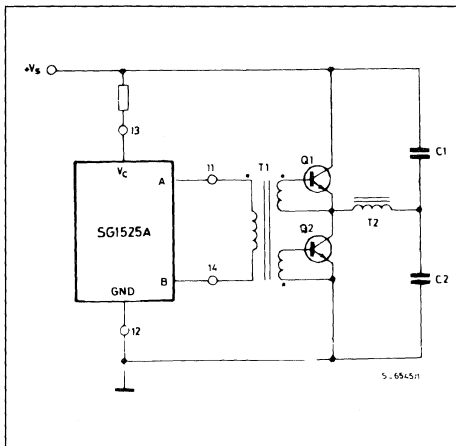
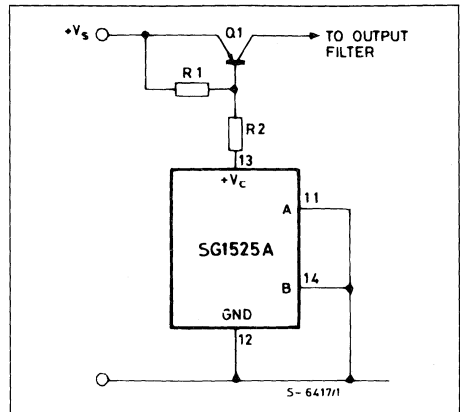


Figure 10 : A single-ended Ground-referenced Power Stage for a Flyback or Boost Regulator.



CONTROLLING POWER SUPPLY START-UP

Although the advantages of the SG1525A's output stage will often be reason enough for its selection, there are several other important and useful features incorporated within this product. One problem previously overlooked in PWM circuits is keeping the output under control as the supply voltage is turned on and off. Undefined states, particularly the possibility of turning on an output before the oscillator is running, can be quite awkward, if not catastrophic. To prevent this, the SG1525A has incorporated an under-voltage lockout circuit which effectively clamps the outputs to the off state with as little as 2 1/2 V of supply voltage which is less than the voltage required to turn the outputs on. This clamp is maintained until the supply reaches approximately 8 V insuring that all the remaining SG1525A circuitry is fully operational prior to enabling the outputs. The clamp reactivates when the supply is lowered to approximately 7.5 V. There is about 500 mV of hysteresis built in to eliminate clamp oscillation at threshold.

Another important aspect of power sequencing is restraining the outputs from immediately commanding a 100 % duty cycle when they are activated. This is accomplished by a slow turn on (soft-start) which is defined by an internal 50 μA current source in conjunction with an externally applied capacitor. The details of this power sequencing system are shown in figure 11.

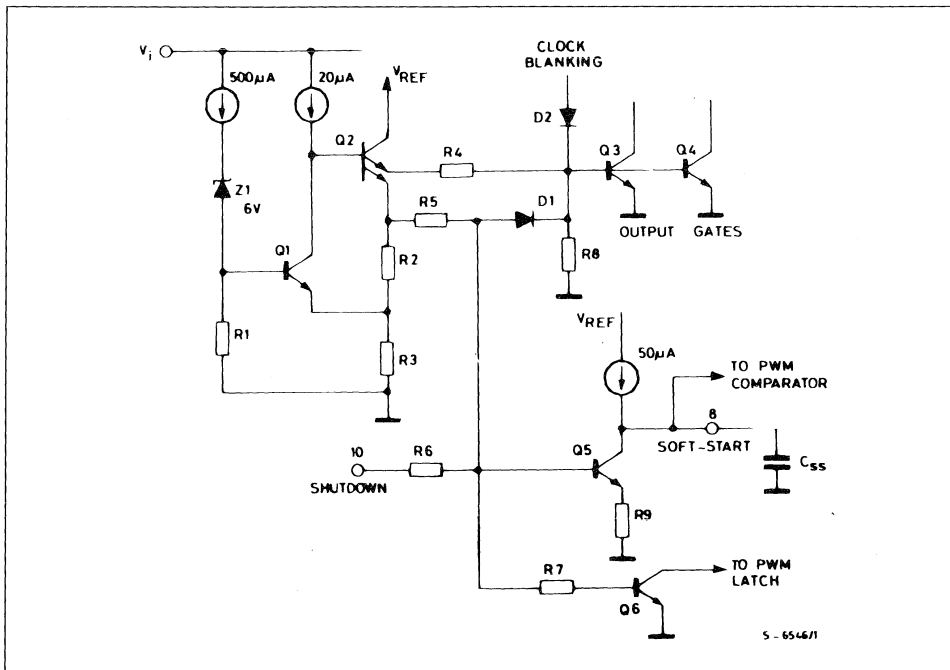
Q₃ and Q₄ are the output gates normally driven by the oscillator through D₂ to provide output blanking between pulses. (One of these transistors is shown as Q₂ in figure 3). At low supply voltages, Q₂ conducts with base drive from the 20 μA current source. Q₂ provides three functions. First, current through R₄ acti-

vates the output gates with minimum voltage drop. Second, current through R₅ activates the shutdown transistor Q₅ holding the soft-start capacitor, C_{SS}, discharged. Third, R₂ provides a small bucking voltage across R₃ for hysteresis at the switch point.

When the input voltage becomes high enough to provide a little more than one volt at the base of Q₁, that transistor turns on. This turns off Q₂, activating the outputs and allowing C_{SS} to begin to charge from the internal 50 μA current source. The time to reach approximately 50 % duty cycle will be

$$t = \left(\frac{2 \text{ volts}}{50 \mu\text{A}} \right) C_{SS}$$

Figure 11 : The Internal Power Turn-on, Soft-start, and Shutdown Circuitry of the SG1525A.



POWER SUPPLY SHUTDOWN

An important part of any PWM controller is the ability to shut it down at any time for a variety of reasons, including system sequencing requirements or fault protection. Several options are available to the user of the SG1525A, which require an understanding of the capability of the shutdown terminal, pin 10. Referring to figure 11, the base of Q₅ is turned on by a signal which is clamped to approximately 1.4 V by the action of D₁ and the V_{BE} of gates Q₃ and Q₄.

This holds the outputs off and keeps C_{SS} discharged by Q₅ which, with R₉, becomes a 100 μA net current sink.

If, during normal operation, pin 10 is pulled high, three things happen. First, the outputs are turned off within 200 ns through D₁. Second, the PWM latch is set by Q₆ so that even if the signal at pin 10 were to disappear, the outputs would stay off for the duration of that period, being reset by the next clock pulse. Third, Q₅ is activated commencing a 100 μA

discharge of C_{SS} . However, if the activation pulse on pin 10 has a duration shorter than 1/3 of the clock period, the voltage on C_{SS} will remain high and soft-start will not be reactivated. Naturally, a fixed signal on pin 10 will eventually discharge C_{SS} , recycling soft-start.

Thus, the shutdown pin provides both sequencing capability as well as a convenient port for protective functions, including pulse-by-pulse current limiting.

REGULATING PWM PERFORMANCE IMPROVEMENTS

The SG1525A also offers significant performance and application improvements in almost all of the additional basic functions of a PWM over those obtainable with earlier devices. A general description of these features is outlined below :

REFERENCE REGULATOR

The output voltage of this regulator is internally trimmed to $5.1 \text{ V} \pm 1\%$ during manufacture, eliminating the need for adjusting potentiometers in most applications.

ERROR AMPLIFIER

SG1525A uses the same basic transconductance amplifier as the SG1524 with an important difference : it is powered by V_I rather than V_{REF} . Now the input common-mode range includes V_{REF} eliminating the need for a voltage divider with its attendant tolerances. An additional feature relative to the error amplifier is that the shutdown circuitry feeds into a separate input to the PWM comparator allowing pulse termination without affecting the output of the error amplifier which might have a slow recovery, depending upon the external compensation network selected. An important benefit of a transconductance amplifier is the ease with which its current mode output can be over-ridden by other external controlling signals.

PWM COMPARATOR

The significant benefit of the SG1525A's PWM comparator is in its following latch. A common problem with earlier devices was that any noise or ringing on the output of the error amplifier would affect multiple crossings of the oscillator ramp signal resulting in multiple pulsing at the comparator's output. The SG1525A's latch terminates the output pulse with the first signal from the comparator, insuring that there can be only a single pulse per period, removing all jitter or threshold oscillation from the system. Another important advantage of this latch is the ability to easily implement digital or pulse-by-pulse

current limiting by merely momentarily activating the shutdown circuitry within the SG1525A. This could be as simple as connecting pin 10 to a ground-referenced current sensing resistor. For greater accuracy, some added gain may be advantageous. Once a current signal causes shutdown, the output will remain terminated for the duration of the period, even though the current signal is now gone. An oscillator clock signal resets the latch to start each period anew.

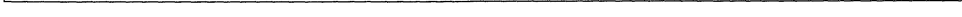
OSCILLATOR

The functions of the oscillator within the SG1525A have been broadened in two important aspects. One is the addition of a synchronization terminal, pin 3, allowing much easier interfacing to an external clock signal or to synchronize multiple SG1525A's together. The other is the separation of the oscillator's discharge network from its charging current source for deadtime control. Reference should be made to the schematic of figure 12 for an understanding of the operation of this circuit. The heart of this oscillator is a double-threshold comparator, Q_7 and Q_8 , which allows the timing capacitor to charge to an upper threshold by means of the current source defined by R_T and mirrored by Q_1 and Q_2 . The comparator then switches to a lower threshold by turning on Q_{10} and discharges C_T through Q_3 and Q_4 with a rate defined by R_D . As long as C_T is discharging, the clock output is high, blanking the outputs.

Since the overall oscillator frequency is defined by the sum of the charge and discharge times, there are three elements now in the frequency equation which is approximately :

$$f \approx \frac{1}{C_T (.07 R_T + 3 R_D)}$$

External synchronization can easily be accomplished with a 2.8 V positive pulse at pin 3. This will turn on Q_9 , lowering the comparator threshold below wherever the voltage on C_T may happen to be. Two factors should be considered : First, the voltage on C_T determines the amplitude of the PWM ramp, and if the sync occurs too early, the loop gain will be higher and the resolution may be worse. Second, the sync circuit is regenerative within 200 ns ; and, while a wider pulse can be used, C_T will not begin to recharge as long as the sync pin is high. For synchronizing multiple SG1525A devices together, one need only to define a master with the correct $R_T C_T$ time constant, connect its output pin to the slave sync pins, and set each slave $R_T C_T$ for a time constant 10-20 % longer than the master.



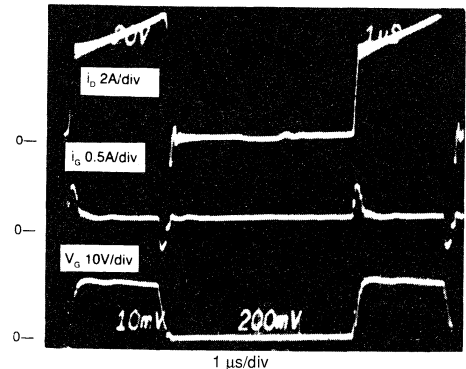


A 200 WATT, OFF-LINE, FORWARD CONVERTER

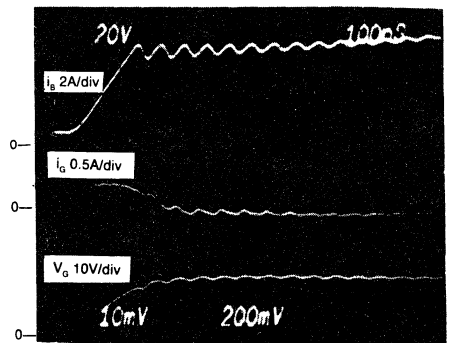
The ease of interfacing the SG1525A into a practical power supply system can be illustrated by the off-line, power converter shown in figure 13. This 200 W supply places the control circuitry on the primary side of the power transformer where direct coupling can be used to drive the power switch. While simplifying the drive electronics, this configuration usually requires an isolated voltage feedback signal which is most easily accomplished by an optocoupler driven by some type of voltage regulator IC such as a L123 or LM723. One other undefined block in figure 13 is the auxiliary power supply which supplies the low voltage, low current bias supply for the SG1525A and the drive for Q_1 the power switch. The choice of the SGSP479 power MOS for this switch keeps the total power requirements from the auxiliary supply at less than 1 W ; readily implemented with a small, line-driven transformer.

This converter is designed to operate at 150 kHz which is accomplished by running the SG1525A at 300 kHz and using only one of the outputs. This also automatically insures that the duty cycle can never be greater than 50 %, a requirement of the power transformer in this configuration. The high operating frequency allows the output filter's roll-off to be set at 12 kHz, greatly simplifying the overall loop stability considerations as adequate response can be achieved with only the single-pole compensation of the error amplifier provided by the 0.05 μ F capacitor on pin 9. The totem-pole output of the SG1525A is used to advantage to drive Q_1 by providing a 400 mA peak current to charge and discharge the power MOS gate capacitance while keeping overall power dissipation low. Waveform photographs of this operation are shown in figure 14.

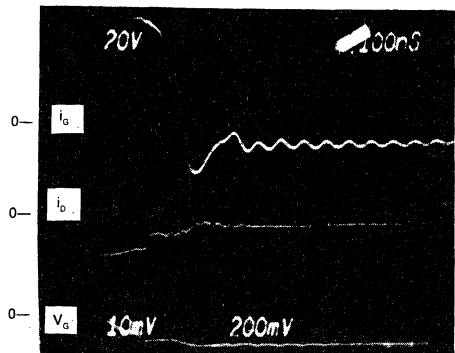
Figure 14 : Current and Voltage Waveforms for the 200 W Off-line Forward Converter with a SG1525A Direct Driven Power MOS Switch (operating frequency is 150 KHz with output current equal to 40 A).



a) Waveforms of I_b , I_g , V_g



b) Risetime
= 90 ns



c) Falltime
= 30 ns

APPLICATION NOTE

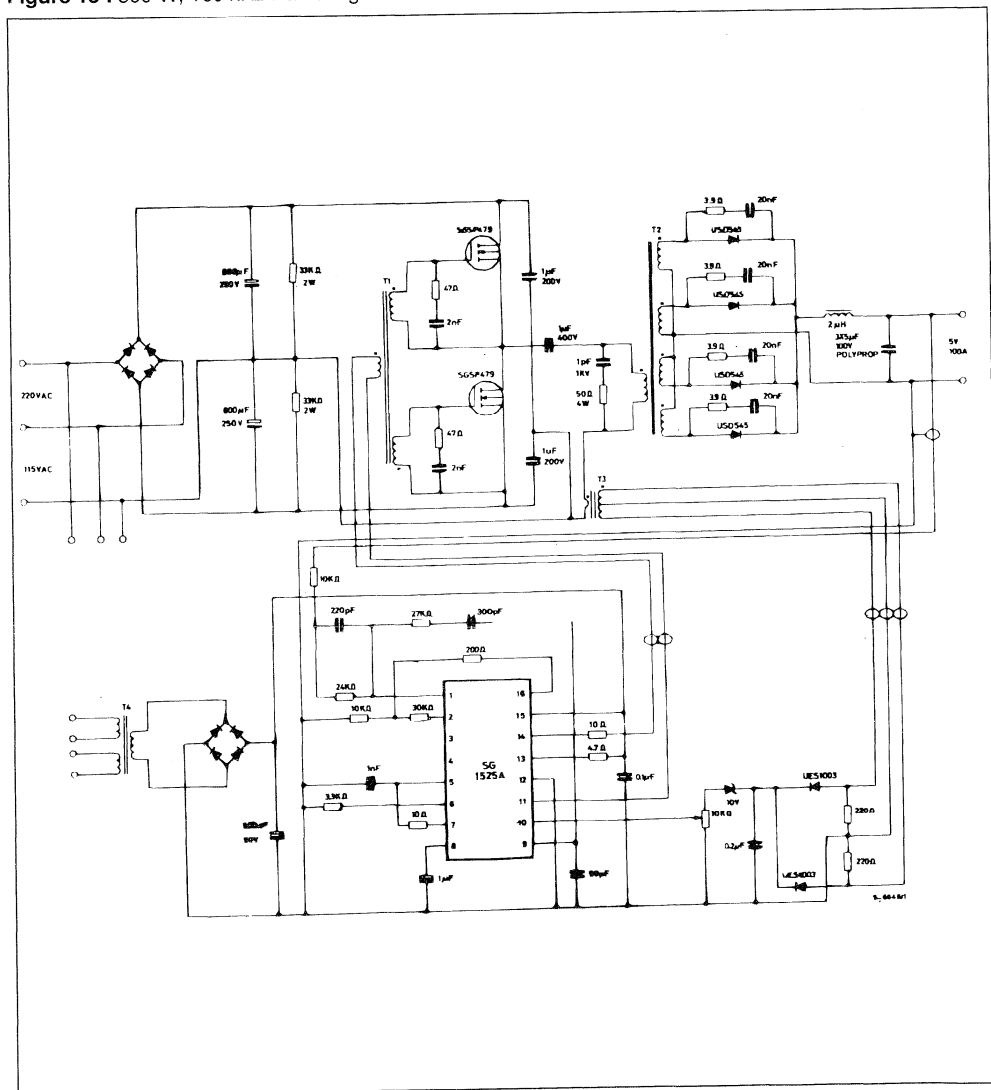
When operating at full load, the efficiency of this converter is 73 % with by far the greatest power losses occurring in the output rectifiers—even though Schottky devices have been selected.

Switching losses have been minimized by the fast current transitions, primarily defined by the leakage inductance of the transformer. Although this switching time could probably be even further reduced, there could be problems with current spikes during

rise time due to Schottky rectifier capacitance.

Current limiting for this converter is provided by measuring the current in SGSP479 with the 0.1 Ω resistor in series with the source and using this voltage to activate the shutdown circuitry within the SG1525A. While this will provide a fast-acting short circuit protection on a pulse-by-pulse basis, a comparator may need to be added for a more accurate current limit threshold.

Figure 15 : 500 W, 100 kHz Half-bridge Schematic.



Transformer winding data

500 W, 100 kHz, Off-Line, Half-Bridge Converter :

- T1 Core : Ferrox 486T250-3C8
Pri : 14 T #22AWG
Sec (2) : 7 T #22AWG
- T2 Core : Ferrox EC52-3C8 (EE)
Pri : 14 T, 2 layers, 2 #16AWG in parallel
Sec (2) : each 2 T, C.T., copper strap
0.01" x 0.8"
- T3 Core : Ferrox 486T250-3C8
Pri : 1 T
Sec : 20 T, C.T. #22AWG
- T4 117 V/220 V, 25 V, 0.15 A, 50-60 Hz
- L1 Core : Ferrox IF30-3C8
4 turns, 5 #12AWG in parallel

500 WATT, OFF-LINE, HALF-BRIDGE CONVERTER

The circuit shown in figure 15 uses a pair of SGSP479 power MOS in a half-bridge configuration with the SG1525A chip referenced to the secondary side of the power transformer.

The power MOS gates are driven directly from the control chip output through step down and isolation transformer T1. The SG1525A output terminals (pins 11 and 14) provide active pull-up and pull-down (dual source/sink for the primary of T1. This provides the fast, high current turn-on and turn-off pulses needed for the power MOS gates. In addition, the two ends of the primary windings are shorted to ground during deadtime, which prevents accidental turn-on by transients. Note that the current supplied by the SG1525A outputs drops to a small value when the gate capacitance has been charged or discharged to the desired gate voltage. Damping resistors with series blocking capacitors across the two secondaries of T1 minimize ringing due to the power MOS gate capacitance and the inductance of T1 and lead inductance, particularly during deadtime.

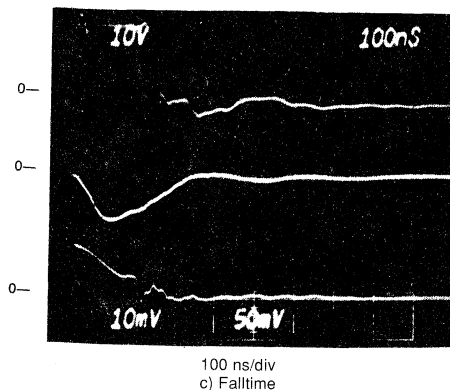
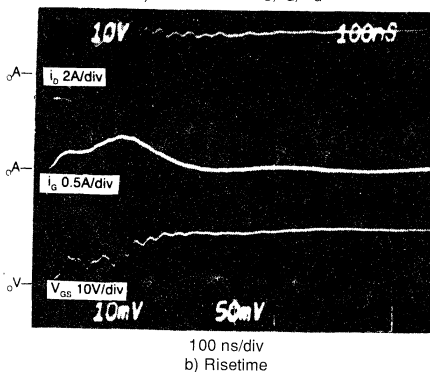
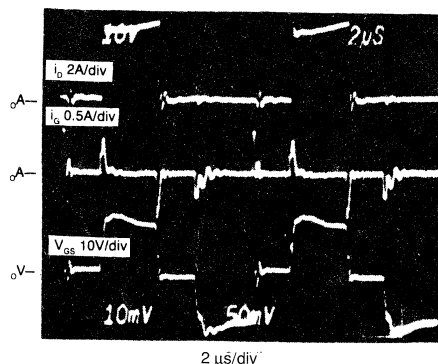
Deadtime for the SG1525A is set very simply by a single resistor between pins 5 and 7. Only a small amount of deadtime is needed since the power MOS have no storage time and a very short delay time.

Slow turn-on is accomplished by a single capacitor at pin 8.

Current limiting is provided by current transformer T3 in series with the primary of the power transformer T2. The signal is rectified, threshold adjusted and sent to the shutdown terminal, pin 10, of the SG1525A.

Waveforms of the converter are shown in the scope photos of figure 16. Current rise and fall times are 20 ns and 10 ns.

Figure 16 : Performance Waveforms for the Half-bridge, 500 W, 100 kHz Converter with Output Current of 80 A.



IMPROVED PERFORMANCE ; LESS COMPLEXITY

Although power supply designers for some time now have had an ever widening inventory of IC components available to ease their design tasks, the final measure of improvement has to be in terms of system performance versus cost. With fewer interface components to the power stages, freedom from potentiometer adjustments, protected start-up and shut-down, a built in soft-start network and several additional system-level features, the SG1525A pro-

vides a significant contribution to both performance and costs while simultaneously making the designer's task easier. With these accomplishments, it is clear that this device truly does represent a step-function improvement, introducing a second-generation of power control components.

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250W OFF-LINE FORWARD CONVERTER

This paper gives a practical example of the design of an off-line switching power supply with forward converter topology. Topics include transformer and filter inductor design, proportional base drive, component selection, output filter design and closing the control loop using the new UC1524A control circuit.

POWER SUPPLY SPECIFICATIONS :

Topology : Forward Converter with Proportional Base drive

Line input : 117V $\pm$ 15% (99-135V), 60Hz
 230V $\pm$ 15% (195-265V), 50Hz

Output : Voltage : 5V
 Current : 5 to 50A
 Current Limit : 60A short circuit
 Ripple Voltage : 100mV P-P max.
 Line Regulation : $\pm$ 1%
 Load Regulation : $\pm$ 1%

Other Features :

- EFFICIENCY : 75%
- LINE ISOLATION : 3750V
- SWITCHING FREQUENCY : 40kHz

THE COMPLETE POWER SUPPLY CIRCUIT

The complete 250W switching power supply schematic is given in figure 2. This supply meets all of the specification requirements defined on this page.

LINE INPUT AC TO DC CONVERSION

The input rectifier/filter section converts the AC line voltage into a crudely filtered and unregulated DC voltage, V_{in} , which powers the downstream switching regulator. The input section is configured as a full-wave bridge when operating from the 230V line, and as a voltage doubler when operated from 117V. This provides approximately the same V_{in} range (200-380V) for the switching regulator with either

Figure 1 : Block Diagram of the Switching Power Supply.

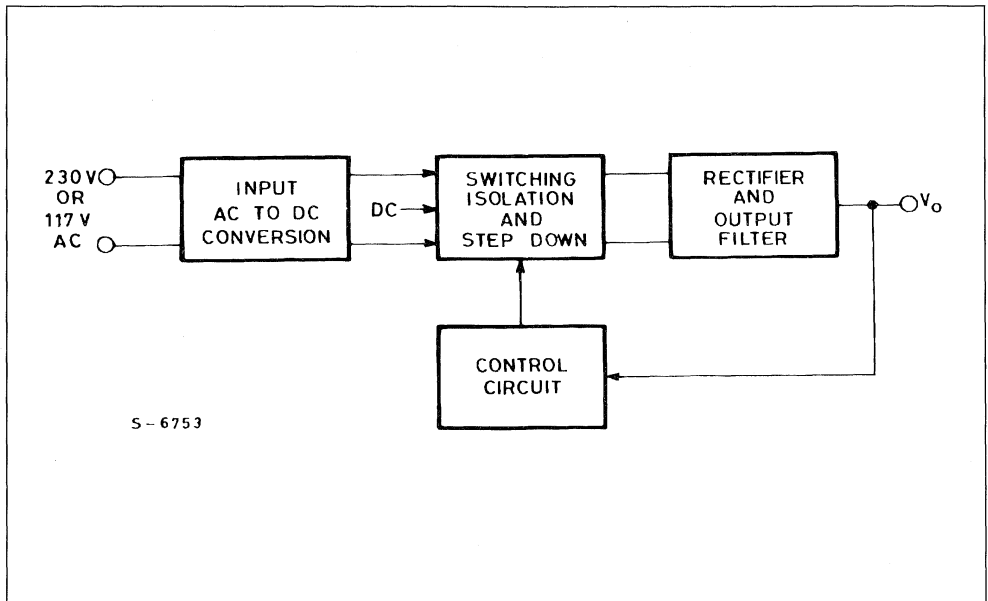
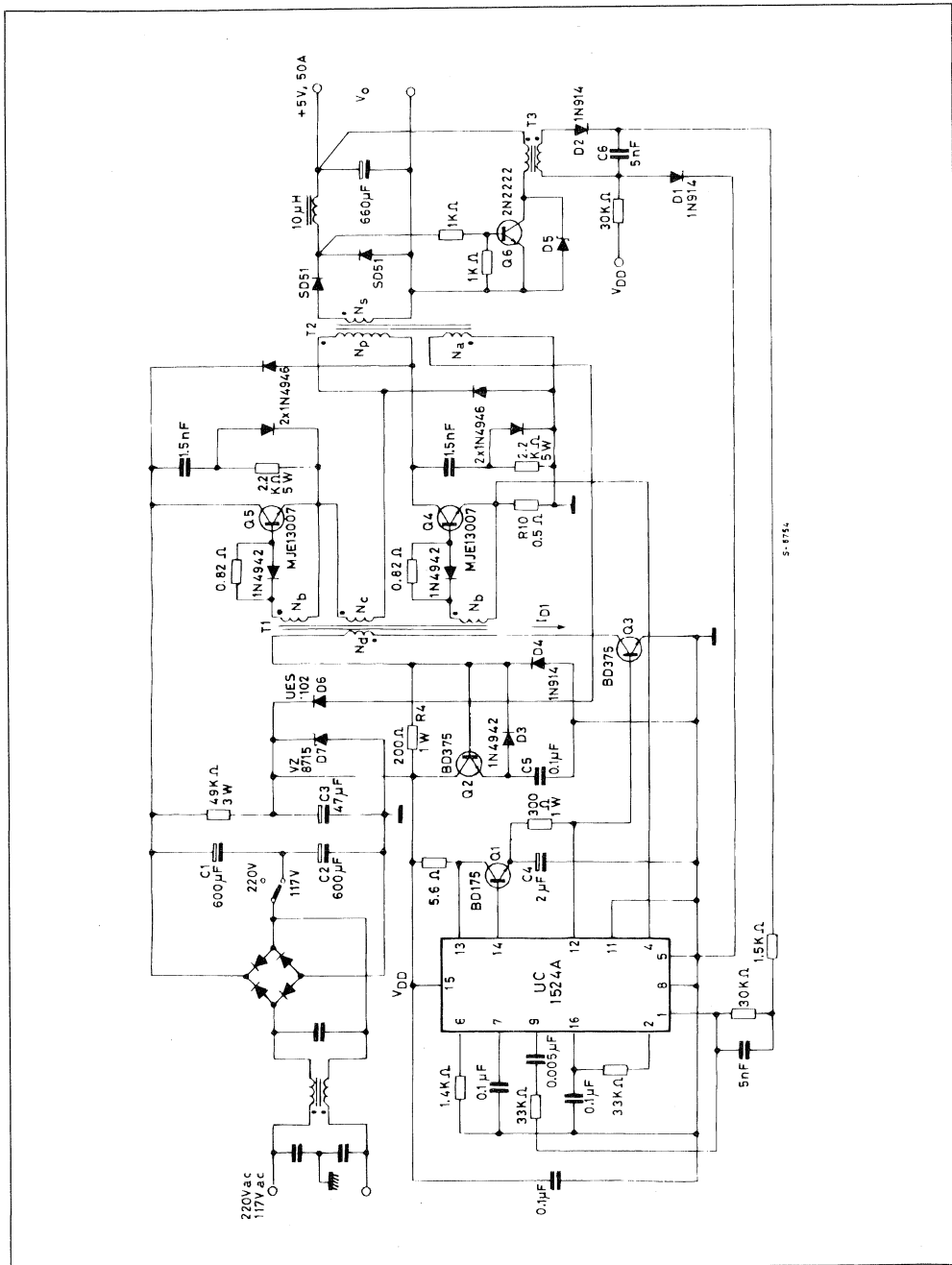


Figure 2 : Complete 250W Switching Power Supply.



S-47754

line voltage. Minimum input voltage, $V_{\min}$, is 200V at low line.

The design of the input section is covered extensively in Appendix B. The power input required in this application equals power output (250W) divided by efficiency (75%), or 333W. Circuit values for this application can be obtained by multiplying the 100W input values given in Table 1 of Appendix B by $P_{in}/100 = 3.33$, using the worst case voltage double configuration :

$$C_1 = C_2 = 3.33 (160) = 533\mu F \text{ (use } 600\mu F) \quad (1)$$

$$I_{chg} = 3.33 (1.126) = 3.75 \text{ A RMS AC} \quad (2)$$

The switching regulator draws 40KHz rectangular current pulses which discharge the input capacitors. Peak discharge current, I_{dis} occurs at $V_{\min}$ when the duty cycle, D, is maximum (50 %) :

$$I_{dis} = P_{in}/(V_{\min}D) = 333/(200 \cdot 0.5) = 3.33 \text{ A peak} \quad (3)$$

The RMS AC component of the discharge current, I_{dis} , which flows through the input capacitors at worst case 50% duty cycle is :

$$I_{dis} = (I_{dis})/2 = 3.33/2 = 1.67 \text{ A RMS AC} \quad (4)$$

The total RMS AC current rating required for the input capacitors is calculated from Equation 6 of Appendix B.

$$I_{CAP} = \sqrt{I_{chg}^2 + I_{dis}^2} = \sqrt{3.75^2 + 1.67^2} \quad (5)$$

SWITCHING CIRCUIT TOPOLOGY

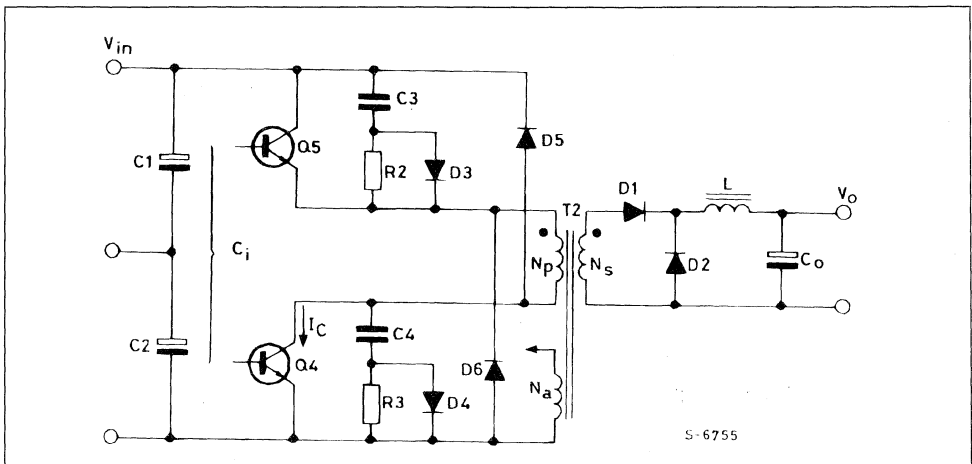
The two transistor forward converter configuration shown in figure 3 was used in this 250W switching power supply for the following reasons :

1. Transistor voltage ratings are half the voltage required in a comparable single transistor circuit (400V vs. 800V). Only 1/4 the silicon chip area is required for the same current rating, and the switching speeds will be twice as fast.
2. The snubber networks are for load line shaping only and are not required to absorb all the energy stored in the transformer leakage reactance. Instead, clamp diodes D5 and D6 conserve most of this energy by returning it to the input, improving the efficiency.
3. Closed-loop stability is easier to achieve than with a flyback converter because there is no right half plane zero.
4. Filter capacitor requirements are much less severe than in boost or flyback converters because of the output filter inductor.
5. Transformer construction is simplified because there is no need for a clamp winding (N_a is used for the auxiliary supply).
6. Reliability is improved because faster transistor dissipates only one half of these reduced losses.

Disadvantages of this topology are :

1. Two transistors are required instead of one (but cost may be less).
2. Restricted to less than 50% duty cycle to permit core reset. This results in poorer transformer utilization.
3. Added cost of filter inductor, which is not required for the flyback converter.

Figure 3 : Two Transistors Forward Converter.



SPECIFYING THE SWITCHING TRANSISTORS

Maximum peak primary current flowing through the transistors, I_{CM} , is the same as I_{dis} from Equation 3 or 3.33 A.

The transistors should have good $V_{CE(sat)}$ and switching speeds at a collector current of at least 4.0A, which includes an allowance for unusual conditions such as short circuit current. (Disregard spec sheet "maximum current ratings" which are inflated for competitive marketing reasons, and focus on the specified test conditions).

The collector voltage rating must be greater than maximum V_{in} , or 380V in this application. Conservatively, this should be the BV_{CEO} rating, but with careful load line shaping to make certain the transistor is completely off before voltage is applied, a less conservative designer might specify BV_{CEX} greater than $V_{in(max)}$.

The MJE13007 satisfies the above requirements, with BV_{CEO} of 400V, $V_{CE(sat)}$ less than 2.0V at 5A, and worst case fall time of 400 ns under the proportional base drive conditions provided.

SNUBBER NETWORK DESIGN

The turn-off snubber networks shown across each transistor in figure 3 provide shaping of the load line to ensure that it remains below the reverse bias safe operating area (RBSOA) of the transistors. Capacitors C_3 and C_4 accomplish this by holding the voltage across each transistor low during current turn-off. The snubber capacitors thus absorb the turn-off transition energy that otherwise would have been dissipated in the transistors (see figure 4).

$$C_3 = C_4 = \frac{I_{CM} t_f}{2V_{in(max)}} = \frac{3.33 \times 4 \times 10^{-6}}{2 \times 380} \quad (6)$$

$$= .00175\mu F \text{ (use .0015mF)}$$

Resistors R_2 and R_3 are designed to discharge the snubber capacitors with a discharge time constant of one-half the minimum on time, $t_{on(min)}$.

$$t_{on(min)} = \frac{D_{(max)} V_{in(min)}}{f V_{in(max)}} = \frac{0.5 \cdot 200}{40.000 \cdot 380} = 6.58\mu s \quad (7)$$

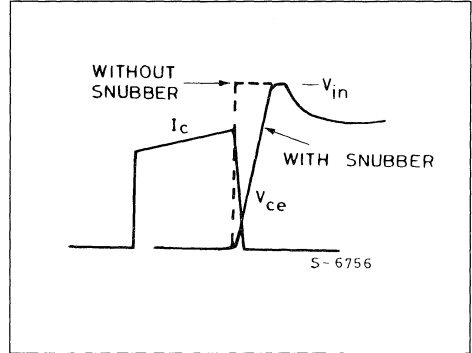
$$R_2 = R_3 = \frac{t_{on(min)}}{2C_3} = \frac{6.58 \times 10^{-6}}{2 \times 1.5 \times 10^{-9}} = 2.2K\Omega$$

Maximum power dissipation in each resistor :

$$P_{R2} = P_{R3} = \frac{1}{2} C_2 V_{in(max)}^2 f \quad (8)$$

$$= \frac{1.5 \times 10^{-9}}{2} \times 380^2 \times 40.000 = 4.3W$$

Figure 4 : Effected of Snubber Network on Turn-off Characteristics.



POWER TRANSFORMER DESIGN

The design of the 40KHz inverter transformer is detailed in Appendix A. A primary to secondary turns ratio of 148/9, or 15.33, ensures that 5V output is provided with minimum V_{in} of 200V at 50% duty cycle, including voltage drops in rectifiers, transistors and windings.

Transformer winding N_a is used to provide an auxiliary supply to power the control and base drive circuits. This makes good use of the energy stored in the transformer primary inductance.

OUTPUT FILTER DESIGN

The output filter and its associated waveforms are shown in Figure 5. The filter inductor calculation is based on the maximum "off" time :

$$D_{(min)} = D_{(max)} \frac{V_{in(min)}}{V_{in(max)}} = 0.5 \frac{200}{380} = 0.263 \quad (9)$$

$$t_{off(max)} = \frac{1 - D_{(min)}}{f} = \frac{1 - 0.263}{40.000} = 18.4\mu s$$

The inductance required to prevent discontinuous mode operation depends upon the minimum load current :

$$\Delta I_L(\max) = 2I_{o(\min)} = 2 \times 5 = 10A \quad (11)$$

$$L = \frac{(V_o + V_F) t_{off(\max)}}{\Delta I_L(\max)} = \frac{(5 + 0.6) 18.35}{10} = 10\mu H \quad (12)$$

The capacitance required to achieve the output ripple specification of 0.1V is :

$$C_o = \frac{1}{2} \frac{\Delta I_L(\max)}{2} \frac{1}{2f} \frac{1}{V_o} = \frac{10}{8 \times 40.000 \times 0.1} = 312\mu F \quad (13)$$

The maximum ESR of the capacitor is :

$$ESR = V_o / \Delta I_L(\max) = 0.1/10 = 0.01\Omega \quad (14)$$

To obtain the necessary ESR requires a capacitor much larger than the 312μF calculated. This design will use three 220μF solid tantalum capacitors, Mallory THF227MO10P1G, in parallel. A single 14.000μF aluminium electrolytic capacitor, Mallory CG0143M10R2C3PL could also be used.

With the tantalum capacitor, the resonant frequency of the filter is 2KHz. With the aluminium electrolytic, the resonant frequency is reduced to 425Hz, changing the closed-loop design.

CLOSING THE CONTROL LOOP

The UC1524A is used for the control circuit. It has additional features such as pulse by pulse current limiting and high current and voltage output capability (200mA, 60V) compared with the SG1524. The UC1524A reference is trimmed to ± 1% which makes it possible to avoid using a voltage-setting potentiometer in many instances.

The control to input transfer function, dV_o/dV_c , shown in Figure 6, includes the cascaded gain of the sawtooth modulator within the UC1524A control IC, the power switching circuit, and the output filter characteristics, $H_e(s)$.

In the control IC, a control voltage V_c is compared with sawtooth ramp voltage V_s (2.5V) to establish the drive pulse width to the power switches. For the forward converter, only one of the two alternating outputs of the UC1524A is used so as to limit the duty cycle to 50% maximum and allow for transformer core reset :

$$D = 0.5 V_c / V_s = 0.5 V_c / 2.5 = V_c / 5 \quad (15)$$

The forward converter is a member of the buck regulator family. Transformer turns ratio $n = 16.44$:

$$V_o = \frac{V_{in}}{n} D = \frac{V_{in} V_c}{n 2V_s} \quad (16)$$

The low frequency control to output transfer characteristic is obtained by differentiating with respect to V_c :

$$\frac{dV_o}{dV_c} = \frac{V_{in}}{n 2V_s} = \frac{380}{15.33 \times 5} = 4.95 = 13.2db \quad (17)$$

Note that gain is greatest at maximum V_{in} . The overall control to output transfer characteristics including the filter is :

$$\frac{dV_o}{dV_c} = \frac{V_{in}}{n 2V_s} = H_e(s) \quad (18)$$

Figure 5 : Output Power Filter Design.

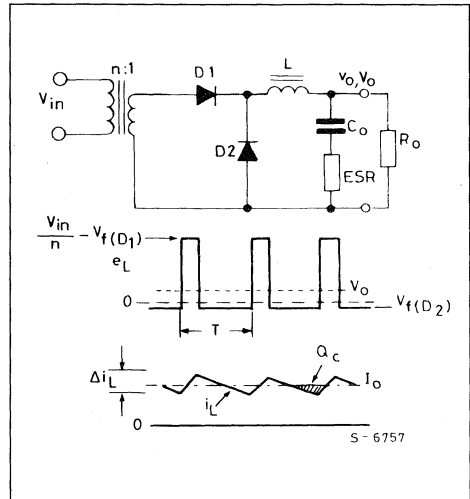
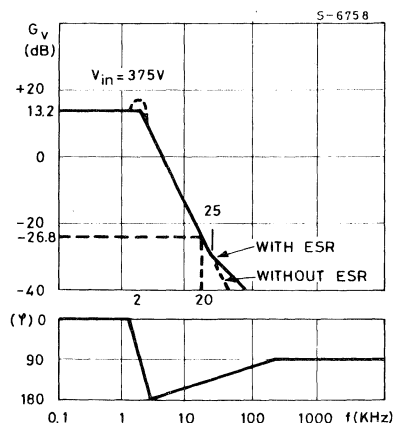


Figure 6 : Control to Output Transfer Function LC Filter and Modulator.



The filter introduces a two-pole characteristic at its resonant frequency (2kHz). Above resonance, the gain drops 40db per decade, and the phase shift becomes - 180 degrees. Combined with the - 180 degrees phase shift of the feedback network, this will cause instability and oscillations unless compensated.

Closing the loop involves feeding back the error voltage from the output terminal of the supply ($\hat{V}_o$) to the IC control voltage port ($\hat{V}_c$) through the UC1524A error amplifier. The approach taken is to make the gain of the feedback network such that the overall loop gain crosses zero db (with adequate phase margin) at one half the switching frequency.

As shown in figure 6, control to output gain is 13.2db at low frequencies, rolling off above 2KHz at -40db per decade, so that at 20KHz the control to output gain is 13.2 - 40, or 26.8db. For overall loop gain of zero, the feedback network gain must be made + 26.8dB at 20KHz.

From 20KHz down to 2KHz, there is a net single zero in the feedback network which cancels one of the two filter poles and reduces the phase shift in this region to - 270 degrees.

Below the filter resonant frequency the two filter poles are gone. However, the resonant frequency may be less than 2KHz because of plus tolerances on the filter capacitor. The feedback network is therefore designed to transition from a net single zero to a single pole at 1KHz, half the resonant frequency.

Figure 7 : Open Loop Gain and Phase Plot.

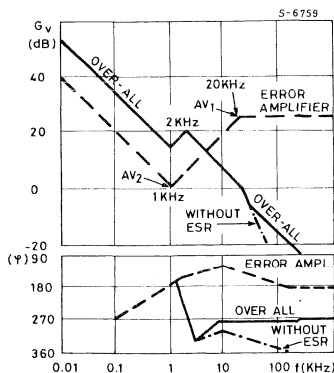


Figure 8 : Error Amplifier with Compensation.

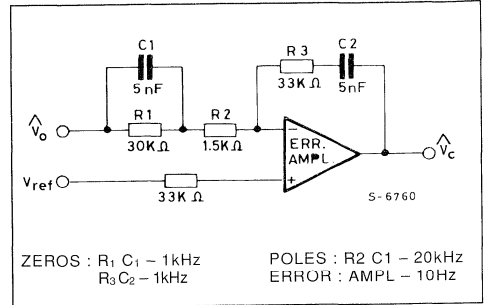


Figure 7 shows the gain and phase plot of the error amplifier and the overall feedback loop. Figure 8 shows the specific feedback network used to achieve this result.

The high frequency error amplifier gain is set by R_2 and R_3 . An R_3 value of 33K is chosen to minimize amplifier loading :

$$Av_1 = R_3/R_2 = 26.8\text{db} = 21.9 \quad (19)$$

$$R_2 = R_3/Av_1 = 33000/21.9 = 1500\Omega$$

The required error amplifier gain at 1KHz is :

$$Av_2 = Av_1 \times 1\text{KHz}/20\text{KHz} = 21.9 \times 1/20 = 1.095 \text{ (0.8 dB)} \quad (20)$$

The gain at 1KHz is determined by R_1 , R_2 and R_3 :

$$Av_2 = R_3/(R_1 + R_2) = 33\text{K}/(R_1 + 1500) = 1.095 \quad (21)$$

$$R_1 = 28.6\text{K}\Omega \text{ (use } 30\text{K}\Omega)$$

The two zeros at 1KHz which changes the feedback network from a net single zero to single pole are equal to :

$$f_1 = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_3 C_2} = 1\text{kHz} \quad (22)$$

$$C_1 = 5.3\text{nF}, \quad C_2 = 4.8\text{nF}$$

C_1 and R_1 in parallel with R_2 result in an additional pole at 20KHz. This flattens the error amplifier gain above 20KHz. The overall phase shift will gradually increase toward 360 degrees, but it doesn't matter because the overall gain is less than one.

An additional pole occurs below 10Hz. This is the inherent single-pole characteristic of the error amplifier's 5M Ω output impedance loaded by feedback capacitor C_2 .

PROPORTIONAL BASE DRIVE

In figure 2, transistors Q₂ and Q₃ and base drive transformer T₁ provide proportional drive to the bases of power switching transistors Q₄ and Q₅. The proportional base drive technique provides excellent performance from high voltage bipolar transistors. It provides large base current pulses for fast turn-on and turn-off, but with modest drive power requirements. Sustaining base drive is provided regeneratively from a collector current winding on the drive transformer. The transistors are never overdriven, even under light load conditions, since the sustaining base drive is proportional to the collector current. Design considerations for the proportional base drive technique are given in Appendix C.

Referring to the circuit of figure 2, when Q₃ is on, R₄ establishes 75mA magnetizing current in drive winding N_d of T₁. When Q₃ turns off, the energy stored in T₁ drives 150mA into the base of each transistor. Collector current starting to flow in N_c provides sustaining base drive. With I_C of 3.33A under full load conditions, an additional 667mA of drive is provided to each base.

While Q₃ is off, capacitor C₅ charges through Q₂ in less than 1μs. Then, when Q₃ turns back on, C₅ provides a negative base drive pulse of -1.5A to each transistor, achieving turn-off in less than 1μs.

Drive transformer T₁ has a drive winding inductance of 0.7mH and is designed to saturate at 75mA. High voltage insulation is not required because all windings are on the line side of the supply.

Core : Ferroxcube 1107P-L00-3B7 Pot Core

N_d : 20 turns AWG34 (0.16mm.)

N_b : 5 turns AWG28 x 2 (2 wires, one for each base)

N_c : 2 turns 5 x AWG28 (5 wires paralleled, AWG28 = 0.32mm.).

AUXILIARY POWER SUPPLY

A 15V auxiliary supply powers the control and driver circuits, obtaining its energy from capacitor C₃. Flyback energy is normally provided by T₂ through winding N_a and D₆ to maintain the charge on C₃ every switching cycle. However, at initial power-up it is necessary to provide separate means to activate the V_{dd} supply. Otherwise, the control and driver circuits could not become functional and the supply could not start to switch.

The unique under-voltage lockout feature of the UC1524A facilitates this technique. All of its internal circuits are disabled (except the reference) until the V_{dd} voltage reaches 8V. This holds the standby current to less than 4mA until the 8V threshold is

reached, and permits C₃ to be initially charged through R₁ from the unregulated input. Enough energy is stored in C₃ to operate the control/driver circuits for several switching cycles, until flyback energy from winding N_a can take over and maintain the voltage on C₃.

It is also necessary to eliminate bas drive to Q₃ during initial power-up, otherwise Q₃ will draw current through R₄ which will prevent C₃ from initially charging. This is accomplished by transistor Q₁ which disconnects base drive source capacitor C₄. When the UC1524A becomes active, its second output turns Q₁ on periodically to charge C₄.

The amount of energy stored in the power transformer is twice the drive/control circuit requirements. Excess energy is dumped into 15V zener diode D₇ which establishes the V_{dd} supply voltage at that level. This also provides a constant clamp voltage across the switching transistors, regardless of line voltage. With good coupling between N_a and primary winding N_p, it may be possible to eliminate clamp diodes D₁₂ and D₁₃.

OUTPUT VOLTAGE SENSE AND OVER-CURRENT SENSE

A small, inexpensive transformer, T₃, couples the output voltage to the line side control circuit with high voltage isolation. The transformer is wound on a Ferroxcube 204-T250-3E2A ferrite toroidal core. Primary and secondary windings are both 14 turns 0.2mm.

During the time the power switching transistors are on, Q₆ is on, applying V_o to the primary of T₃. Through D₂, this provides a real-time feedback voltage to the control circuit across C₆. When Q₆ is off, D₅ clamps the flyback voltage to 15V. Core reset is accomplished well before the end of the "off" time, since the "off" time of the forward converter is always more than 50%. All transformer windings then go to 0V, establishing a DC coupling level. D₁ in series with the ground return compensates for the forward voltage drop and temperature coefficient of D₂.

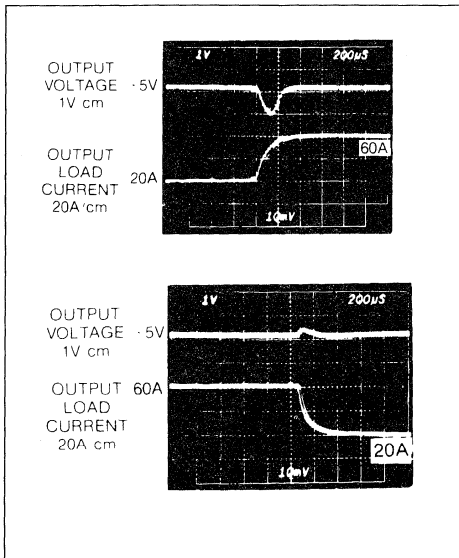
Pulse by pulse current limiting is set by sense resistor R₁₀. Primary current is limited to 4A, corresponding to 62A load current.

Transient response of the switching supply is shown in figure 9 with changes in load from 20A to 60A and back to 20A. This behavior is a large signal phenomenon. It doesn't matter how fast the control loop is, it is temporarily driven into the bounds because the load change is much larger than the output filter inductor current can accommodate in one cycle. Nevertheless, recovery is smooth and there is no evidence of ringing or oscillations, demonstrating the

stability of the control loop. Step changes in load current that are small enough for the control loop to remain functional are barely noticeable at the output.

Transient response can be improved by reducing the filter inductor and increasing the filter capacitor size, but this will increase the minimum load current required to keep the inductor current from becoming discontinuous.

Figure 9 : Step Change in Output Load.



APPENDIX A

DESIGN OF THE POWER TRANSFORMER AND FILTER INDUCTOR

Flux Density Excursion. In this forward converter application, the flux excursion is entirely within the first quadrant of the B-H characteristic, from zero flux density toward saturation. With simple duty cycle control, using the UC1524A control IC, it is possible to have nearly twice the normal Volt-seconds, $V_{in(max)} t_{on(max)}$, during startup or after a large step increase in load current. This means that the flux density cannot be permitted to go more than half way toward saturation under normal conditions or the core will saturate under transient conditions.

Saturation flux density for 3C8 power ferrite material is greater than 0.3 Tesla (3000 Gauss), allowing a ΔB of 0.15T (0 to 0.15T) in this application. (With Volt-second control, available in the UC1840 control IC, a ΔB of 0.3T would be permissible, significantly reducing the transformer size).

Core Selection. The core area product, AP, requirements in this applications are calculated for power input of 333 Watts and frequency of 40KHz.

$$AP = A_w A_e \left(\frac{11.1 P_{in}}{K \Delta B f} \right)^{1.143} = \left(\frac{11.1 \cdot 333}{0.141 \cdot 0.15 \cdot 40.000} \right)^{1.143} = 5.4 \text{ cm}^4$$

This equation is based on the assumptions that the windings occupy 40% of the window area, the primary and secondary windings are of equal area, and the windings are operated at a current density that will result in a temperature rise of 30°C with natural convection cooling.

The EC52 core with an AP of 5.71 cm⁴ is the obvious choice.

Designing the Windings. The minimum number of primary turns required to support the Volt-seconds required for normal operation is calculated from equation :

$$N_p(\min) > \frac{5000 V_{in(\min)}}{\Delta B A_e f} > \frac{5000 \cdot 200}{0.15 \cdot 1.183 \cdot 40.000} > 91 \text{ turns}$$

The primary to secondary turns ratio is :

$$n = \frac{N_p}{N_s} = \frac{0.9D(V_{in(\min)} - V_{CE(sat)})}{V_o + V_F} = \frac{0.45(200 - 2)}{5 + 0.8} = 15.36$$

Secondary turns :

$$N_s = \text{Integer}(N_p/n) = \text{Integer}(91/15.36) = 6 \text{ turns}$$

Recalculate the primary turns :

$$N_p = 6 \times 15.36 = 92 \text{ turns}$$

RMS primary current from :

$$I_p = I_{in(max)}/K_t = \frac{P_{in(max)}}{V_{in(max)} K_t} = \frac{333}{200 \cdot 0.71} = 2.34A$$

The maximum current density for this size core is : $J_{max} = 450AP^{-0.125} = 450(5.71)^{-0.125} = 362 \text{ A/cm}^2$

The minimum primary wire area, A_{xp} , is :

$$A_{xp} = I_p(max)/J_{max} = 2.34/362 = .0065 \text{ cm}^2$$

0.9mm is appropriate.

The maximum RMS secondary current, I_s , occurs at 50% duty cycle :

$$I_s(max) = I_o(max)/1.414 = 50/1.414 = 35.3A$$

Minimum secondary wire area, A_{xs} , is :

$$A_{xs} = I_s(max)/J_{max} = 35.3/362 = 0.0975 \text{ cm}^2$$

This calls for 3.6mm to 3.25mm. Ten 1mm wires in parallel will carry the required secondary current and provide a smooth winding with less leakage inductance and acceptable eddy current losses. Copper strip 2.5 x 0.4cm could also be used.

The number of turns required for the auxiliary winding is :

$$N_a = \frac{V_{dd} N_p}{V_{in(min)}} = \frac{15}{200} \times 92 = 7 \text{ turns}$$

This will provide enough Volt-seconds during fly-back to reset the core (back to zero flux density) at 50% maximum duty cycle. 0.2mm wire is adequate to carry the V_{dd} supply current. This winding should be tightly coupled to the primary.

Double-check the wire fit in the window (neglect N_a). The total copper area of all windings should be less than 40% of the total window area of the core ($0.4 \times 3.12 = 1.25\text{cm}^2$ max.).

$$A_w' > N_p A_{xp} + N_s A_{xs} = 92(.0065) + 6 \times 10(.00823) = 1.09\text{cm}^2$$

Calculate Losses and Temperature Rise. The mean length per turn, ϕ_t , for the EC52 core is 7.3cm, and 0.9mm wire is .000353 Ω /cm at 100°C.

$$P_w = 2 \phi_p^2 N_p \phi_t (\Omega/\text{cm}) = 2 (2.34)^2 \times 92 \times 7.3 \times .000353 = 2.59\text{W}$$

The flux density assumes the transformer is operating with a symmetrical flux swing about the origin. The forward converter operates asymmetrically with $\Delta B/2$, or .075T. The resulting 0.1W/cm² must be multiplied by the core volume to obtain the total core loss, P_c .

$$P_c = .01 \times 18.7 = .187\text{W}$$

Total transformer losses are :

$$P_t = P_w + P_c = 2.59 + .187 = 2.78\text{W}$$

The temperature rise of the core for natural convection cooling is calculated from :

$$\Delta\theta = \frac{850 P_t}{A_s} = \frac{850 (2.78)}{91} = 25.9^\circ\text{C}$$

Summarizing the transformer design :

Core : Ferroxcube EC52, 3C8 Ferrite E-E core
 N_p : 92 turns 0.9mm
 N_a : 7 turns 0.2mm
 N_s : 6 turns 10 x 1mm (10 wires paralleled)

The primary and auxiliary windings are tightly coupled. The secondary is insulated with 2 mil mylar tape to provide 3750V line isolation capability.

Filter Inductor Design. The inductor design is summarized as follows :

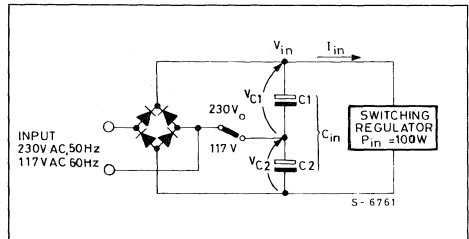
Core : Ferroxcube 4229-3C8 Ferrite Pot Core
 Winding : 7 turns 10 x 1.15mm (10 wires paralleled)
 Losses : 2.2W
 Temp.
 Rise : 35°C

APPENDIX B

LINE INPUT AC TO DC CONVERSION AND INPUT FILTER CAPACITOR SELECTION

The input rectifier/filter section of an off-line power supply converts the 50-60Hz AC line voltage to a DC voltage, V_{in} , which powers the downstream high frequency switching section. A circuit diagram typical of a dual range input rectifier/filter section is shown in Figure 1B. For 230V line operation, the input rectifiers are configured as a full-wave bridge. For 117V operation, the input circuit is reconfigured as a voltage doubler, so that V_{in} will be approximately the same as under 230V operation. While it is technically possible to operate the input section as a bridge at both 230V and 117V, the switching regulator would have to be designed to operate over a much larger V_{in} range which would significantly increase its cost.

Figure 1B : Circuit Diagram.



Input filter capacitance C_{in} determines V_r , the 100/120Hz peak to peak ripple voltage component of V_{in} (see figure 2B). At low line voltage, V_r determines the minimum input voltage, V_{min} , which is an important consideration in the design of the switching supply. V_{min} defines the transformer turns ratio required to achieve the specified output voltage at maximum duty cycle.

If the input filter capacitance is too small, the resulting large ripple voltage will require increased duty cycle range and control loop gain to maintain the specified output voltage. V_{min} will be less, resulting in poor transformer utilization, higher peak current through the switching transistors, and higher peak inverse voltage across the output rectifiers.

Input filter capacitance larger than necessary will not only cost more, the recharging current pulses drawn from the line will be narrower and larger in amplitude (figure 2B). This hurts the line power factor and increases EMI. The higher RMS input current causes increased losses in the line, input rectifiers and filter capacitors, and can impair reliability.

Table 1. 100W Input Rectifier/Filter Section

Parameter		117V Bridge (60Hz)	117V Doubler (60Hz)	230V Bridge (50Hz)	Unit
RMS Line Voltage	V_{ac}	99-135	99-135	195-265	V
Peak Line Voltage	V_{pk}	140-191	280-382	276-375	V
Max Ripple Voltage	V_r	40	80	76	V
DC Input Voltage	V_{in}	100-191	200-232	200-375	V
Input Capacitance	* C_{in}	203	80	61	μF
Doubler Capacitance	* C_1, C_2		160	(122)	μF
Charging Time	t_c	1.954	2.275	2.345	ms
Peak Charge Current	* I_{chg}	3.64	3.28	1.82	A
RMS AC Charge Current	* I_{chg}	1.54	1.126	.776	A

ERROR : AMPL. - 10Hz

A reasonable rule of thumb is to compromise on a ripple voltage 25-30% of the minimum peak line voltage, resulting in acceptable capacitor size, weight and cost. Table 1 shows the resulting values for 117V bridge operation with V_{min} of 100V, and 117V doubler and 230V bridge operation with V_{min} of 200V, for a switching supply with 100W power input. The input filter capacitors are designed to supply the full load energy of the supply and hold V_{in} above the desired V_{min} between AC line peaks. With the switched dual range input section (117V doubler of 230V bridge) filter capacitor requirements are determined by the voltage doubler configuration.

Design Equations and Calculations : The following examples are given for full-wave bridge operation from the 230V line (195-265V), and full-wave bridge and voltage doubler operation from 117V line (99-135V).

Since virtually all the losses in the switching power supply are downstream of the input rectifier/filter, the input section must handle the entire power input, P_{in} (equal to full load power output divided by efficiency). Power input in these examples is assumed to be 100W at full load. The resulting capacitance and current values can be adjusted for any other power input by multiplying by the actual $P_{in}/100$.

Between line peaks, the input filter capacitor must supply the entire full load energy requirement of the supply. Ripple voltage V_r must be small enough to maintain V_{in} greater than the desired V_{min} under worst case conditions of low line frequency, low line voltage and full load. Energy required at 100W for one entire line cycle at **50Hz** (worst case used with 230V line) :

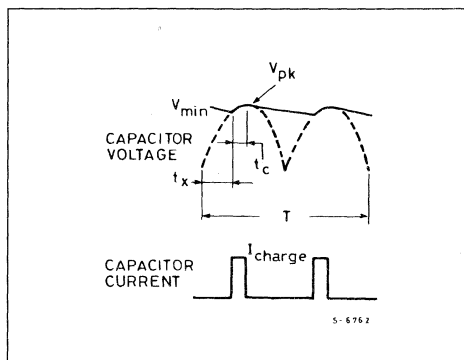
$$V_{in} = \frac{P_{in}}{f} = \frac{100}{50} = 2.0 \text{ Joules (W-sec.)} \quad (1)$$

At **60Hz**, the energy required for one line cycle at 100W is reduced to **1.667 Joules**.

Full Wave Bridge Operation. Referring to figures 1B and 2B, input filter capacitor C_{in} (C_1 in series with C_2) charges to peak line voltage each half cycle. C_{in} then discharges, providing all the energy required by the switching supply until it is recharged at the next half cycle. Energy from C_{in} each **half** line cycle is :

$$W_{in}/2 = \frac{1}{2} C_{in} (V_{pk}^2 - V_{min}^2) \quad (2)$$

$$C_{in} = \frac{V_{in}}{V_{pk}^2 - V_{min}^2}$$

Figure 2B : Bridge Waveforms.

As shown in figure 2B, the recharging time, t_c , is established by the intercept of the capacitor voltage waveform with the rectified AC line :

$$V_{\min} = V_{pk} \cos(2\pi f t_c)$$

$$t_c = \frac{\cos^{-1}(V_{\min}/V_{pk})}{2\pi f}$$

Assuming a rectangular charging current pulse of peak amplitude i_{chg} (constant current during the charging interval) :

$$\Delta Q = i_{chg} \Delta t = C \Delta V \quad (4)$$

$$i_{chg} = C (V_{pk} - V_{\min}) / t_c$$

The RMS AC component of the charging current, i_{chg} , is conducted through the filter capacitors and contributes to capacitor heating due to their equivalent series resistance (ESR). The DC component of the total RMS charging current does not pass through the capacitor and does not contribute to capacitor heating.

$$i_{chg} = \sqrt{I_{CHG}^2 - I_{DC}^2} = \sqrt{i_{chg}^2 t_c 2/T - i_{chg}^2 (t_c 2/T)^2} \quad (5)$$

$$I_{chg} = i_{chg} \sqrt{t_c 2f - (t_c 2f)^2}$$

The switching supply discharges the input capacitors by drawing high frequency pulses of current. The AC component of the RMS discharge current, I_{dis} , also causes filter capacitor heating. The filter capacitors must be selected to have RMS current ratings greater than the total RMS AC current components. This is an important consideration for capacitor reliability.

$$\text{Total } I_{CAP} = \sqrt{I_{chg}^2 + I_{dis}^2}$$

The DC component of the high frequency discharge current pulses equals the DC component of the charging current from the line. Because the form factor of the high frequency discharge current at low line is much better (closer to 1.0) than the charging current waveform, the RMS AC discharge current, I_{dis} , is much less than I_{chg} , depending somewhat on the switching circuit topology.

For 230V (50Hz) bridge operation : At 195V minimum line voltage, the minimum peak voltage, V_{pk} , is 276V. Conservatively assume 270V peak, allowing for drops in rectifiers and line. From Equation (2) :

$$C_{in} = \frac{2}{270^2 - 200^2} = 61\mu F$$

Changing pulse width from equation (3) :

$$t_c = \frac{\cos^{-1}(200/270)}{2\pi 50} = 2.345\text{ms}$$

Peak charging current from Equation (4) :

$$i_{chg} = 61 (270-200)/2.345 \times 10^{-3} = 1.82\text{A}$$

RMS charging current from Equation (5) :

$$t_c 2f = 2.345 \times 10^{-3} \times 2 \times 50 = .2345$$

$$I_{chg} = 1.82 \sqrt{.2345 - .2345^2} = .771\text{A}$$

For 117V (60Hz) bridge operation (normally used only for single range 117V input) : At 99V minimum V_{pk} is 140V. Conservatively assume 135V peak, allowing for drops in rectifiers and line :

$$C_{in} = \frac{1.667}{135^2 - 100^2} = 203\mu F$$

$$t_c = \frac{\cos^{-1}(100/135)}{2\pi 60} = 1.954\text{ms}$$

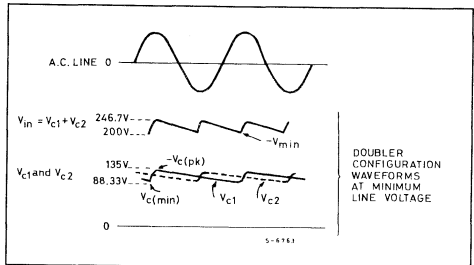
$$i_{chg} = 203 (135 - 100)/1.95 \times 10^{-3} = 3.64\text{A}$$

$$t_c 2f = 1.954 \times 10^{-3} \times 2 \times 60 = .2345$$

$$I_{chg} = 3.64 \sqrt{.2345 - .2345^2} = 1.54\text{A}$$

Voltage Doubler Operation, 117V (60Hz) Line : Referring to figure 1B and 3B at minimum line voltage (99V), the peak voltage is 140V. Conservatively assume 135V peak, allowing for drops in rectifiers and line.

Figure 3B : Voltage Doubler Waveform.



C_1 and C_2 alternatively charge to peak line voltage. Note that whenever the input voltage, V_{in} , is at instantaneous minimum, one capacitor is at its minimum, but the other capacitor is half way between peak and minimum voltage. The minimum voltage on each capacitor corresponding to an overall $V_{\min}$ of 200V can be approximated as follows :

$$V_{\min} = V_{C1\min} + V_{C2\text{avg}} = V_{C\min} + \frac{V_{C\min} + V_{Cpk}}{2}$$

$$V_{C\min} = \frac{2V_{\min} - V_{Cpk}}{3} = \frac{2(200) - 135}{3} = 88.33\text{V}$$

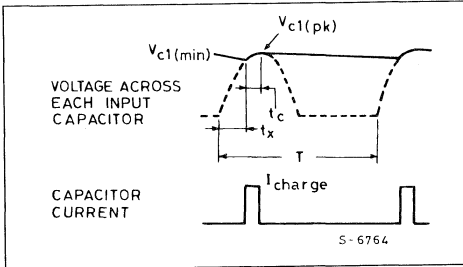
C_1 and C_2 each discharge for a complete cycle. Each capacitor must supply half the energy required by the switching regulator for an entire line cycle :

$$W/2 = \frac{1}{2} C_1 (V_{Cpk}^2 - V_{Cmin}^2)$$

$$C_1 = C_2 = \frac{W}{V_{Cpk}^2 - V_{Cmin}^2} = \frac{1.667}{135^2 - 88.33^2} = 160\mu F \quad (8)$$

C_{in} the series combination of C_1 and C_2 , equals $80\mu F$.

Figure 4B : Voltage Doubler Charging Current.



Note that the voltage doubler operated from the 117V line requires larger C_{in} than the 230V bridge input, so that for supplies with dual range 117/230V input, the 117V doubler operation dictates the filter capacitor requirements.

Figure 4B shows the waveforms associated with charging each of the input capacitors in the voltage doubler configuration at full load and minimum line voltage. Recharge time, t_c , is established by the intercept of the capacitor voltage waveform with the rectified AC line :

$$V_{C1min} = V_{C1pk} \cos(2\pi f t_c)$$

$$t_c = \frac{\cos^{-1}(V_{C1min}/V_{C1pk})}{2\pi f} \quad (9)$$

$$t_c = \frac{\cos^{-1}(88.3/135)}{2\pi \cdot 60} = 2.275\text{ms}$$

Assuming a rectangular charging current pulse of peak amplitude i_{chg} (constant current during the charging interval) :

$$\Delta Q = i_{chg} \Delta t = C \Delta V$$

$$i_{chg} = C (V_{pk} - V_{min})/t_c \quad (10)$$

$$i_{chg} = 160 (135 - 88.3)/2.275 \times 10^{-3} = 3.28\text{A}$$

The RMS current in each capacitor is :

$$I_{chg} = i_{chg} \sqrt{t_c f - t_c^2 f^2} \quad (11)$$

$$t_c f = 2.275 \times 10^{-3} \times 60 = .1365$$

$$I_{chg} = 3.28 \sqrt{.1365 - .1365^2} = 1.126\text{A}$$

APPENDIX C

PROPORTIONAL BASE DRIVE

Proportional base drive is a simple and effective method of achieving improved performance with high voltage bipolar power switching transistors in off-line applications. As shown in figure 1C, a current transformer provides regenerative base drive current whose amplitude is proportional to the collector current being switched. The drive current ratio is established by the turns ratio of the collector and base windings.

The proportional drive method may be employed with any power switching circuit topology. Advantages over conventional fixed base current drive methods include :

1. Fixed base drive current must be large enough to handle the full load (or short-circuit load) collector current. Under lightly loaded conditions, the switching transistors are severely over-driven, resulting in long storage and fall times and more difficult turn-off. Proportional drive provides optimal performance under varying load current conditions.
2. Proportional base drive requires less drive power from the control circuit. During the "on" time of the switching transistor, base drive is provided regeneratively from the collector circuit through the current transformer. The control drive circuit is not required to provide sustaining base drive current. It must only provide short pulses of drive current to initiate turn-on and turn-off. The amplitude of these drive current pulses can easily be made large enough to obtain good switching performance from high voltage bipolar devices in off-line applications.

Referring to figure 1C and 2C, when driver transistor Q1 is on, power switch Q2 is off. Magnetizing current I_{d1} in the control drive winding N_d approaches a steady-state value equal to the drive circuit supply voltage V_{dd} divided by R_1 . Capacitor C_1 is discharged and there is zero voltage across all windings of T_1 .

Figure 1C : Proportional Base Drive Circuit.

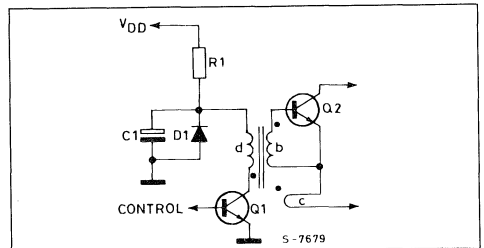
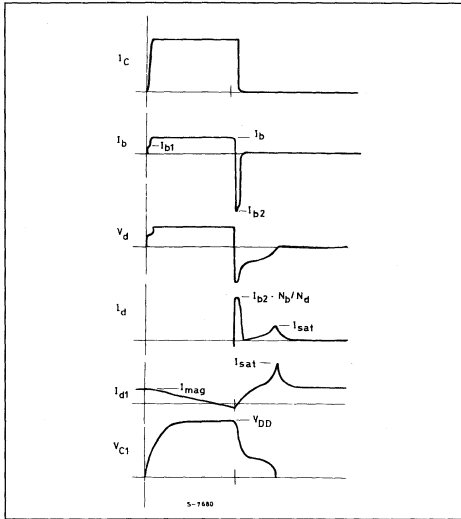


Figure 2C : Waveforms.

When the output of the control circuit turns on, driver Q_1 turns off and primary current I_{d1} must cease. Energy stored in T_1 causes the voltage at the dotted ends of all windings to flyback in the positive direction. I_{d1} multiplied by turns ratio N_d/N_b becomes I_{b1} , the turn-on base drive current pulse to Q_2 .

Collector current I_c starting to flow in winding N_c causes a regenerative increase in base drive to Q_2 until it is switched fully on. The final value of I_c induces a proportional base drive current, I_b , according to the turns ratio N_b/N_c .

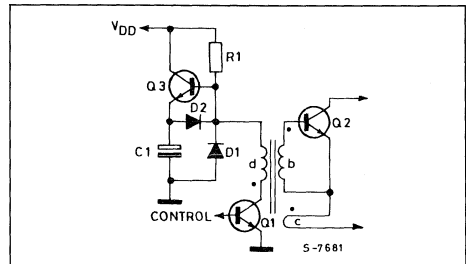
During the time that Q_2 is on and Q_1 is off, capacitor C_1 charges through R_1 to supply voltage V_{dd} . At the end of this "on" period, driver transistor Q_1 is turned on again, applying the voltage on capacitor C_1 to the drive transformer primary. This drives the voltage on the base of Q_2 sharply negative. The turn-off base current pulse, I_{b2} , can be made larger than Q_2 collector current, resulting in very rapid turn-off of Q_2 .

After Q_2 is off and I_{b2} ceases, any remaining voltage on C_1 across the drive transformer primary helps to rebuild the magnetizing current. Diode D_1 prevents the possibility of any underdamped ringing from driving the upper end of N_d negative. At the end of the "off" period, magnetizing current I_{d1} has been re-established and the cycle repeats.

It is quite feasible to operate high voltage bipolar transistors at frequencies above 50kHz with reasonable efficiency because of the large amplitude base drive pulses obtainable with this method. However,

the circuit of figure 1C, as just described, is not capable of operation at frequencies above a few kHz. This is because capacitor C must charge to V_{dd} during the "on" period of Q_2 , and the $R_1 C_1$ charging time constant is far too long for this to be accomplished at 50kHz.

This problem is solved by the addition of a rapid recharge circuit as shown in figure 3C. During the time that Q_2 is on and Q_1 is off, current through R_1 is multiplied by the current gain of Q_3 , which significantly reduces the charging time of C_1 . When Q_1 turns on, C_1 discharges through D_2 . The base-emitter of Q_3 is reverse biased, holding it off during the entire Q_2 "off" time.

Figure 3C : Improved Proportional Base Drive Circuit.

Design Procedure. Application parameter values must be defined, including drive requirements for the power switching transistors.

- I_c Maximum collector current
- I_{b1} Initial turn-on base drive current
- I_c/I_b Sustaining proportional base drive ratio
- I_{b2} Turn-off base drive current at max. I_c
- V_{bb2} Turn-off base drive source voltage at max I_c
- t_2 Maximum transistor turn-off time
- V_{dd} Drive supply voltage
- f Operating frequency

Drive transformer base/collector turns ratio is equal to the desired proportional base drive ratio :

$$N_b/N_c = I_c/I_b \quad (1)$$

Drive transformer driver/base turns ratio is established by the desired turn-off base source voltage and drive circuit supply voltage, minus 1V diode drop :

$$N_d/N_b = (V_{dd} - 1)/V_{bb2} \quad (2)$$

When Q_1 turns off, primary magnetizing current, I_{d1} , transferred to the base winding must provide the required turn-on base drive, I_{b1} .

$$I_{d1} = I_{b1}/(N_d/N_b) \quad (3)$$

The R_1 value required to obtain this magnetizing current is :

$$R_1 = V_{dd}/I_{d1} \quad (4)$$

During initial turn-off, driver primary current I_{d2} must absorb the proportional base drive current and transformer magnetizing current I_{d1} in addition to the turn-off base drive current :

$$I_{d2} = \frac{I_{b2} + I_c(N_b/N_c)}{(N_d/N_b)} + I_{d1}$$

Capacitor C_1 is designed to supply the worst-case energy required to turn off Q_2 :

$$W = \frac{1}{2} C_1 (V_{dd} - 1)^2 = (V_{dd} - 1) I_{d2} t_2$$

$$C_1 = \frac{2 I_{d2} t_2}{V_{dd} - 1} \quad (6)$$

When Q_2 is operated at very low duty cycle (such as immediately after a sudden decrease in load current), C_1 may not have time to fully charge to V_{dd} during the very short "on" time, in spite of the assistance provided by Q_3 . This will probably not be a problem, because Q_2 will also not have time to store much charge and will be much easier to turn-off. The time required for Q_2 to reach equilibrium charge storages is comparable to the time required to remove this charge during turn-off. The C_1 charging time constant (reduced according to the gain, H_{fe} of Q_3) will generally be adequate if it is less than 1/2 the Q_2 turn-off time, t_2 .

$$T_{C1} = R_1 C_1 / H_{fe} \quad (7)$$

Drive Transformer Design. Turns ratios for the drive transformer were established in equations (1) and (2). Only certain integral number of turns are permissible for each winding. For example, if N_d/N_c is 25, the permissible number of drive winding turns are 25, 50, 75, etc., corresponding to 1, 2 and 3 collector turns.

Winding i^2R losses are usually negligible. The drive transformer design is based on the following two considerations :

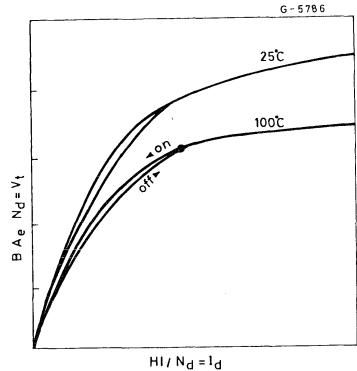
1. Magnetizing current I_{b1} is required for initial turn-on of the power switching transistor. During the time Q_2 is on, the magnetizing current will decrease due to voltage V_{be} across the base winding. The magnetizing current must not be allowed to decrease to less than zero, or it will cause premature turn-off under light load conditions by overcoming the small proportional drive current I_b . Referred to the primary, the drive winding inductance must be large enough to prevent I_{d1} (Equation 3) from reaching zero with volt-

age $V_{be} (N_d/N_b)$ during the longest possible "on" time (usually half the switching period, $1/2f$) :

2. Under light load conditions, relatively little charge is required to turn-off Q_2 . C_1 will then have substantial voltage remaining which will be applied to the drive winding during the remainder of the "off" period. This will cause the magnetizing current (and its associated energy storage) to become much larger than desired. The problem is solved by designing the drive winding to saturate at a current level slightly greater than the desired value of magnetizing current, I_{d1} . This will result in dumping any excess energy remaining in C_1 and establishing a consistent starting point on the B-H characteristic at the beginning of each "on" period.

Figure 4C shows the B-H characteristic of the core as seen from the drive winding. For the vertical axis, B times core area A_e and N_d equals $\sqrt{V_d} \phi_t$ (Faraday's Law). For the horizontal axis, H times effective core length, ϕ , and divided by N_d equals the magnetizing current I_d (Ampere's Law). The characteristic slope equals the drive winding inductance, L_d , and the area to the left equals the energy stored.

Figure 4C.



The operating point shown will satisfy the two requirements above if it exceeds I_{d1} on the horizontal axis and if it exceeds $V_{be} (N_d/N_b)/2f$ on the vertical axis under worst case conditions at high temperature. Procedurally, use Faraday's Law with B close to saturation at high temperature and with the area, A_e , of the core selected. Solve for N_d :

$$\frac{V_{be} (N_d/N_b)}{2f} = B A_e N_d \quad (8)$$

Use the smallest permissible N_d equal to or greater than the value calculated above. An N_d value larger than the calculated amount simply means that the

change in flux density will be less than the maximum permitted.

Next, use Ampere's Law with a value for H corresponding to the B value chosen before, the smallest permissible N_d from above, and l equal to l_{d1} . Solve for the magnetic path length, ϕ .

$$N_d l_{d1} = H\phi \quad (9)$$

Compare the actual j_e value for the core selected with the value calculated above. If the actual j_e of the core, is significantly larger than the calculated ϕ , it will be necessary to use either a smaller core, or use a larger permissible number of turns, N_d . Otherwise, the operating point will not be close enough to saturation, and the B and H levels will both be too low to prevent the magnetizing current from becoming negative at the end of the "off" period.

If the actual core j_e is smaller than the calculated ϕ , the core will be too heavily saturated, and will not store enough energy to provide the desired I_{b1} . Either go to larger core, or introduce a small gap, ϕ_g , according to the relationship :

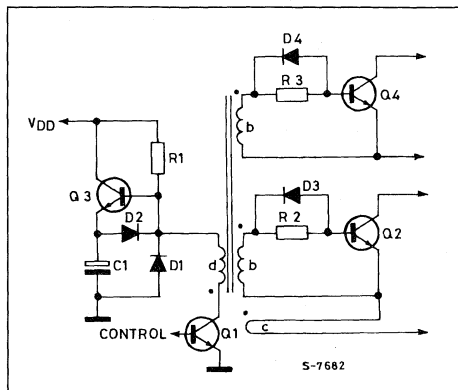
$$j = (\phi_e + \mu_a l_g), \text{ where } \mu_a = B/H \quad (10)$$

Driving Two Transistors. Two power switching transistors are often used in series in order to halve their high voltage V_{ce} rating requirements. It is usually desirable to drive these two transistors from a single drive circuit. This can be accomplished by means of two identical base windings in the transformer. N_b/N_c must be halved and N_d/N_b doubled from the values calculated in Eq. (1) and (2) because the total base current is twice as much as with a single transistor.

As shown in figure 5C it is also necessary to add a small amount of resistance in series with each base in order to ensure current sharing. A resistor which drops 0.5V at maximum sustaining base drive, I_b , should be adequate. The added resistance does not affect the calculation of N_d in Equation (8) because its voltage drop is negligible compared to V_{be} under light load conditions, when the sustaining base drive is small. However, during turn-off, each series base

resistor must be shunted by a small diode. Otherwise, a very large V_{bb2} value would be required in order to pull the desired I_{b2} out of each base. The forward drop on this diode must be added to the V_{bb2} requirement in Eq. (2).

Figure 5C : Two-transistor Driver.



Line-side Vs. Output-side Control Circuit. The base and collector windings of the drive transformer are normally on the input, or line side, of the power supply. When the control/driver circuits are located on the output side of the supply, high voltage insulation is required between the drive winding and the base and collector windings. This high voltage insulation, usually greater than 3000V, will impair the coupling between line-side and output-side windings. This results in high leakage inductance, causing voltage spikes during turn-on and turn-off which may necessitate additional snubbing or clamping the drive transistor collector and the power switching transistor base.

When the control and driver circuits are located on the line side, the drive transformer does not require high voltage insulation. Leakage reactance can be made almost negligible, especially if multifilar windings are employed.

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- (1) J. Gregorich and W. Hazen, "Designing Switched-Mode Converters with a New Proportional Drive Technique", Proceedings of POWERCON 5, May 1978, pp. E2 (1-8).
- (2) P. Wood, "High Efficiency, Cost Effective Off-line

Switching Converters", TRW Applications Note 143, April 1978, pp. 3-4.

- (3) R. Severns, "A New Improved and Simplified Proportional Base Drive Circuit" Proceedings of POWERCON 6, May 1979, pp. B2 (1-12).

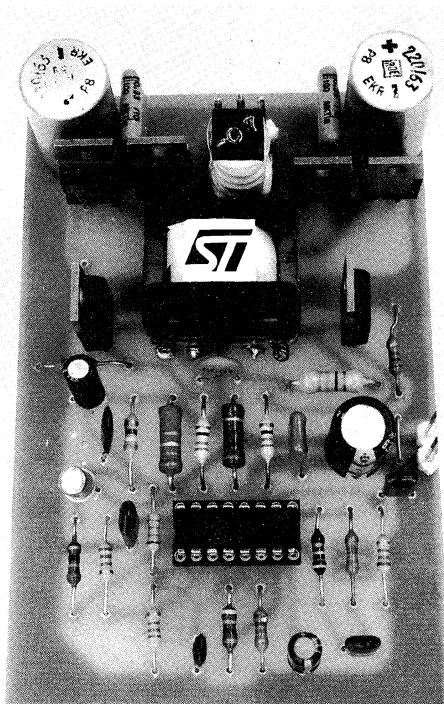
200KHz 15W PUSH PULL DC-DC CONVERTER

INTRODUCTION

The 15W DC-DC converter, shown in Fig. 1 has a push-pull topology and works in continuous mode with two outputs (+6V, -6V) and features primary side control with full protection against fault con-

ditions. There is no insulation between the primary and secondary side.

Due to the high working frequency, the power switches used are the new SGS-THOMSON advanced POWER MOS type: IRFZ20 with high



density and bonding on the active area.

The PWM controller is the linear integrated circuit SGS3525A, with dual source/sink output drivers,

internal soft-start, pulse by pulse shut-down and adjustable dead time control.

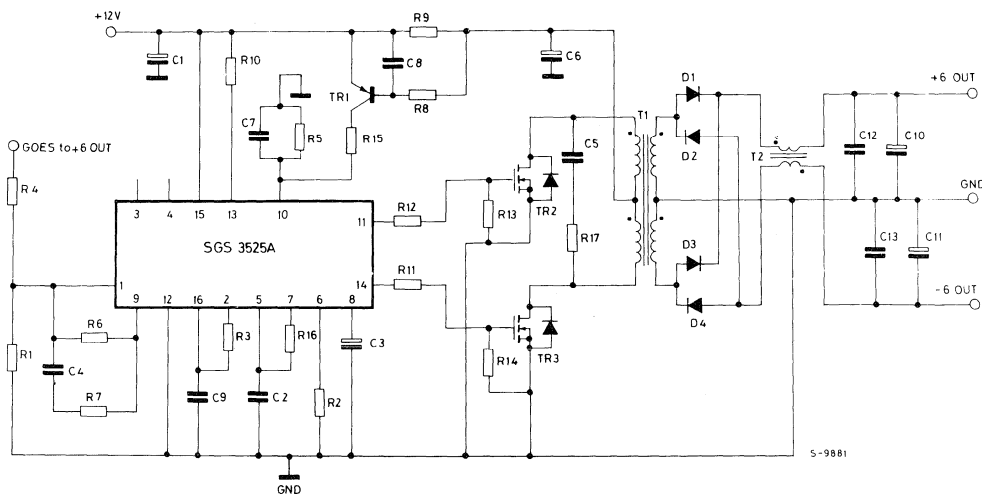
Table 1 shows the power supply specifications.

TABLE 1

Operating mode	:	push-pull
DC input voltage	:	10V DC to 18V DC
Switching frequency	:	200KHz $\pm$ 10%
Total power output	:	15W
Outputs	:	+6V $\pm$ 5% 0.1 to 1.3A -6V $\pm$ 5% 0.1 to 1.3A
Line regulation (+6 output)	:	0.05%/V
Load regulation (+6 output)	:	0.2%/A
Efficiency (@ 1/2 load)	:	76%

Output ripple @ max load +6V, -6V outputs: 50mV peak to peak

Fig. 1



CIRCUIT DESCRIPTION

The DC input is chopped at a high frequency (200KHz). This high switching frequency allows the use of a very small transformer.

Due to the push-pull configuration of the converter the POWER MOS devices, the transformer and the diodes work at the frequency of 100KHz (photo 1, 2); the output filters and the oscillator of PWM controller work at a frequency of 200 KHz (photo 3).

When Tr2 is on and Tr3 is off, diodes D2, D3 conduct and diodes D1, D4 are off. When Tr3 is on and Tr2 is off diodes D1, D4 conduct and diodes D2, D3 are off.

The snubber formed by C5, R17 is used to clamp the voltage spikes on Tr2 and Tr3 drains. With a leakage inductance $L_d = 0.5\mu\text{H}$, a primary current $I_p = 2.8\text{A}$ @ $V_{IN\text{ MIN}}$ and maximum load and an allowable voltage spikes $V_p = 30\text{V}$ we can calculate

C5 as follows:

$$C5 = \frac{L_d \cdot I_p^2}{(2V_{\text{MIN}} + V_p)^2 - (2V_{\text{IN}})^2} = 1.8\text{nF}$$

Eq. 1

The PWM controller SGS352A has the two drive outputs in totem-pole configuration in order to drive the POWER MOS. The feedback signal for the PWM is directly connected to pin (inverted input of error amplifier) from +6V output by the resistive divider R4-R1. The maximum current protection was sensed by Tr1, R9, R8 and is connected to pin 10 (shut-down).

The magnetic coupling of the series inductance in the output filter is very important for good regula-

tion of the voltages. In this way when the load is very different in the two outputs (+6V max load; -6V min load or viceversa) the indirectly regulated output (-6V) has a very stable output voltage (see fig. 2).

The efficiency is excellent: 70% over a wide range (Fig. 3).

The transient response is very fast: about 50ms. Photo 4 shows the transient response of load regulation due to a load variation from 100mA to 1.3A and from 1.3A to 100 mA (+6V output).

Fig. 4 shows the P.C. board (track layout) and the component positions.

Fig. 2

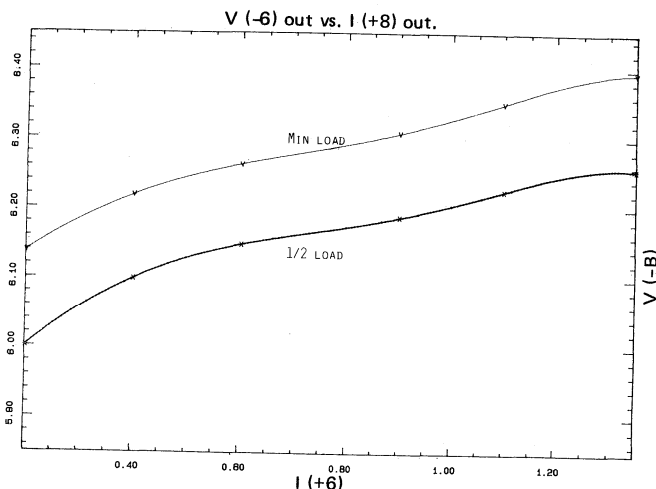


Fig. 3

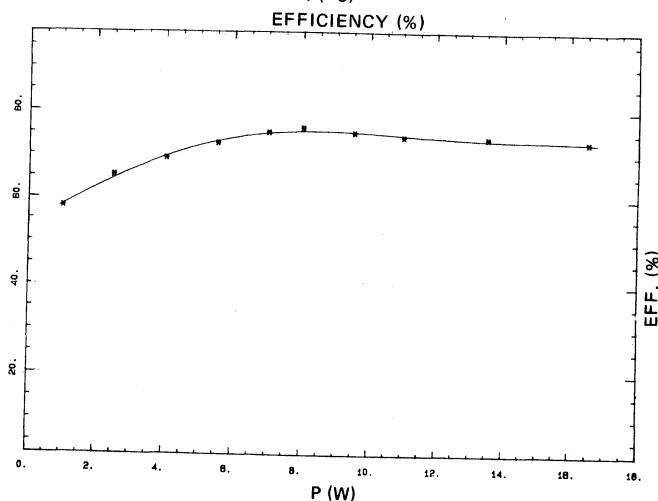
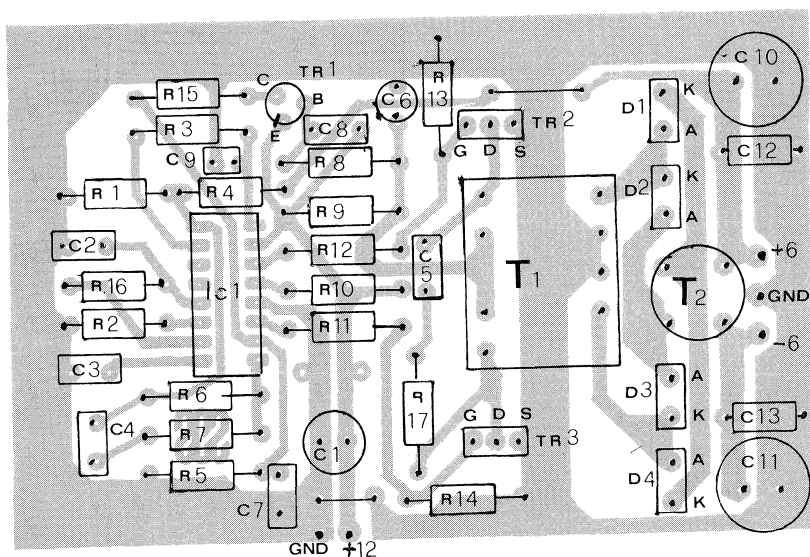


Fig. 4 - P.C. board and components layout (1:1 scale)



TRANSFORMER

For this design a Tominta E core of 2E 6 ferrite material was chosen. To calculate the core size we used the following equations:

$$A_e \cdot A_n > \frac{10^5 \cdot P_{OUT}}{1.16 \cdot \Delta B \cdot f \cdot d} = 0.143 \text{ cm}^4 \quad \text{Eq. 2}$$

where:

P_{OUT} = output 15 (W)

ΔB = flux density swing (T) we chose $\Delta B = 200 \text{ mT}$

d = current density we chose = 450 A/cm^2

f = working frequency of transformer

A_e = effective area of magnetic path [cm^2]

A_n = useful winding cross section [cm^2]

The core size is then EE 25 $\times$ 6.5 with $A_e = 0.42 \text{ cm}^2$, $A_n = 0.45 \text{ cm}^2$ and $A_e \cdot A_n = 0.189 \text{ cm}^4 > 0.143 \text{ cm}^4$.

The maximum value of primary current at V_{MIN} is:

$$I_p = \frac{P_{OUT}}{\mu \cdot \delta_{MAX} \cdot (V_{MIN} - \Delta V)} = \frac{15}{0.75 \cdot 0.8 \cdot 9} = 2.8 \text{ A} \quad \text{Eq. 3}$$

Where ΔV is the voltage drop on the R9 resistor

and on the POWER MOS, δ_{MAX} = maximum duty cycle, η = efficiency.

The turns ratio is given by the following equations:

$$n = \frac{V_{prim.}}{V_{sec.}} \cdot \delta_{MAX} = \frac{V_{MIN} - \Delta V}{V_{OUT} + V_f} \cdot \delta_{MAX} = 1.03 \quad \text{Eq. 4}$$

The number of turns N_p is calculated as follows:

$$N_{p MIN} = \frac{V_{MIN} [V] \cdot \delta_{MAX}}{\Delta B [T] \cdot A_e [\text{cm}^2] \cdot f [\text{Hz}]} \cdot 10^4 = 9.5 \text{ turn} \quad \text{Eq. 5}$$

The number of turns used was $N_p = 10$ and $N_s = 10$

The primary inductance is then the same as the secondary inductance.

$$L_p = L_s = N_p^2 \cdot A_L = 100 \cdot 2400 \text{ nH} = 240 \mu\text{H}$$

The value of L_d (leakage inductance) was measured on the transformer:

$$L_d = 0.5 \mu\text{H}$$

OUTPUT FILTER

The most interesting part of the output filter is the transformer T2 which, coupling the output series inductance of the two outputs, gives good regulation of the -6V output (magnetic regulator).

T2 construction is very simple because the two inductance are directly wound on the same cylindrical ferrite core. Each winding is made up of 200 turns and is: $L(+6V) = L(-6V) = 17\mu H$.

The four fast recovery diodes used are BYW29-100 type.

Capacitors C10, C11 are $220\mu F$ Roederstein EKR low ESR type for application in switching power supplies.

The ripple value obtained is very low: 50mV peak to peak (photo 3).

Photo 1 - Tr2, Tr3, V_{ds} ($V_{ds} = 20V/div.$)

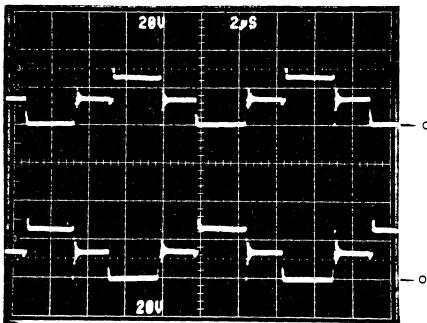
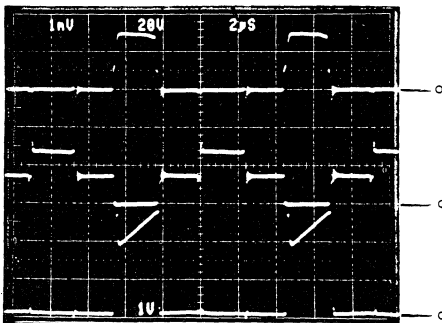


Photo 2 - Tr3 waveforms ($V_G = 10V/div$, $V_{ds} = 20V/div$, $I_d = 1A/div.$)



COMPONENT LIST

Resistors

R1	=	8.2K	1/4W
R2	=	5.6K	1/4W
R3	=	1.2K	1/4W
R4	=	1.5K	1/4W
R5	=	1.2K	1/4W
R6	=	470K	1/4W
R7	=	3.3K	1/4W
R8	=	390Ω	1/4W
R9	=	0.22Ω	1W
R10	=	10Ω	1/4W
R11	=	22Ω	1/4W
R12	=	22Ω	1/4W
R13	=	5.6K	1/4W
R14	=	5.6K	1/4W
R15	=	18Ω	1/4W
R16	=	47Ω	1/4W
R17	=	33Ω	1/2W

Capacitors

C1	=	100μF
C2	=	1nF
C3	=	1μF
C4	=	10nF
C5	=	1.8nF
C6	=	2.2μF
C7	=	10nF
C8	=	2.7nF
C9	=	10nF
C10	=	220μF
C11	=	220μF
C12	=	330nF
C13	=	330nF

Transistors

TR1	=	2N2907
TR2, TR3	=	IRFZ20

Diodes

D1, D2, D3, D4	=	BYW2929-100
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ICs

I1	=	SGS3525A
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Transformers

T1 core	=	TOMITA EE 25 × 6.5 2E6 Material
T2 core	=	cylindrical 30 × 20mm

Photo 2a - Turn ON

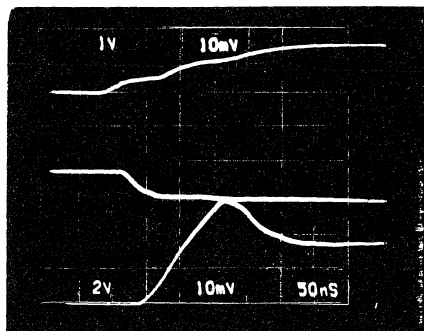


Photo 2b - Turn OFF

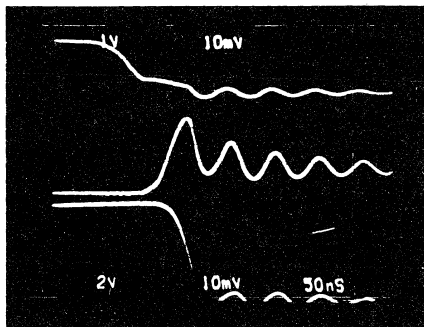


Photo 3 - Ripple on +6V and -6V outputs (20mV/div.)

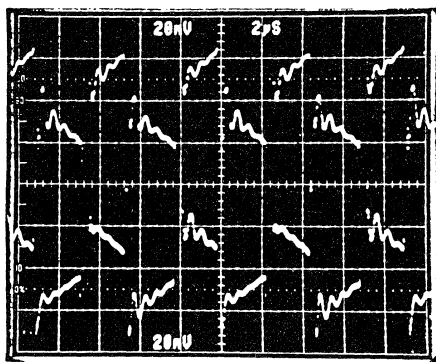
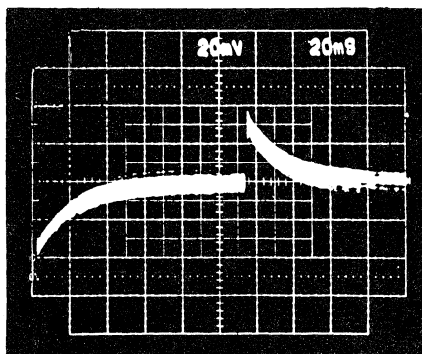


Photo 4 - Transient response (20mV/div)



A WIDE RANGE INPUT DC-DC POWER CONVERTER

INTRODUCTION

This 300W DC-DC converter, shown in Fig. 1 has a flyback topology and works in continuous mode with single output and features primary side control.

The Power switch is designed around an emitter switching configuration. This arrangement uses three bipolar devices, BUX 12, and with POWER MOS device in cascode.

The pulse width modulation (PWM) controller is the SGSUC3840 linear integrated circuit. The characteristics of this IC are pulse by pulse current limiting with shut-down for short circuit protection, over and under voltage sensing with protective shut-down, soft start, voltage feed-forward for excellent line regulation (without regulation by feed back network). These facilities are used to advantage in this design.

CIRCUIT DESCRIPTION

A DC input voltage is chopped at a high frequency, 80KHz is possible.

This high switching frequency allows the use of a very small transformer with respect to the output power.

In the configuration, shown in Fig. 1, an additional low-voltage winding, N_B , (two turns on this transformer) is used to provide continuous operating power for the base of the bipolar power device.

The resulting base current is proportional to the load.

The polarity of the transformer windings is configured as a flyback converter. When transistor Q6 conducts, the output diodes are reverse biased and energy is stored in the primary inductance. When Q6 turns-off, the voltage polarity of the primary winding reverses and the stored energy is delivered to the output.

Fig. 1 300W DC-DC converter circuit diagram.

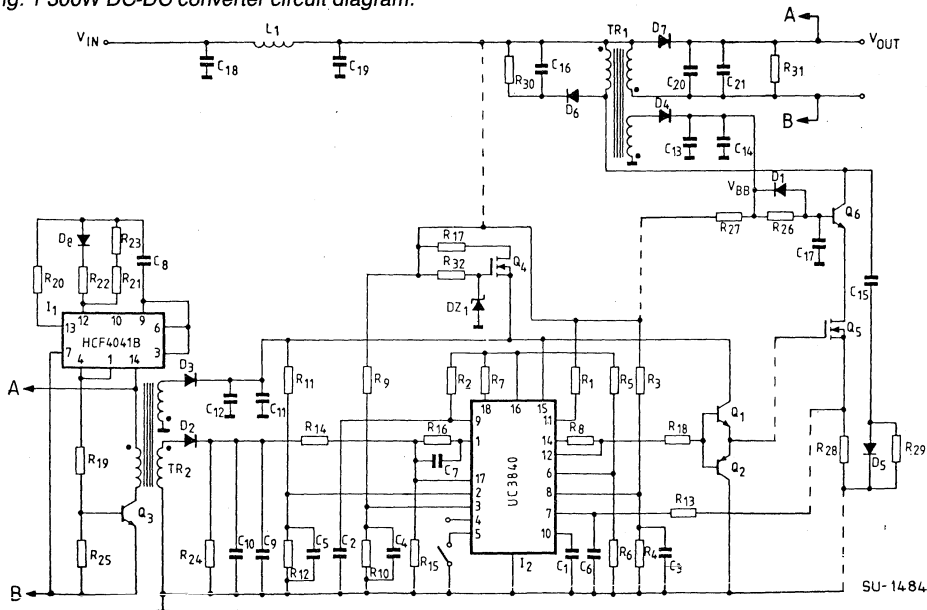


Table 1 - Power Supply Specifications

Operating mode	:	Flyback Continuous Mode
DC Input Voltage	:	48V to 80V DC
Switching frequency	:	80KHz $\pm$ 10%
Output Power	:	300W
Output Voltage	:	12V $\pm$ 5%
Output Current	:	2 to 25A
Line Regulation	:	0.03%/V
Load regulation	:	0.17%/A (med. value)
Efficiency @ 300W		
$V_{IN} = 48 V_{DC}$	:	70%
$V_{IN} = 80 V_{DC}$	:	75%
Efficiency max @ 150W		
$V_{IN} = 70 V_{DC}$	:	80%
Output Ripple @ 25A	:	400mV

The power supply operates in continuous mode: the energy stored in the primary inductance is not completely transferred to the load during each cycle, for this reason the current in the primary winding has a trapezoidal waveform, Fig. 3.

The emitter switching configuration of the power switch allows the bipolar transistor to operate at higher frequencies since this technique gives a substantial reduction in the bipolar storage time.

Other advantages are:

- The dynamic drive circuitry is simplified and the energy needed to drive the gate of the POWER MOS device is very low (800nJ per cycle).
- Greater ruggedness than in a single bipolar switch at turn-off with the inductive load. Consequently there can be smaller snubber networks and a higher leakage inductance in the transformer.
- The power dissipation during on time is lower than the on losses of a single POWER MOS device with the same characteristics (I_C , BV_{CE}) of the bipolar device.

For better load regulation with isolated output, a smaller converter (transformer Tr2 with a small signal transistor Q3, as a switch) is used instead of a feedback winding.

This converter, operating at a fixed frequency (160KHz) and duty-cycle, provides on the first secondary winding, N_i with forward polarity, a voltage proportional to the output regulating voltage, which is used as a feedback signal.

The other secondary winding of this converter (with flyback polarity) N_f is used to provide continuous operating power for the UC3840 and the IRFZ42 gate drive.

Table 2 - Tr2 specifications

- Core	Siemens E20, N30
- Primary	$N_p = 38$ turns
- Feedback sec.	$N_f = 30$ turns
- Supply sec.	$N_i = 56$ turns

The start-up of the power supply is obtained by resistor R27 which supplies the transistor base and by the network (formed by POWER MOS device Q4, DZ1, R17, R32) which supplies the PWM circuit and IRFZ42 gate drive transistors Q1 and Q2. When the voltage on the secondary winding of Tr2 increases, the POWER MOS device, Q4, is automatically turned-off, Q4 is at low voltage, low current POWER MOS device: an SGSP301 was selected. It is interesting to note that the DC safe operating area of a POWER MOS transistor used under these conditions is greater than that of an equivalent bipolar device.

The circuit was mounted on two printed boards. Board 1 holds the control circuit and board 2 the power switch. Board 2 has a copper thickness of about 300 μ m. The high current areas are double sided.

TRANSFORMER

Designing the transformer leads to trade off decisions involving factors such as leakage inductance specifications, insulation, size, power dissipation, and cost.

The core selected for this power supply is a Siemens EC70-N27 with the following characteristics:

- Effective core Area $A = 279 \text{ mm}^2$
- Saturation flux density @ 20°C = 470 mT
- Maximum working flux density $B = 300 \text{ mT}$

The design starts with a calculation of the maximum duty cycle, Δ , and the maximum on time $T_{on \max}$, Fig. 2.

With $V_{CC \min} = 48V$, $V_{reset} = 45V$, $T = 12.5\mu s$ (80KHz).

The maximum duty cycle is;

$$\Delta = \frac{V_{reset}}{V_{reset} + V_{CC \min}} = \frac{45}{45 + 48} = 48\% \quad T_{on \max} = 6\mu s$$

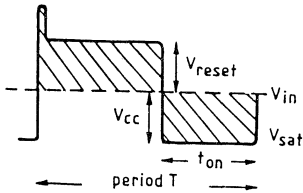
Eqn. 1

By equating the volts/second areas - the shaded areas in Fig. 2 the turns ratio can be calculated using the worst case as follows: (see Fig. 2).

$$\begin{aligned} n_{primary} (V_o + V_t) \cdot (T - T_{on \max}) &= n_{secondary} (V_{CC \min} \cdot T_{on \max}) \\ n_{(p/s)} &= \frac{V_{CC \min} \cdot T_{on \max}}{(V_o + V_t) \cdot (T - T_{on \max})} = \frac{48 \cdot 6 \cdot 10^{-6}}{(12 + 1) \cdot 6.5 \cdot 10^{-6}} = 3.4 \end{aligned}$$

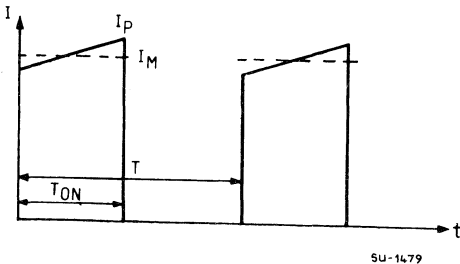
Eqn. 2

Fig. 2 - Switching waveforms at the collector of Q6



SU-1485

Fig. 3 - Current waveform in the primary inductance



SU-1479

Fig. 3 shows the mean current value (I_{mean}) in the primary inductance during the on state. It can be calculated as follows using the minimum input voltage:

$$I_{mean} = \frac{P_{max} \cdot T}{\eta \cdot V_{CC \min} \cdot T_{on \max}} = \frac{300 \cdot 12.5}{0.7 \cdot 48 \cdot 6} = 18.6A$$

Eqn. 3

The primary inductance L_p can be calculated by fixing a maximum peak value for primary current $I_p = 20A$;

$$L_p = \frac{V_{CC \min} \cdot T_{on \max}}{2(I_p - I_{mean})} = \frac{48 \cdot 6 \cdot 10^{-10}}{2 \cdot 1.4} = 100\mu H$$

Eqn. 4

At full load and at $V_{CC \max}$ we have

$$T_{on} = \frac{n \cdot (V_o + V_t) \cdot T}{V_{CC} + n(V_o + V_t)} = 4.4 \mu s$$

Eqn. 5

The flux balance in the transformer core depends on equal volts-second products being applied during charge and reset phases.

$$I_{man} (@ 80V) = \frac{P_{max} \cdot T}{n \cdot V_{max} \cdot T_{on \min}} = 16A$$

$$I_p = 17.1A$$

With an air-gap, $g = 3mm$, then $Al = 140nH$, N_p can be calculated as follows:

$$N_p = \sqrt{L/Al} \text{ (from manufactures data book)}$$

Eqn. 6

$$N_p = \sqrt{100 \cdot 10^3 \text{ nH}/140nH} = 27 \text{ turns}$$

The minimum air gap with working flux density $B = 250mT$ is:

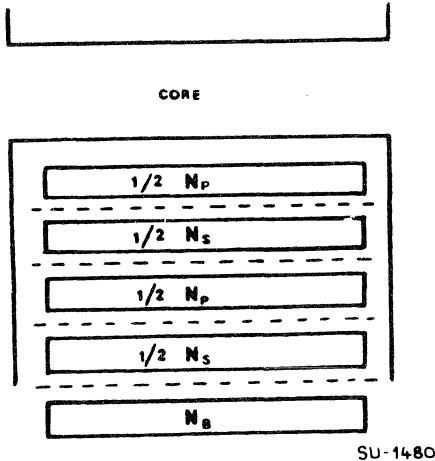
$$g = \frac{I \cdot N_p \cdot \mu_0}{B} = 2.7 \text{ mA}$$

$\mu_0 = 12.56 \cdot 10^{-7} \text{ Hm}^{-1}$ (permeability of free space)

Since we have $g = 3mm$ at all working conditions $B < 250mT$.

$$N_s (+12) = N_p/n = 27/3.4 = 8 \text{ turns}$$

Fig. 4 - Transformer construction showing the winding pattern for reduced for leakage induction.



To reduce the skin effect in the transformer windings at 80KHz, multistrand conductors must be used. The prototype specifications are given in table 3.

Table 3 - Winding specifications

Primary	N_p	= 27 turns, 6 wires $0 = 0.8\text{mm}$
Secondary out.	$N_s(+12)$	= 8 turns, 16 wires, $0 = 0.8\text{mm}$
Secondary aux.	$N_B(+3)$	= 2 turns, 1 wire, $0 = 0.8\text{mm}$

Fig. 4 shows the transformer construction.

POWER SWITCH

In this application the peak switching current is 20A and the correspondent peak collector voltage is approximately 280 volts including the 180 volts spike caused by leakage inductance, Fig. 2.

The bipolar transistors selected are 3 × BUX12 in parallel and the POWER MOS selected is the IRFZ42.

BUX12 × 3

BV_{CEO}	=	250V
BV_{CES}	=	300V
$I_C \text{ CONT}$	=	50A

IRFZ42

BV_{DSS}	=	50V
$R_{DS \text{ ON}}$	=	35 mΩ
I_D	=	35A

The emitter switching configuration gives very short storage time t_s for 3 × BUX12: at full load we have $t_s = 300\text{ns}$ max, and fall time is 150ns maximum. (Photo n. 5).

When the voltage falls on pin 12 of the UC3840, Q1 is off and Q2 conducts. The POWER MOS Q5 is then off and interrupts the emitter current of Q6: at this time current, I_C , flows through the base, becoming a reverse base current I_{B2} that extracts the stored charge from the collector region. The voltage on the drain of Q5 is held at the same value as V_{BB} .

SNUBBERS

To protect the power switch we have two snubber networks.

The first network of C15, R29 and D5 is used to reduce the switch-off power losses of Q6 by delaying the transistor V_{CE} rise while the current falls at turn-off.

$$C15 = \frac{I_p \cdot t_f}{2 \cdot V_{VE \text{ max}}} = \frac{20 \cdot 150 \cdot 10^{-10}}{2 \cdot 280} = 5.35\text{nF}$$

5.6nF was selected

R29 resistor is selected to discharge C15 with a time constant of $3\mu\text{s}$ (about $T_{on \text{ min}}$).

$$R29 = \frac{3 \cdot 10^{-6}}{2C15} = 270\Omega$$

The power dissipated in this resistor is:

$$P = 1/2 C15 \cdot (V_{CE \text{ max}})^2 \cdot f = 17W$$

The second network, C16, R30 D6 is used to limit the overvoltage due to the transformer leakage inductance when Q6 turns-off.

$$C16 = \frac{L_d \cdot I_p^2}{(V_{res} + V_p)^2 - V_{res}^2}$$

Where: L_d = Leakage inductance (about $1\mu\text{H}$)

V_{res} = Reset voltage 45V

V_p = Allowable voltage spike (180V)

$C16 = 8.2\text{nF}$

R30 value is selected so that the voltage across C16 is equal to the reset voltage at the end of the discharge period. Since D6 conducts for about $2.5\mu\text{s}$ C16 discharge period is about $10\mu\text{s}$, then R30 value is calculated as follows:

$$R30 = \frac{(V_{reset} + V_p) \cdot 10 \cdot 10^{-6}}{V_p \cdot C16} = 1.5K$$

The power dissipated in this resistor is:

$$P = 1/2 L_d \cdot I^2 \cdot f = 16W$$

Due to non-linear effects the power dissipated is about 100W.

PWM CONTROLLER

- Operating frequency is set by R2, C2:
With R2 = 8.2K, C2 = 1.5nF, $f = 1/R2 \cdot C2 = 80KHz$

- Start-up is achieved by the network of Q4, R17, R32, DZ1. With a start up current of 60mA we have:

$$R17 = \frac{V_{CC \min}}{60 \cdot 10^{-3}} = 800\Omega \quad R32 = 47K$$

- V_{start} and undervoltage threshold are set by R11, R12. These are calculated by equating the current through the node using Kirchoffs laws.

$$V_{start} = \frac{3V(R11 + R12)}{R12} + 0.2mA \cdot R11 = 13V$$

similary:

$$V_{uv}(fault) = \frac{3V(R11 + R12)}{R12} = 9.5V$$

solving these equation for R11 and R12 then we get the nearest preferred values of:

$$R11 = 18K \quad R12 = 8.2K$$

- Over voltage fault:

Setting the overvoltage fault to $V_{CC} = 100V$ we have:

$$100 = 3V \frac{R9 + R10}{R10} \quad R9 = 33 \cdot R10, R9 = 220K \\ R10 = 6.8K$$

- Duty cycle clamp - soft start:

The duty clamp reduces the duty cycle value to below 48% when the input voltage V_{IN} falls belows 48V.

The divider R3, R4, is set to provide 3.9 volts at pin 8. With $V_{IN(min)} = 46V$, R3 = 507K and R4 = 17K. With C3 = 47nF the soft start time is about 6ms.

The feed forward function provides a variable - slope ramp waveform on pin 10 which is one of the inputs to the PWM comparator. The ramp is proportional to the DC input voltage; in this way the pulse width is immediately reduced when the input voltage rises. The result will be a constant volt - second product delivered to the transformer primary resulting in good open-

loop line regulation.

With $T_{on} = 6\mu s @ 48V$ we have:

$$\frac{dV}{(dt) \min} = \frac{V_p - V_{valley}}{6} = \frac{4.2 - 0.5}{6} = 0.616V/\mu s$$

using this value and $V_{DC \min} = 48V$ with $C1 = \leq C2$

$$\frac{dV}{dt} = \frac{V_{DC \min}}{R1 \cdot C1} \quad R1 \cdot C1 = 77.8\mu s \\ R1 = 220K \quad C1 = 350pF$$

- Current limit.

The resistive divider of R5 (18K) and R6 (1.5K) provides a $V_{ref} = 0.38V$ on pin 7 which is the positive input of error amplifier. For a current limiting value $I_{short \text{ circuit}} = 22A$ the R28 value is set as:

$$R28 = V_{ref}/I_{sc} = 18m\Omega$$

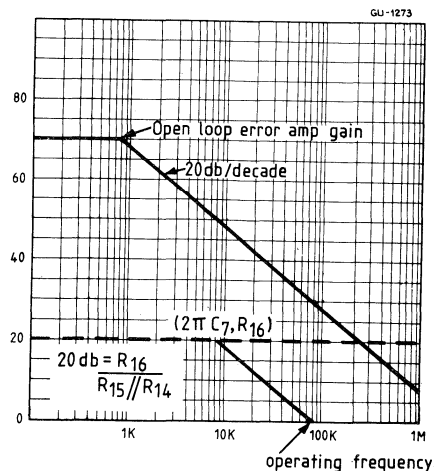
the shut down current value is defined as:

$$I_{SD} = \frac{V_{ref} + 0.4}{R28} = 44A$$

- Voltage control loop.

The error amplifier is set-up for an added DC gain of about 20dB and a second pole at 9KHz. The pole introduced by C17/R16 reduces the gain from 20dB at about 9KHz to 0dB at 80KHz to meet the loop stability criteria.

Fig. 5 - Gain setting for the error amplifier



OUTPUT CAPACITORS

For the high output current of this application the most important characteristics of an output capacitor is its equivalent series resistance, E.S.R. In fact the voltage output ripple is mainly due to losses on the capacitor equivalent series resistance. E.S.R. specification is:

$$\text{E.S.R.} < V_o / I_c \quad \text{where:}$$

V_o = Allowable peak-to-peak output ripple voltage
 I_c = Ripple current in the output capacitor

The mean current in the secondary winding of the transformer while the output diodes conduct is:

$$I_{\text{mean}} = I_{\text{max output}} / (1 - f \cdot t_{\text{on max}}) = 48\text{A}$$

The secondary peak current I_{pk} which corresponds to I_c is:

$$I_{\text{pk}} = I_c = I_{\text{mean}} + 1/2 [\Delta I_{\text{prim}} \cdot n \cdot t_{\text{on}} / T - t_{\text{on}}] = 52.4\text{A}$$

With $V_o = 0.4\text{V}$ we have:

$$\text{E.S.R.} < 0.4 / 52.4 = 0.0075\Omega$$

POWER OUTPUT RECTIFIER

The power output rectifier must be of a fast recovery type in order to reduce losses and the current spike at turn-on of the power switch.

Power diodes with low forward voltages reduce the output filter losses.

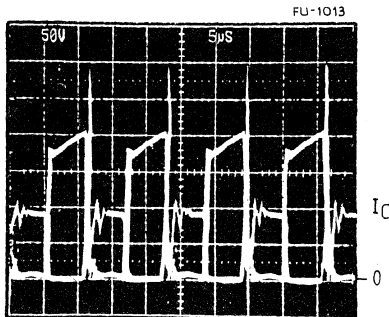
A BYV52 - 50A fast recovery low V_f diode is the solution chosen for this converter.

TESTS ON THE CIRCUIT

The power supply was tested in several operating conditions: with minimum, maximum and rated input voltage, and with various load configurations.

Photograph No. 1 shows the collector voltage and current waveform of the bipolar switch at maximum load ($I_{\text{out}} = 25\text{A}$) and at minimum input voltage.

Photo 1 - I_c , V_{CE} on bipolar switch ($I_c = 5\text{A/div}$, $V_{CE} = 50\text{V/div}$)



This is the worst case because it has a higher primary current and consequently a higher voltage spike on bipolar collectors (due to leakage inductance).

Photograph Nos. 2 and 3 show the details of photograph No. 1 during turn-off and turn-on respectively.

Photograph No. 4 shows bipolar device base current and POWER MOS device gate voltage with the same operating conditions as Photograph No. 1.

Photograph No. 5 shows the collector current, I_c and the base current, I_b waveforms of the bipolar device at turn-off; we can see the high value of reverse base current I_{B2} and the very short storage time (about 300ns).

Photograph No. 6 shows the output ripple at maximum load with $V_{\text{IN}} = 48\text{V}$. (Worst case).

Photo 2 - Turn-off, bipolar switch ($I_c = 5\text{A/div}$, $V_{CE} = 50\text{V/div}$)

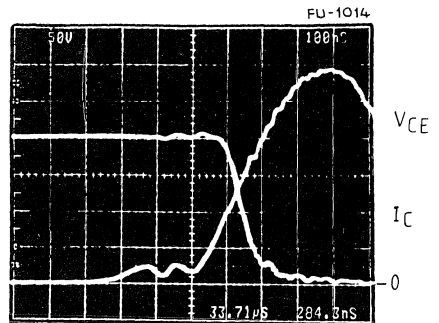


Photo 3 - Turn-on, bipolar switch ($I_c = 5\text{A/div}$, $V_{CE} = 50\text{V/div}$)

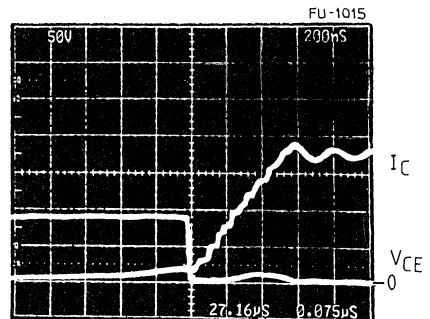
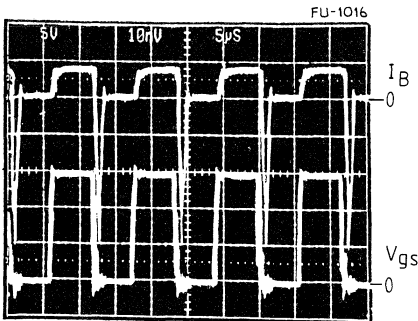
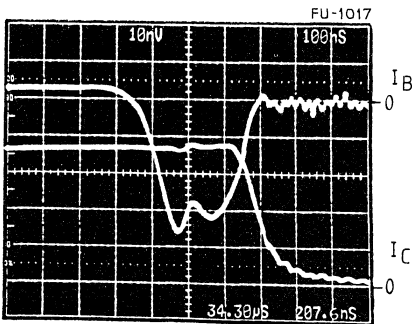
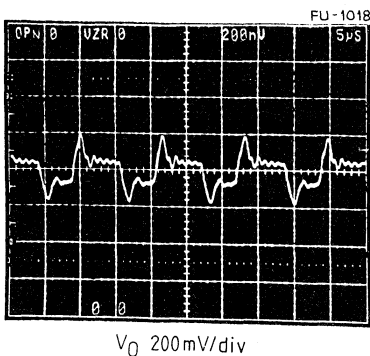


Photo 4 - $I_B = 2A/div$, $V_{gate} = 5V/div$ Photo 5 - Storage time bipolar switch ($I_B = 5A/div$, $I_C = 5A/div$)Photo 6 - Output ripple $v = 200m V/div$ 

Photograph No. 7 shows the transitory response of load regulation due to a load variation from 1A to 25A and from 25A to 1A.

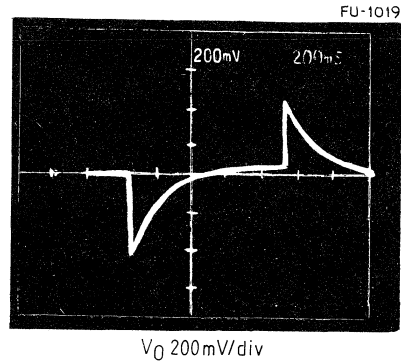
Photo 7 - Transient response $V = 200mV/div$ 

Fig. 6 and fig. shows the line regulation and the load regulation ($V_{IN} = 70V$) respectively. The line regulation is $0.03\%/V$ with an overall variation of 1.1% and the load regulation is $0.17\%/A$ with an overall variation of 2.9% over the operating range.

Fig. No. 8 shows the efficiency of the DC-DC converter at $V_{IN} = 70V$. At full load ($I_{out} = 25A$) the efficiency is 75% and the power losses on the circuit are about 100W. The power losses are divided approximately as follows: (Table 4)

Table 4

— 25W	Losses on output diodes
— 27W	Losses on transformer
— 27W	Losses on the two snubbers
— 5W	Losses on IRFZ42
— 10W	Losses on bipolar devices
— 2W	Losses on resistor R26
— 2W	Losses on resistor R28
— 1.5W	Losses on resistor R31

Fig. 6 - Line regulation

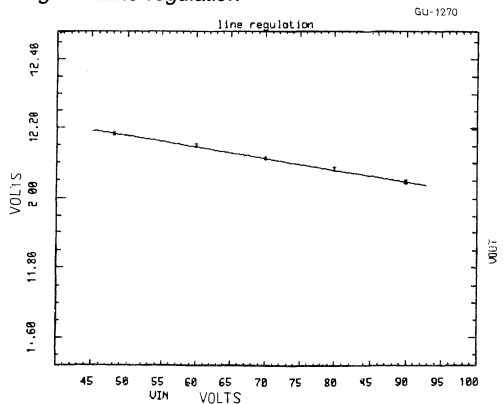


Fig. 7 - Line regulation

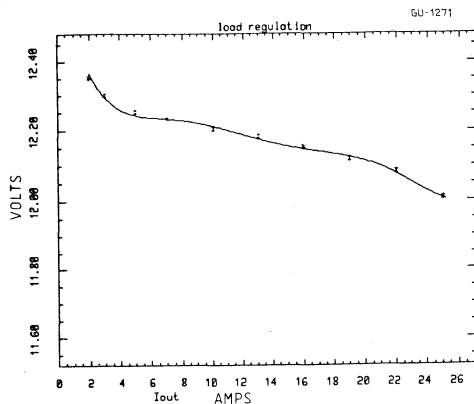
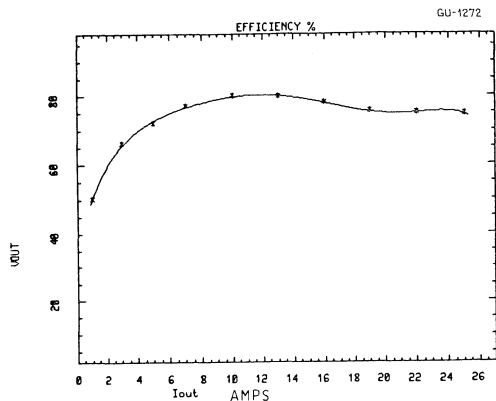


Fig. 8 - Efficiency



CONCLUSION

By using the emitter switching technique this DC-DC converter design uses its switching element to maximum advantage having a very rugged RBSOA and the ability to operate at high frequency. This allows the construction of a compact power supply. The technique also allows high frequency swit-

ching with a relatively simple driving circuit. In addition to these advantages the efficiency of the converter at half and full load under a wide range of input voltages, is acceptable as is the output ripple. The efficiency could be further improved by replacing the fast recovery epitaxial diodes in the secondary winding with Schottky diodes.

APPENDIX - Components list of the circuit diagram in fig. 7

R1 = 220K Ω	R27 = 4.7K Ω 2W	C14 = 1.5 μ F
R2 = 8.2K Ω	R28 = 18m Ω 5W	C15 = 5.6nF 300V
R3 = 507K Ω	R29 = 270 Ω 20W	C16 = 8.2nF 300V
R4 = 47K Ω	R30 = 1.5K Ω 15W	C17 = 47nF
R5 = 18K Ω	R31 = 100 Ω 2W	C18 = 100 μ F 100V
R6 = 1.5K Ω	R32 = 47K Ω	C19 = 100 μ F 100V low E.S.R.
R7 = 15K Ω		C20 = 4.7 μ F
R8 = 470 Ω	Q1 = SGS2N2222A	C21 = 5 $\times$ 4700 μ F 16V low E.S.R.
R9 = 220K Ω	Q2 = SGS2N2907	
R10 = 6.8K Ω	Q3 = SGS2N2222A	D1 = BYW81 - 50A
R11 = 18K Ω	Q4 = SGSP301	D2 = 1N4148
R12 = 8.2K Ω	Q5 = IRFZ42	D3 = 1N4148
R13 = 18K Ω	Q6 = 3 $\times$ BUX12	D4 = BYW80 - 50A
R14 = 19K Ω		D5 = BYTO8P - 300A
R15 = 28.9K Ω	C1 = 350pF	D6 = BYV52 - 50A
R16 = 82K Ω	C2 = 1.5nF	D7 = 4 $\times$ BYW81P - 100A
R17 = 820 Ω 1/2W	C3 = 47nF	D8 = 1N4148
R18 = 82 Ω	C4 = 6.8nF	DZ1 = 1N4112
R19 = 560 Ω	C5 = 6.8nF	
R20 = 47K Ω	C6 = 220pF	IC1 = SGS HCFF 4041B
R21 = 1.5K Ω	C7 = 220pF	IC2 = SGS UC 3840
R22 = 1.8K Ω	C8 = 330pF	
R23 = 2K Ω potentiometer	C9 = 470pF	Tr1 core : Siemens EC 70 N27
R24 = 820 Ω	C10 = 220nF	Tr2 core : Siemens E 20 N30
R25 = 82 Ω	C11 = 47 μ F	L1 core : TDK P2616
R26 = 1.8 Ω 5W	C12 = 470nF	
	C13 = 47 μ F	

HIGH VOLTAGE TRANSISTORS WITH POWER MOS EMITTER SWITCHING

INTRODUCTION

This paper summarizes the results of an investigation carried out on power devices with both MOS and BIPOLAR parts working together in the same circuit. The "emitter drive" configuration was considered, with switching power supply applications in mind.

The devices used are:

Power MOS:	SGSP321, SGSP352
Bipolar transistors:	BUV48, BU508A
Ultrafast bipolar transistors:	SGSD00035
(Hollow Emitter)	SGSD00039
Fast darlington:	SGSD00031, BU810

In the case of flyback switching power supplies a practical example is also described.

CIRCUIT DESCRIPTION

The term "emitter switching" describes a circuit configuration where a low voltage transistor (MOS or Bipolar) switches off the emitter current of a high voltage transistor, and consequently the transistor itself.

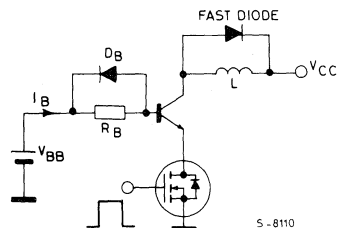
This configuration combines the fast switching of a low voltage device with the high power switching of a high voltage device, since:
high current x high voltage = high power switching.

The combination of a high voltage bipolar and a low voltage Power MOS is preferable due to the high switching speed and the low driving energy of the combined power switch.

The base of the high voltage bipolar device is driven by a constant voltage source. The energy dissipated to drive the high voltage bipolar device depends on the losses that the forward bias current I_{B1} generates in the resistance in series with R_B . $I_{B1}^2 \cdot R_B \cdot t$. This power dissipation can only be reduced by using high gain transistors or darlington.

(See fig. 1)

Fig. 1 - The basic circuit used for the evaluation of the emitter switching system. The base drive circuit used is shown for comparison



The diode in series with the base serves to clamp the base overvoltage at turn-off.

The two transistor stage is driven by the gate of the low voltage Power MOS. Very low driving energies, about 180nJ per cycle, are involved in the charging of the input capacitances.

Consequently the stage can be directly driven by the output of suitable linear integrated circuits.

The possibility of direct driving by an IC output together with the excellent switching speed make this configuration extremely suitable for switching power supplies at frequencies of 50kHz or higher.

CIRCUIT OPERATION

As we have seen, the forward base current I_{B1} is fixed by the external circuitry:

$$I_{B1} = \frac{V_{BB} - V_{BEsat} - V_{Dson}}{R_B}$$

The collector current instead depends on the load, and in general, varies with the time.

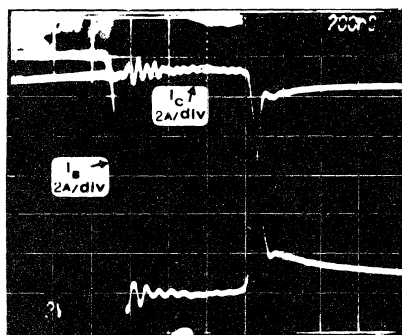
The turn-on and turn-off phases can be analysed separately.

TURN-OFF

When the driving signal to the Power MOS is low the drain current is interrupted and the emitter cur-

rent of the high voltage bipolar falls to zero. The emitter reaches the base voltage and will not carry any more current. As a result the collector current can only flow through the base, becoming a reverse base current that depletes the base to collector junction. This reverse base current I_{B2} , from the moment when the emitter current disappears, coincides with the collector current. See photo 1. The stored charge is removed in a typically very violent, and consequently rapid manner.

Photo 1 - Base and collector current at turn-off



As a result the storage time is substantially reduced.

The fall time, which is related to the recombination under the emitter, is also generally reduced.

Typical values for the fall and storage time of the SGS-Thomson devices used in the test are shown in Table 1, for both emitter and the base drive circuits.

Table 1 - Typical t_i and t_s on inductive load

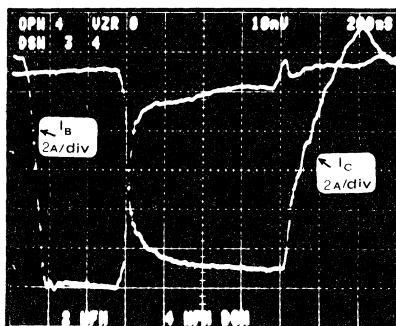
Device	$I_C(A)$	EMITTER SWITCHING		BASE SWITCHING	
		$t_{storage}$	t_{fall}	$t_{storage}$	t_{fall}
BUX48	10	500ns	100ns	2 μ s	200ns
BU508A	5	800ns	300ns	6 μ s	400ns
SGSD00031	10	400ns	100ns	1.2 μ s	100ns
BU810	5	300ns	150ns	800ns	150ns
SGSD00035	10	300ns	50ns	800ns	50ns
SGSD00039	5	300ns	40ns	700ns	50ns

TURN-ON

When the Power MOS is the on state, the bipolar device also starts conducting. The dynamic behaviour (See Photo 2) does not differ in any substan-

tial way from the usual case of the base drive.

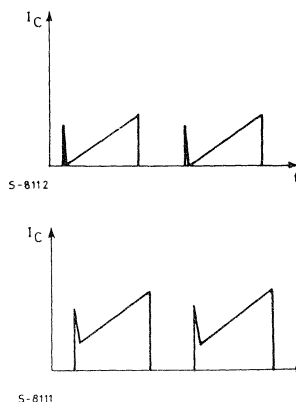
Photo 2 - Base and collector current at turn-on



The dynamic saturation transient $V_{CEsat\ dyn}$ is also practically the same with a base drive as with an emitter drive. The collector current, when the collector load is the primary winding of a switching transformer, can vary according to two possibilities. (See Fig. 2)

- After the initial peak due to the recovery of the diode present on the secondary winding, the collector current increases linearly starting from zero
- After the same initial peak, the collector current increases linearly starting from the value memorized in the magnetic circuit at the end of the previous cycle.

Fig. 2 - Collector current waveforms with varying load



REVERSE BIAS SAFE OPERATING AREA

A problem that occurs in bipolar transistors is damage caused by "current crowding".

Fig. 3a illustrates current flowing in a typical bipolar device. Fig. 3b shows how, when the device is turned off and the current begins to die away, the current focuses with a high concentration under the emitter. This high current density can damage or destroy the transistor.

Fig. 3a

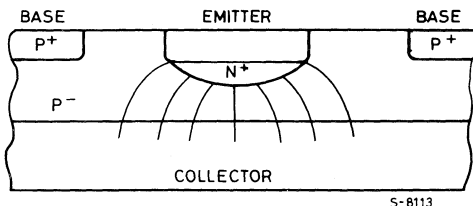
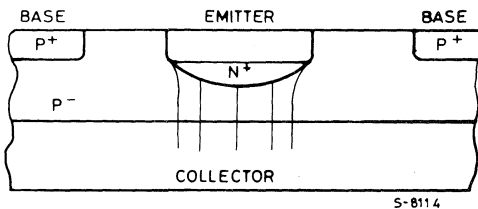


Fig. 3b



The energy dissipated within a bipolar power transistor at turn-off can be found graphically from a plot of I_C versus V_{CE} at turn-off. Three cases are shown in Fig. 4a, b and c. The shaded area is proportional to the energy that is dissipated in the device during turn-off.

Consequently turn-off times affect the SOA of the device, (Fig. 5b). These problems can be overcome using emitter switching.

Fig. 4a -Slow turn-off. No crowding but high average heating

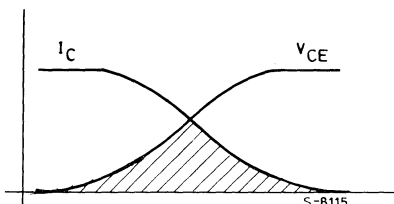


Fig. 4b -Fast turn-off. crowding with low average heating but possible high peak power

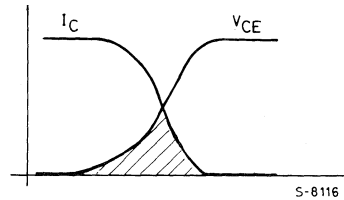
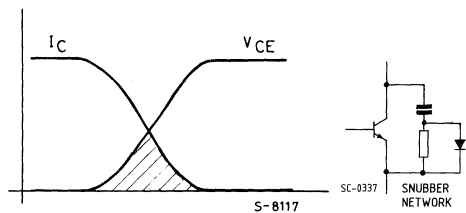


Fig. 4c -Fast turn-off (with V_{CE} delayed by snubber network)



The way the stored charge is swept away in the high voltage bipolar device when it is driven by the emitter, produces some interesting consequences.

The stored charges are evacuated through the base contact when the emitter current is zeroed and not later than a few tens of nanoseconds after the beginning of the storage interval. Consequently, during the turn-off, no charge is injected from the emitter into the base. Although the reverse base current is quite relevant, no focusing of the current in the centre of the emitter fingers takes place.

The bipolar device therefore exhibits an energy absorbing ability at the turn-off RBSOA that is substantially higher than if a normal base drive were used. With a base drive the emitter would inject charges and the voltage drop across the distributed base resistance would induce the "emitter crowding" phenomenon.

The practical evidence for all the transistors investigated (BUV48, BU508A, SGSD00035, SGSD00039) shows that the reverse bias operating area (RBSOA) extends right up to the BV_{CES} ! (See fig. 5).

This extreme effect is unfortunately much less pronounced when using fast darlington. The higher complexity of the charge extraction mechanism and the charge injection from the emitter into the base

in the driver transistor imply that the RBSOA extension is almost irrelevant

Fig. 5a - reverse bias safe operating area

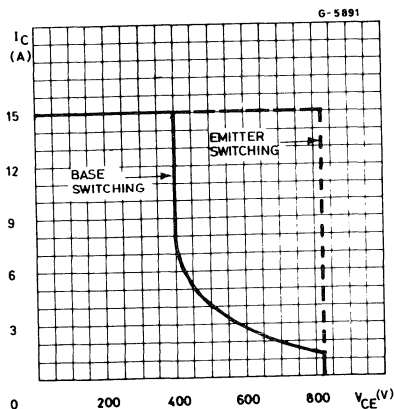
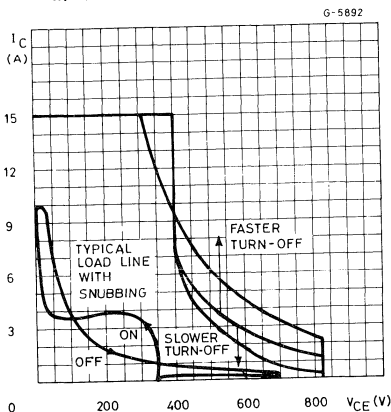


Fig. 5b -How reverse bias safe operating area changes for:
i) slow turn-off
ii) fast turn-off



A POSSIBLE APPLICATION

A possible application of the "emitter switching" configuration is shown in Figure 6, where a switching power supply operating in a "flyback" mode has been implemented.

The basic criteria used in choosing the value of the circuit elements are given below. The purpose of the study was to demonstrate the feasibility and to evaluate the advantages. Exact circuit element values can be further optimized, especially in the case

of the transformer.

The power source in the mains singlephase, 220V a.c., and the switching frequency can be set to 50KHz or more.

The devices used were:

- Q1: fast darlington with $BV_{CES} \geq 600V$ for 110V line
—SGSBU810 for current up to 5A
—SGSD0031 for current above 5A
Fast transistor with $BV_{CES} \geq 800V$ for 220V line
—SGSD00039 for currents up to 5A
—SGSD00035 for current up to 10A
- Q2: Low voltage POWER MOS ($BV_{DSS} = 50V$)
—SGSP352 for currents up to 5A
—SGSP322 for currents over 5A
- Q3: High voltage, low current POWER MOS ($V_{(BR) DSS} < 450V$)

Control

IC: UC3842

DZ2: Zener diode 2W/20V

D1: 25V diode, with I_C peak rating as high as 10A for 500ns

C6: Electrolytic capacitor, 100 μ F, 25V. It absorbs possible variations of V_{BB} .

R3: Resistor setting the forward bias base current of the darlington:

$$R3 = \frac{V_{CE} - V_{BE sat} - V_{DSon} - R_7 I_D}{I_{B1}}$$

Its power rating must exceed $R3 \cdot I_{B2}^2 \cdot t$ (in practice 3W)

R7: Shunt resistor to sense the switch current. The over current $I_{S max}$ protection is set according to

$$R7 = \frac{1V}{I_{Smax}}$$

C4,R6: RC network, filtering the disturbances induced by the switching transients on the I_{Smax} protection input.

C3,R5: RC network, setting the switching frequency and the maximum duty cycle, according to the UC3842 data sheet.

$$t_{charge} = 0.55 R_5 C_3$$

$$t_{discharge} =$$

$$= R_5 \times C_3 \ln [(6.3 R_5 - 2.7)/(6.3 R_5 - 4)]$$

$$f = 1/(t_c + t_d)$$

- R8,R9: Resistive divider of the feedback voltage from a secondary sense winding, rectified by D5 and C5. The divided voltage is compared by the control IC to an internal reference of 2.5V.
- C2,R4: Compensating network in the error amplifier of the feed-back voltage.
- R1: Resistor biasing the Q3 gate (1.2 M Ω , 1/4 W)
- R2: Resistor that limits the inrush current through the POWER MOS, Q3, at the turn-off (1.2 Ω , 2W)
- D4: Fast recovery diode
Its voltage/current ratings depend on the particular secondary winding it rectifies.
- D5: Low current/low voltage diode
- D3,R10, C8: Snubber network (Fig. 6 shows just one of the possible configurations).

$$C8 = \frac{L_d I_c^2}{V_{DS}^2}$$

$$R10 = 1/4fC8$$

$$P(R10) = 1/2 L_d I_D^2 \cdot f$$

where:

f = switching frequency

L_d = stray inductance of the transformer

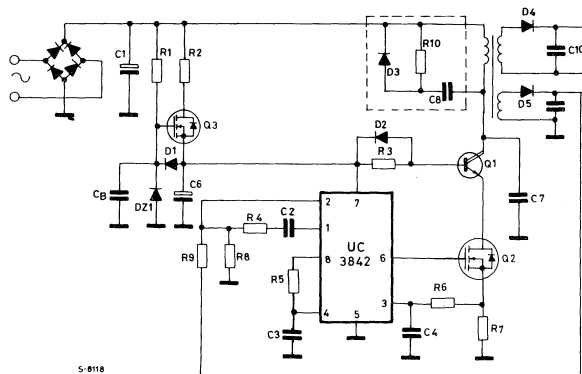
V_{OS} = maximum voltage overshoot admitted

D3: A 400V fast recovery diode

C7: The use of a capacitor reduces the crossover of the Darlington (3 to 6nF)

It is important to note that, the power transistor Q3 acts only at the turn-on of the power supply and when the capacitor C6 supplies more energy to the base of the darlington and to the supply input of the IC than is returned to C6 during the turn-off of the darlington, Q1.

Fig. 6 - "Emitter switching" circuit



CONCLUSION

The "emitter drive" configuration exhibits some clear differences with respect to the usual "base drive" configuration, and they can be particularly useful in switching power supply applications:

- Substantial reduction of the storage time and improvement of the fall time.

Switching frequencies of 50kHz and higher are possible

- The dynamic drive circuitry is simplified. The negative voltage supply is not required to remove the stored charge from the base. The energy needed to drive the gate of the POWER MOS is very low (180 nJ per cycle).

- Extremely high ruggedness at the turn-off of the inductive load (i.e. very large RBSOA) if the high voltage bipolar part is a transistor.
- Higher power dissipation in the on-state, due to the additional losses in the POWER MOS ($I_D^2 R_{DS(on)} t_{on}$).

This last point is the only disadvantage, but it is more than compensated for if switching at high frequencies. The lower switching losses (a saving each cycle) can justify the higher on-state losses (a fixed expenditure) as soon as the switching frequency is high enough, which is often the case in switching power supplies.

LINEAR POWER SUPPLY

POWER SUPPLY DESIGN BASICS

by P. ANTONIAZZI

Aimed at system designers whose interest focusses on other fields, this note reviews the basic power supply design knowhow assumed in the rest of the book.

In mains-supplied electronic systems the AC input voltage must be converted into a DC voltage with the right value and degree of stabilization.

Figures 1 and 2 show the simplest rectifier circuits. In these basic configurations the peak voltage across the load is equal to the peak value of the AC voltage supplied by the transformer's secondary winding. For most applications the output ripple produced by these circuits is too high. However, for some applications - driving small motors or lamps, for example - they are satisfactory.

If a filter capacitor is added after the rectifier diodes the output voltage waveform is improved considerably. Figures 3 and 4 show two classic circuits commonly used to obtain continuous voltages starting from an alternating voltage. The Figure 3 circuit uses a center-tapped transformer with two rectifier diodes while the Figure 4 circuit uses a simple transformer and four rectifier diodes.

Figure 1 : Basic Half Wave Rectifier Circuit.

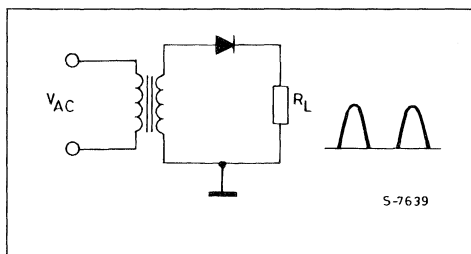


Figure 2 : Full Wave Rectifier Which uses a Center-tapped Transformer.

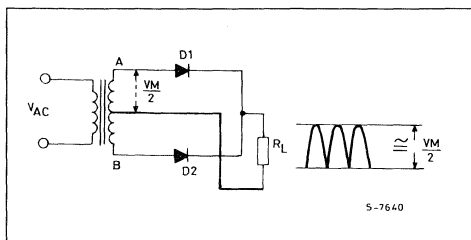


Figure 3 : Full Wave Rectified Output From the Transformer/rectifier Combination is filtered by C1.

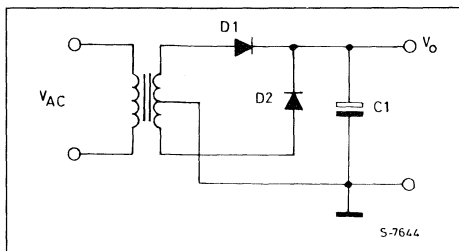


Figure 4 : This Circuit Performs Identically to that Shown in Figure 3.

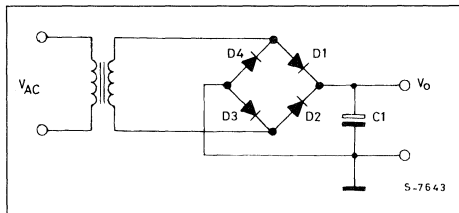


Figure 5 shows the continuous voltage curve obtained by adding a filter capacitor to the Figure 1 circuit. The section b-c is a straight line. During this time it is the filter capacitor that supplies the load current. The slope of this line increases as the current increases, bringing point c lower. Consequently the diode conduction time (c-d) increases, increasing ripple. With zero load current the DC output voltage is equal to the peak value of the rectified AC voltage.

Figure 6 shows how to obtain positive and negative outputs referred to a common ground. Useful design data for this circuit is given in figures 7, 8 and 9. In particular, the curves shown in Figure 7 are helpful in determining the voltage ripple for a given load current and filter capacitor value. The value of the voltage ripple obtained is directly proportional to the load current and inversely proportional to the filter capacitor value.

Figure 5 : Output Waveforms from the Half-wave Rectifier Filter.

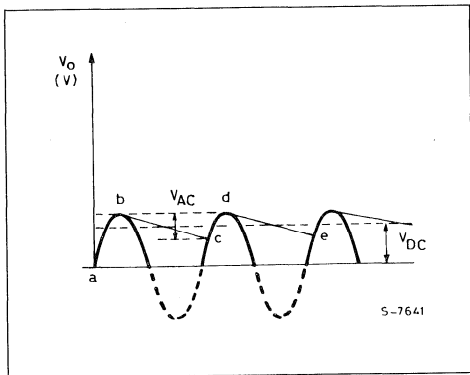


Figure 6 : Full-wave Split Supply Rectifier.

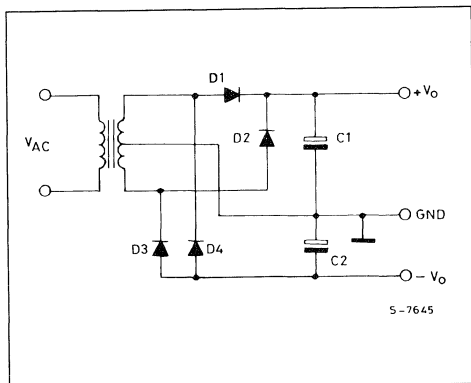


Figure 7 : Ripple Voltage vs. Filter Capacitor Value (full-wave Rectifier).

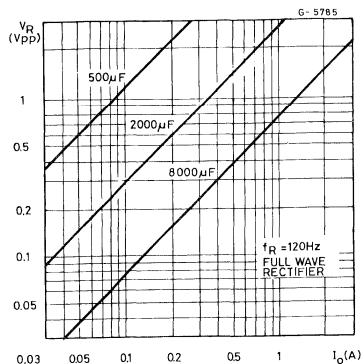


Figure 8 : DC to Peak Ratio for Half Wave rectifiers.

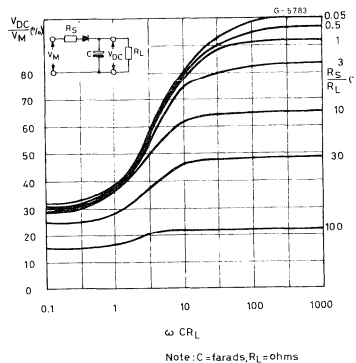


Figure 9 : DC to Peak Ratio for Full-wave Rectifiers.

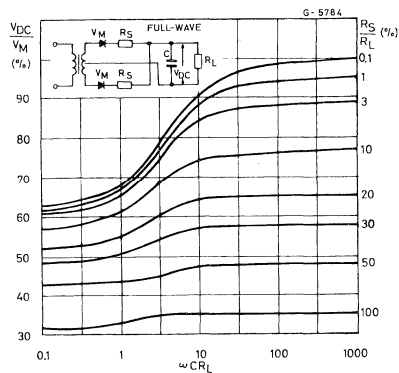


Figure 10 : DC Characteristics of a 50 VA Non-regulated Supply.

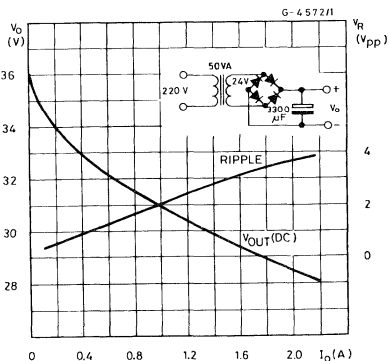


Table 1.

Mains (220V)	Secondary Voltage	DC Output Voltage (V_O)		
		$I_O = 0$	$I_O = 0.1A$	$I_O = 1A$
+ 20%	28.8V	43.2V	42V	37.5V
+ 15%	27.6V	41.4V	40.3V	35.8V
+ 10%	26.4V	39.6V	38.5V	34.2V
	24V	36.2V	35V	31V
- 10%	21.6V	32.4V	31.5V	27.8V
- 15%	20.4V	30.6V	29.8V	26V
- 20%	19.2V	28.8V	28V	24.3V

The performance of a supply commonly used in consumer applications - in audio amplifiers, for example - is described in figure 10 and table 1.

When a low ripple voltage is required an LC filter network may be used. The effect on the output voltage of this addition is shown in figure 11. As figure 11 shows, the residual ripple can be reduced by 40 dB. But often the inductor is costly and bulky.

Often the degree of stability provided by the circuits described above is insufficient and a stabilizer circuit is needed. Figure 12 shows the simplest solution and is satisfactory for loads of up to about 50mA. This circuit is often used as a reference voltage to apply to the base of a transistor of to the input of an op amp to obtain higher output current.

The simplest example of a series regulator is shown in Figure 13. In this circuit the transistor is connected as a voltage follower and the output voltage is about 600 - 700mV lower than the zener voltage. The resistor R must be dimensioned so that the zener is correctly biased and that sufficient base current is supplied to the base of Q1.

For high load currents the base current of Q1 is no longer negligible. To avoid that the current in the zener drops to the point where effective regulation is not possible a darlington may be used in place of the transistor.

When better performance is required the op amp circuit shown in Figure 14 is recommended. In this circuit the output voltage is equal to the reference voltage applied to the input of the op amp. With a suitable output buffer higher currents can be obtained.

The output voltage of the Figure 14 circuit can be varied by adding a variable divider in parallel with the zener diode and with its wiper connected to the op amp's input.

The design of stabilized supplies has been simplified dramatically by the introduction of voltage regulator ICs such as the L78xx and L79xx - three-terminal series regulators which provide a very stable output and include current limiter and

thermal protection functions. Figures 16, 17 and 18 show how these circuits are used. Refer to the data-sheets for more information.

Figure 11 : Ripple Reduction Produced by a Single Section Inductance-capacitance Filter.

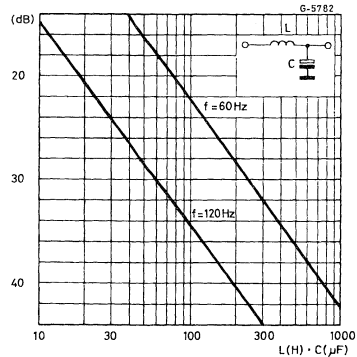


Figure 12 : Basic Zener Regulator Circuit.

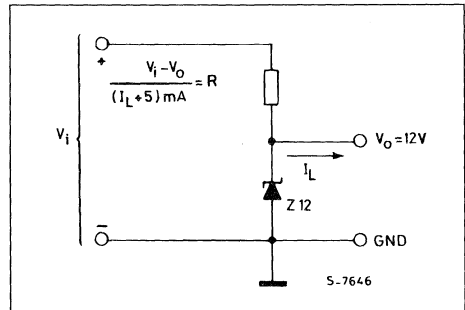


Figure 13 : The Series Pass Zener-based Regulator Circuit can Supply Load Currents up to about 100mA.

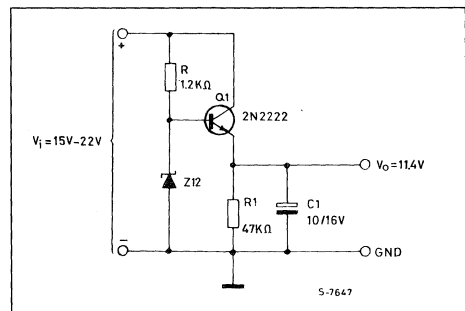


Figure 14 : The Op-amp-based Regulator can Supply 100mA with Excellent Regulation.

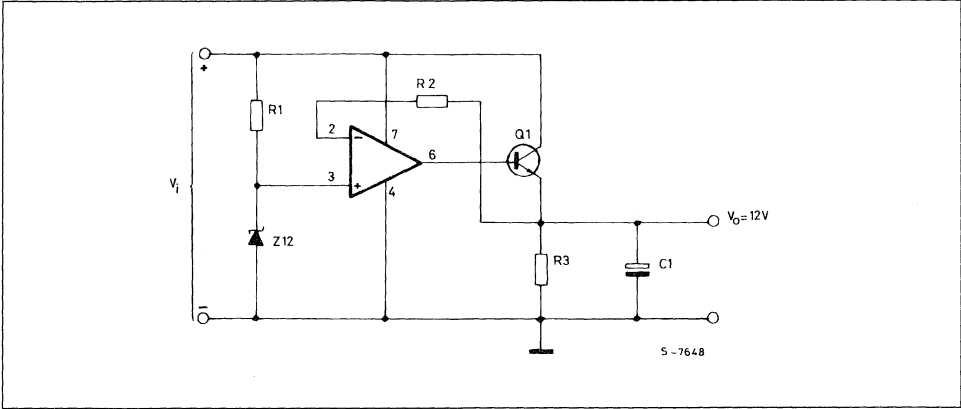


Figure 15 : Zener Regulator Circuit Modified for Low-noise Output.

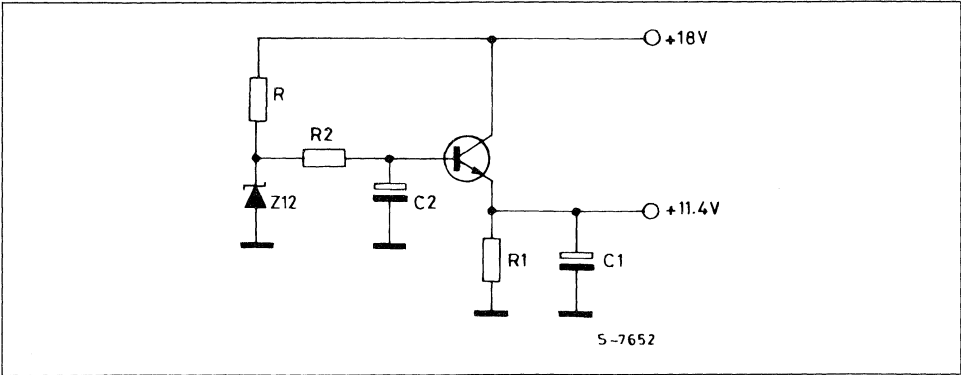


Figure 16 : A Three Terminal 1A Positive Regulator Circuit is very Simple and Performs very Well.

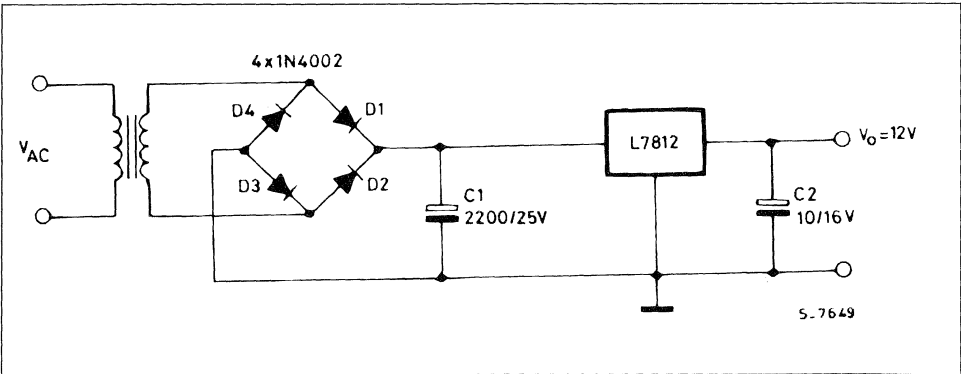
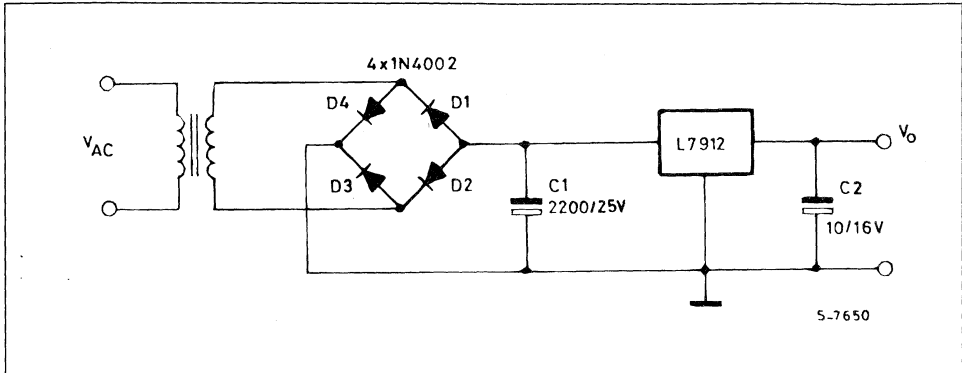
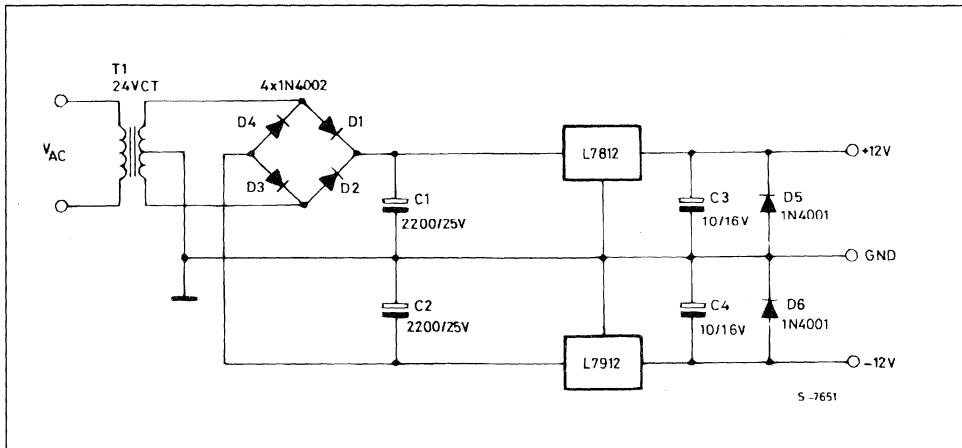


Figure 17 : A Three Terminal 1A Negative Voltage Regulator.**Figure 18** : Complete $\pm 12V - 1A$ Split Supply Regulator Circuit.

VERY LOW DROP REGULATORS ENHANCE SUPPLY PERFORMANCE

By Paolo ANTONIAZZI and Arturo WOLFSGRUBER

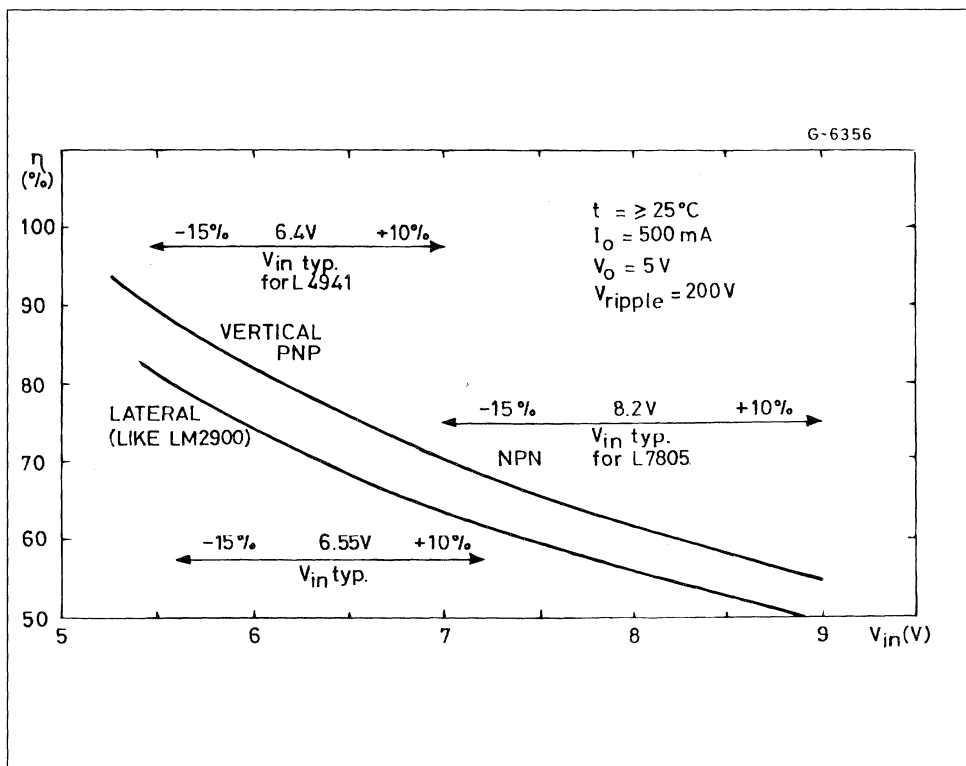
Standard three-terminal voltage regulator ICs use an NPN transistor as the series pass element, so the input-output voltage drop is 1.5V-2V. Low dropout regulators using lateral PNP pass transistors have been available for several years, but a lateral PNP transistor has low gain, so the base current is necessarily high, and a low f_T , so the settling time is poor. Moreover, for stability a large output capacitor is needed.

Applying a new bipolar technology (see APPENDIX : Technology Is The Key) SGS-THOMSON has

developed two 5V low drop voltage regulators that use a new vertical PNP transistor structure to obtain low dropout and low quiescent current.

Type L4940 delivers up to 1.5A and offers an input-output voltage drop of 700mV at the full 1.5A output current. A 1A version, type L4941, has an input-output drop of 450mV at 1A (100mV at 0.1A). Both types have a quiescent current of 15mA at 1A (4mA with no load). Consequently these devices dissipate less power, improving the efficiency of any supply system (figure 1).

Figure 1 : A voltage regulator using vertical isolated PNP transistor is more efficient than regulators with NPN pass transistors because the drop out is lower. And it is more efficient than a regulator having a lateral PNP pass transistor because the quiescent current is lower.



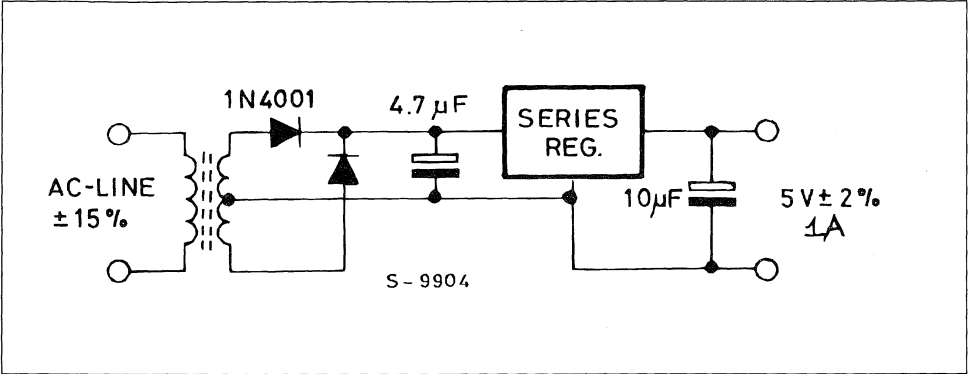
Compared to other "low drop" regulator the L4940 and L4941 have other advantages : regulation performance is guaranteed right down to the minimum input voltage and the device is stable even without an output capacitor. Additionally, a special circuit limits the quiescent current for input voltages from 3V to 5V, typically high for low drop regulators because of the saturation of the series regulator.

The two application areas which benefit the most from second generation low drop regulators like the L4940 and L4941 are post regulation and battery supplies. However, the device brings cost savings in any three-terminal regulator application.

LOW DISSIPATION REDUCES SIZE, WEIGHT & COST

In simple series regulator applications the low dissipation of the L4940/1 reduces the size and weight of the mains transformer, heatsink and printed circuit board. A comparison between equivalent 5V/1A circuits using the L4941 and a standard L7805 regulator (figure 2) shows that the L4941 solution is not only more compact and lighter, it also costs less since the difference in costs between an L4941 and an L7805 is less than the cost saving.

Figure 2 : In simple series regulator applications the L4941 can replace standard three-terminal regulators like the L7805, reducing size, weight and cost. Heat dissipation is reduced, too.



COMPARISON BETWEEN L7805 AND L4941

L4941			L7805	
Component	Value	Cost*	Value	Cost*
Transformer	220V/7.5V 9.4VA	\$4.8	220V/8.6V 11VA	\$5.4
Diodes	2x1N4001	\$0.1	2x1N4001	\$0.1
Capacitors	4.7µF 10V 10µF	\$0.5 \$0.1	4.7µF 16V 100n	\$0.75 \$0.08
Heatsink	20°C/W	\$0.2	10°C/W	\$0.3
PC Area	20cm ²	\$0.27	26cm ²	\$0.35
\$5.97			\$6.98	

The L4941 solution, excluding the cost of the IC, is thus \$1 cheaper. Moreover it is lighter, more compact and dissipates 1.6W less.

* guide price for 1000 pieces.

These low drop regulators also bring important benefits in supplies using post regulation, the technique where one or more linear regulators follow another regulator (often switching), to improve precision, reduce ripple and improve transient response. Though lightweight and cheap, an offline switching regulator suffers from poor load and line regulation and needs additional chokes and capacitors to reduce ripple.

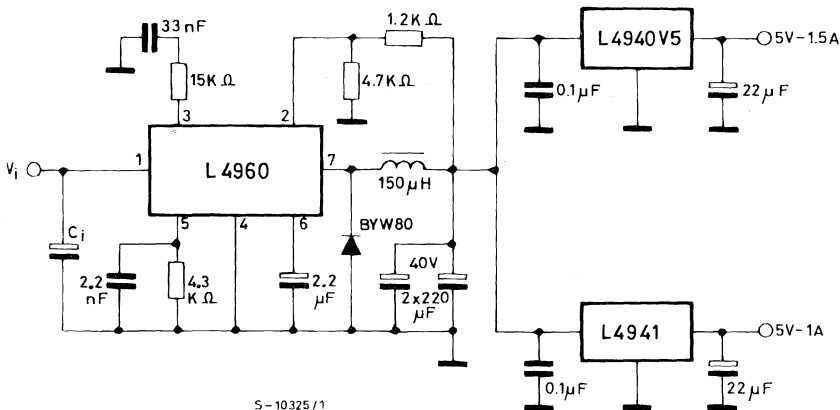
Using standard regulators the efficiency of post regulation systems is low because the intermediate voltage must be high enough to allow for the post regulator's voltage drop. Moreover, a lateral PNP

low drop regulator has a poor transient response so it cannot reject switching ripple effectively.

If L4940s or L4941s are used for post regulation the intermediate voltage need only be 1V above the final output voltage and 40dB SVR can be obtained at 30kHz. Consequently less power is dissipated both in the post regulators and in the pre-regulator, making post regulation much more attractive -- designers can now have the precision, low ripple and fast response without sacrificing efficiency.

Figure 3 shows a typical post-regulation power supply using a switching regulator, based on the L4960, followed by L4941 low drop regulators.

Figure 3 : Low drop regulators like the L4941 improve the efficiency of post regulation supplies because less power is dissipated and because the intermediate voltage can be lower. In this typical supply design an L4960 offline switching regulator is followed by L4941 post regulators, giving an high overall efficiency.



IMPROVING BATTERY SUPPLIES

The second application area where the L4940 and L4941 are particularly useful is in battery-powered equipment. Because of their lower dropout these devices need fewer battery cells -- five, compared to the six needed for an NPN regulator. In addition, with five NiCd cells the efficiency is 77-96% and the cells can be completely discharged.

The low quiescent current of the L4940 and L4941 reduces power consumption, prolonging battery life. Moreover, since they will continue to provide a stable 5V output with input voltages as low as 5.45V they also extend the effective battery life by allowing continued operation when the battery would previously have been discarded (figure 4).

Figure 4 : The vertical PNP pass transistor permits a minimum dropout without the penalty of higher quiescent current, giving a 30-50% longer battery life in equipment drawing a constant current two hours a day.

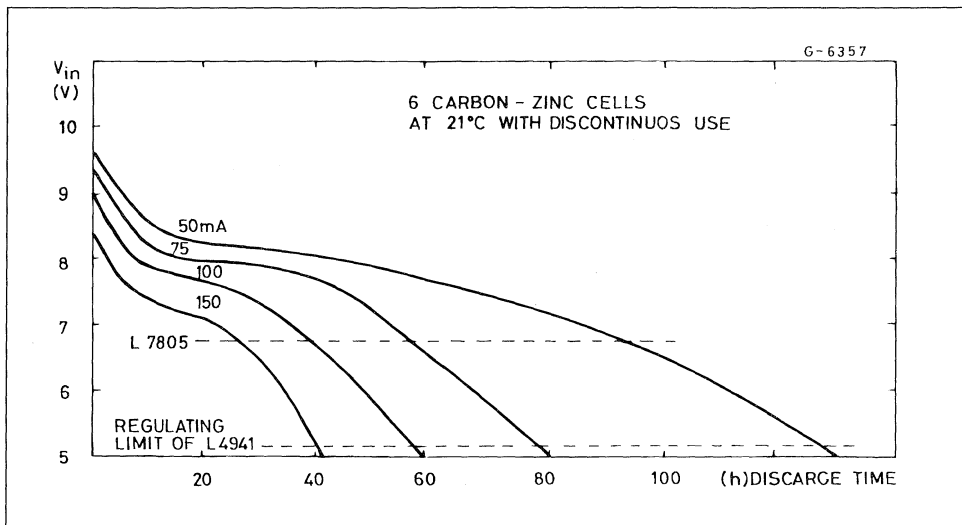
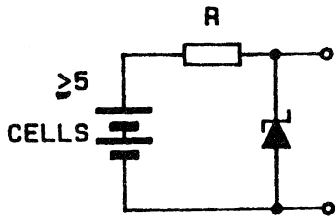
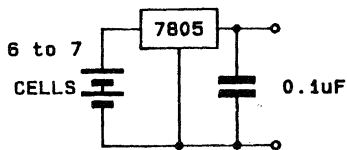


Figure 5 shows how an L4941 solution compares with five alternative 5V battery supplies.

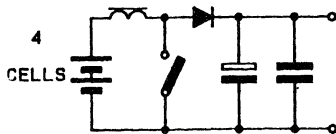
Figure 5 : The L4941 is also useful in battery-powered equipment, prolonging battery life by reducing current drain and supplying a regulated 5V output until the battery voltage has fallen to 5.45V. Here the L4941 solution is compared with five alternatives.



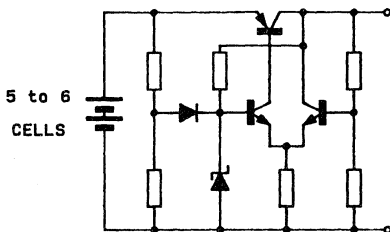
1. ZENER REGULATOR -- High current consumption when battery fully charged and high losses in R_{ser} .



2. NPN SERIES REGULATOR -- Needs at least 7Znn/C, 6NiCd or 4Pd cells..

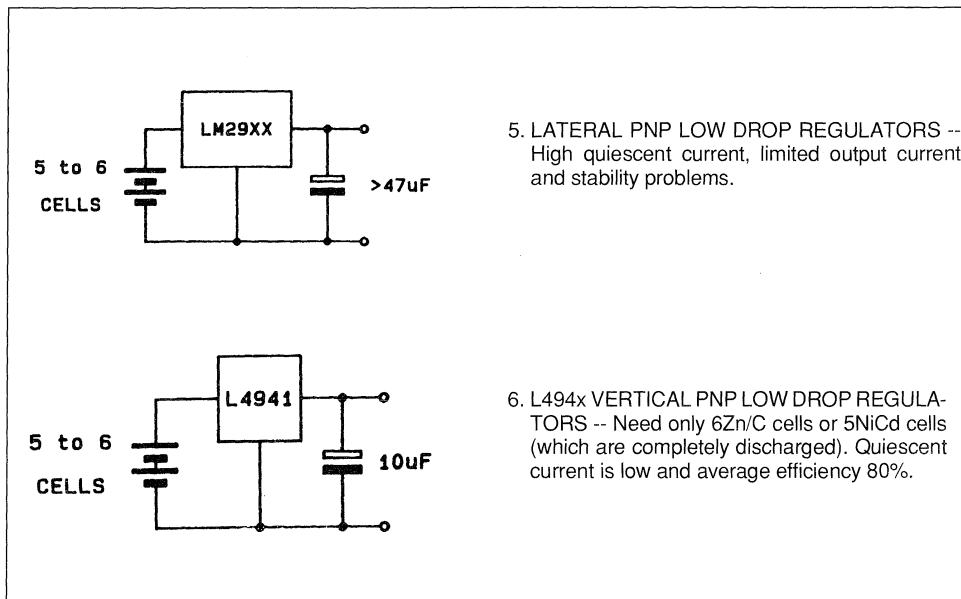


3. DC-DC CONVERTERS -- Complicated and costly. Generates EMI and average efficiency $\Leftarrow 75\%$.



4. DISCRETE LOW DROP REGULATOR -- Bulky and performs poorly in comparison with integrated solutions.

Figure 5 (continued).



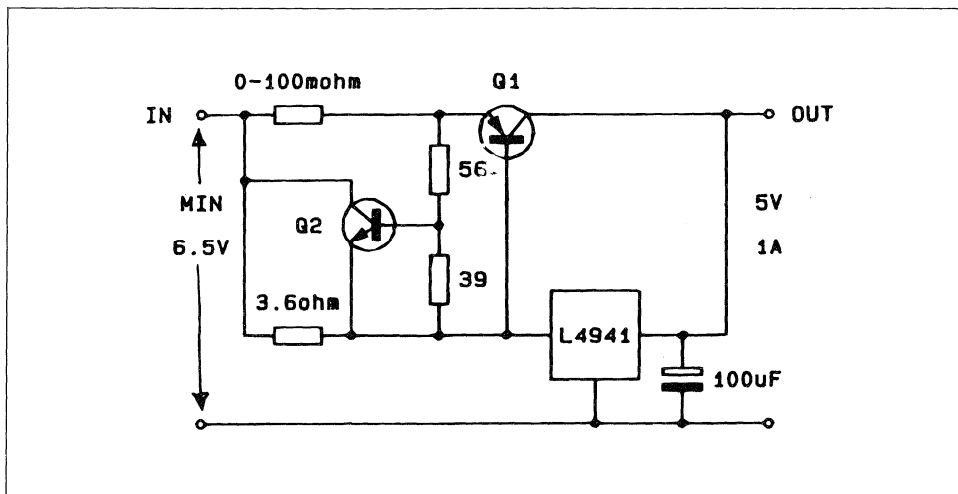
HIGHER CURRENT

To obtain more than 1.5A output current a discrete PNP transistor can be added to the L4940 as shown in figure 6. In this circuit Q2 is a current limiter to protect the external transistor.

test the external pass transistor when the output is short circuited. An on-chip protection circuit prevents damage to the L4940.

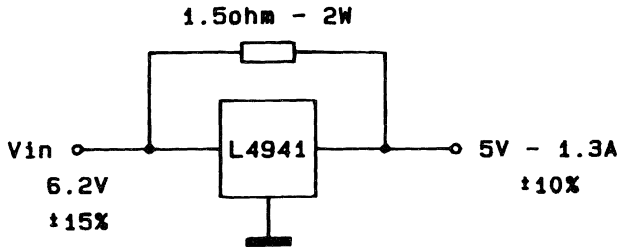
When the load current does not vary greatly higher

Figure 6 : An external PNP transistor can be added to the L4941 to obtain higher output current. Q2 is a current limiter to protect the external transistor.



output current can also be obtained by using a shunt resistor as shown in figure 7.

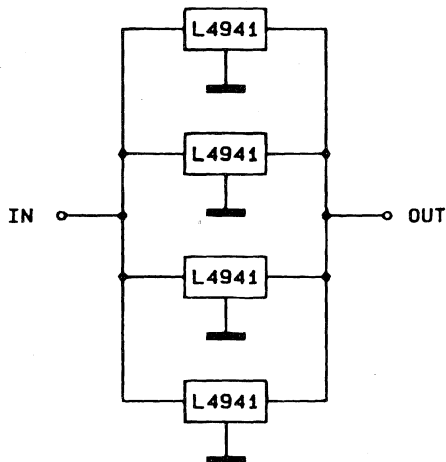
Figure 7 : If the load current does not vary much a simple way to obtain higher current is to add a shunt resistor.



Another way to obtain higher current is simply to connect several devices in parallel as shown in figure 8. This solution also increases the overall re-

liability of the system and is useful also when reliability is of prime importance.

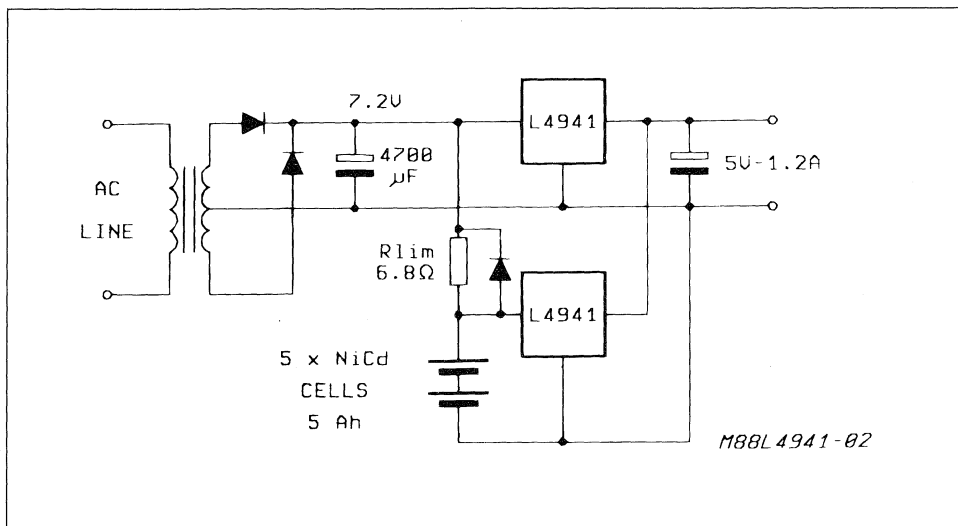
Figure 8 : Multiple L4941s can be paralleled to increase both output current and reliability.



Finally, higher current can be obtained with two devices in parallel connected to parallel sources (figure 9). This circuit provides an uninterruptable 1.2A/5V

output by paralleling the normal line input with a backup battery, which is charged through Rlim when the AC input is present.

Figure 9 : Connecting two L4941s in parallel with an AC input and a battery yields an efficient 1.2A/5V uninterruptable supply.

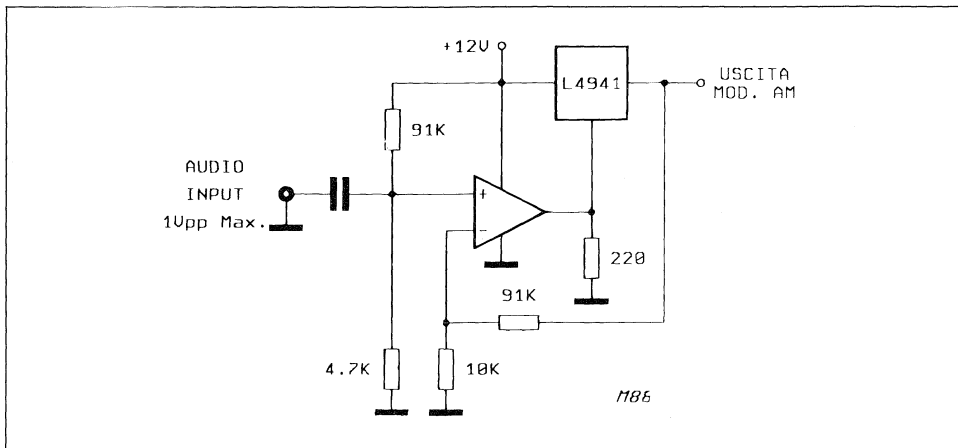


USING THE L4941 AS A MODULATOR

Apart from power supply applications, the L4941 can be used as a modulator (figure 10). The modulator part of this circuit is also useful in the lab as a supply for SVR measurements or generally as a

basic circuit for an amplifier or generator driving resistive loads. The average output voltage can be varied by adjusting the divider on the non-inverting input of the op amp.

Figure 10 : The L4941 can be used as a modulator as illustrated in this circuit.



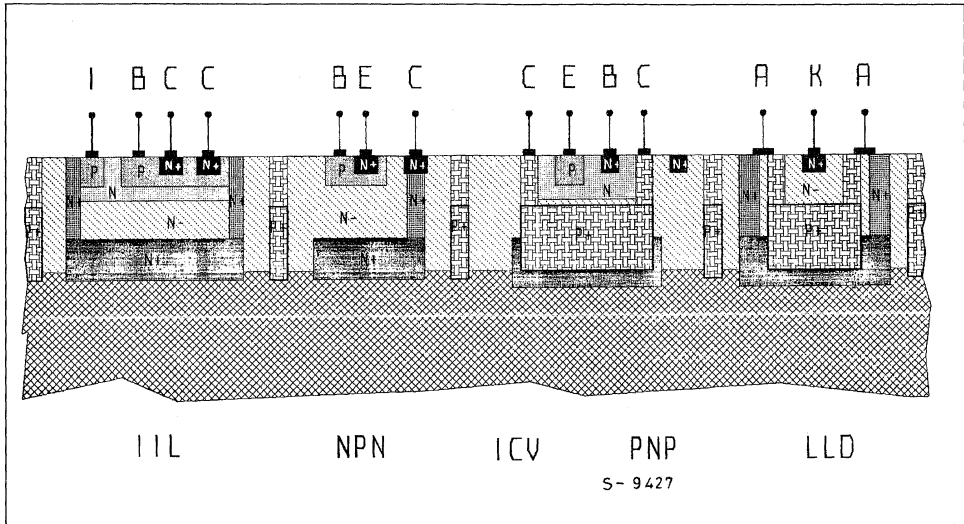
APPENDIX : TECHNOLOGY IS THE KEY

In parallel with the emergence of mixed bipolar/DMOS processes, pure bipolar technology has made significant advances, too. One of the most important of these advances ? the development of a new power PNP transistor structure -- the isolated collector vertical PNP (ICV PNP) -- which is similar in performance to NPN power transistors.

The ICV PNP is a key element in the SGS-THOM-

SON MICROELECTRONICS Multipower-HDS² P² (HDS² P² = High Density Super Signal/Power Process) used to design the L4940 & L4941 low drop regulators, a 20V "Multipower" process which offers NPN & ICV PNP power transistors, small signal NPN & PNP transistors, IIL logic, ECL logic and a new low leakage diode structure (see fig. 11).

Figure 11 : Multipower bipolar process with new ICV-PNP (isolated collector vertical PNP), similar in performance to NPN power transistors.



This process is characterized by an exceptionally high current density -- 6A/mm² for NPN transistors ; 2A/mm² for PNP transistors (at V_{SAT} = 1V, H_{FE} = 10) -- and very high density in the signal processing section.

Thanks to the ICV PNP power transistor structure, designers can choose any output configuration -- low side, high side, half bridge, bridge. In addition, the low voltage drop of the ICV PNP is very useful in applications where the dropout voltage is critical - in voltage regulators and automotive solenoid drivers, for example.

Another new structure offered by Multipower-HDS² P², the Low Leakage Diode (LLD) is very useful in power ICs driving inductive loads. With a parasitic PNP gain about four orders of magnitude lower than

conventional diodes, the LLDs reduce dissipation in the chip -- always an important consideration in power IC design.

Multipower-HDS² P² can be applied in simple products where an ICV PNP output stage is needed such as the L4941. Moreover, because it allows the integration of very complex control circuits it is also used for power ICs which integrate a complete power subsystem such as the L6217, a single chip microstepping drive for stepper motors.

A similar process rated at 60V -- Multipower-S² P² -- has also been developed. While Multipower-HDS² P² is aimed at low voltage, high complexity applications, Multipower-S² P² is intended for higher voltage applications with medium complexity control circuits.

A DESIGNER'S GUIDE TO THE L200 VOLTAGE REGULATOR

Delivering 2 A at a voltage variable from 2.85 V to 36 V, the L200 voltage regulator is a versatile device that simplifies the design of linear supplies. This design guide describes the operation of the device and its applications.

The introduction of integrated regulator circuits has greatly simplified the work involved in designing supplies. Regulation and protection circuits required for the supply, previously realized using discrete components, are now integrated in a single chip. This had led to significant cost and space saving as well as increased reliability. Today the designer has a wide range of fixed and adjustable, positive and negative series regulators to choose from as well as an increasing number of switching regulators.

The L200 is a positive variable voltage regulator which includes a current limiter and supplies up to 2 A at 2.85 to 36 V.

The output voltage is fixed with two resistors or, if a continuously variable output voltage is required, with one fixed and one variable resistor.

The maximum output current is fixed with a low value resistor. The device has all the characteristics common to normal fixed regulators and these are described in the datasheet. The L200 is particularly suitable for applications requiring output voltage variation or when a voltage not provided by the standard regulators is required or when a special limit must be placed on the output current.

The L200 is available in two packages :

Pentawatt - Offers easy assembly and good reliability. The guaranteed thermal resistance ($R_{th(j-case)}$) is 3 °C/W (typically 2 °C/W) while if the device is used without heatsink we can consider a guaranteed junction-ambient thermal resistance of 50 °C/W.

TO-3 - For professional and military use or where good hermeticity is required.

The guaranteed junction-case thermal resistance is 4 °C/W, while the junction-ambient thermal resistance is 35 °C/W.

The junction-case thermal resistance of this package, which is greater than that of the Pentawatt, is

partly compensated by the lower contact resistance with the heatsink, especially when an electrical insulator is used.

CIRCUIT OPERATION

As can be seen from the block diagram (fig. 1) the voltage regulation loop is almost identical to that of fixed regulators. The only difference is that the negative feedback network is external, so it can be varied (fig. 3). The output is linked to the reference by :

$$V_{out} = V_{ref} \left(1 + \frac{R_2}{R_1} \right) \quad (1)$$

Considering V_{out} as the output of an operational amplifier with gain equal to $G_V = 1 + R_2/R_1$ and input signal equal to V_{ref} , variability of the output voltage can be obtained by varying R_1 or R_2 (or both). It's best to vary R_1 because in this way the current in resistors R_1 and R_2 remains constant (this current is in fact given by V_{ref}/R_1).

Equation (1) can also be found in another way which is more useful in order to understand the descriptions of the applications discussed.

$$V_{out} = R_1 i_1 + R_2 i_2$$

and since in practice $i_1 \gg i_4$ (i_4 has a typical value of 10 μ A) we can say that

$$V_{out} + R_1 i_1 + R_2 i_1 \text{ with } i_1 = \frac{V_{ref}}{R_1}$$

Therefore

$$V_{out} = \frac{R_2}{R_1} V_{ref} + V_{ref} = V_{ref} \left(1 + \frac{R_2}{R_1} \right)$$

In other words R_1 fixes the value of the current circulating in R_2 so R_2 is determined.

Figure 1 : Block Diagram.

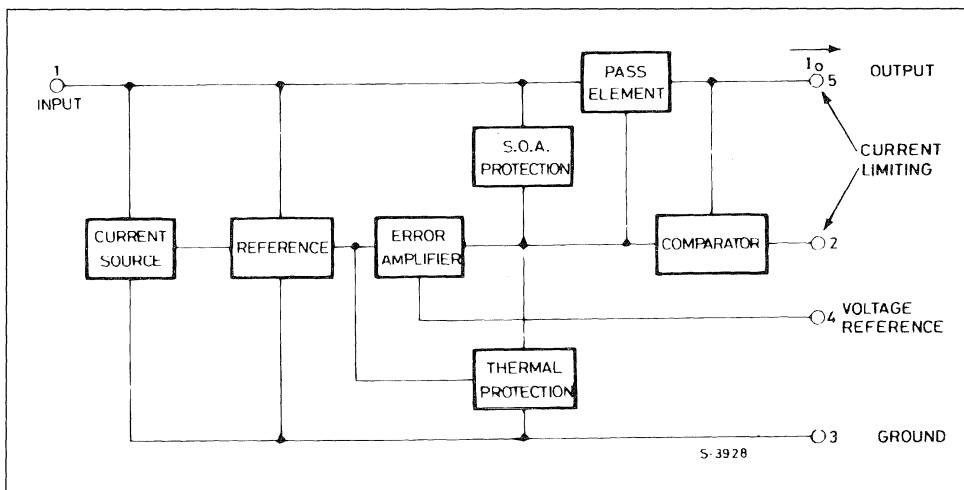


Figure 2 : Schematic Diagram.

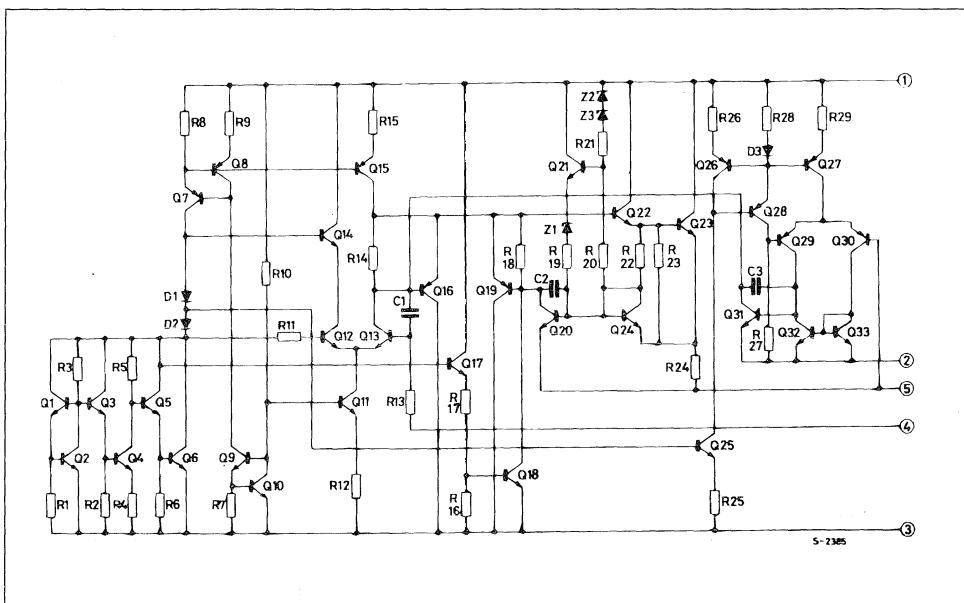
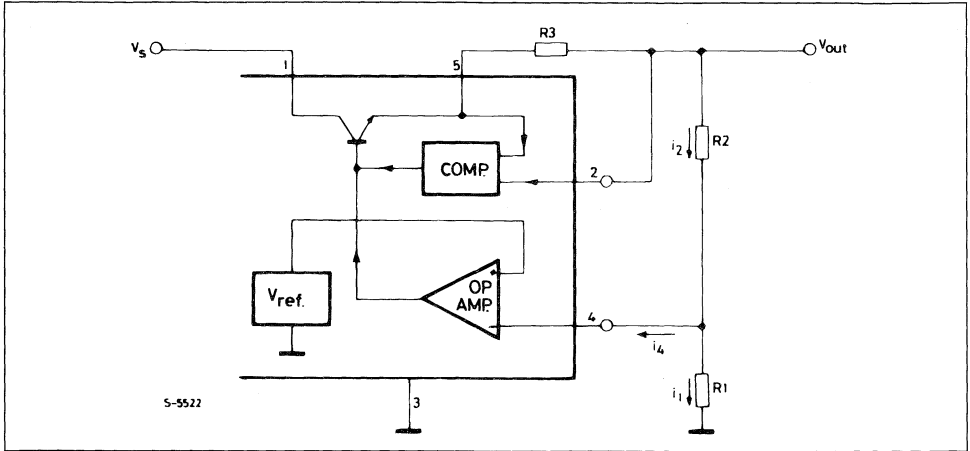


Figure 3.

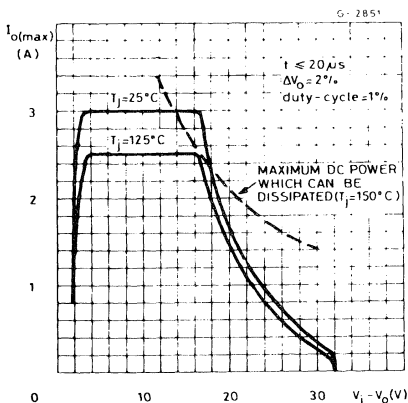


OVERLOAD PROTECTION

The device has an overload protection circuit which limits the current available.

Referring to fig. 2, R24 operates as a current sensor. When at the terminals of R24 there is a voltage drop sufficient to make Q20 conduct, Q19 begins to draw current from the base of the power transistor (darlington formed by Q22 and Q23) and the output current is limited. The limit depends on the current which Q21 injects into the base of Q20. This current depends on the drop-out and the temperature which explains the trend of the curves in fig. 4.

Figure 4.



THERMAL PROTECTION

The junction temperature of the device may reach destructive levels during a short circuit at the output or due to an abnormal increase in the ambient temperature. To avoid having to use heatsinks which are costly and bulky, a thermal protection circuit has been introduced to limit the output current so that the dissipated power does not bring the junction temperature above the values allowed. The operation of this circuit can be summarized as follows.

In Q17 there is a constant current equal to :

$$\frac{V_{ref} - V_{BE17}}{R17 + R16} \quad (V_{ref} = 2.75 \text{ V typ})$$

The base of Q18 is therefore biased at :

$$V_{BE18} = \frac{V_{ref} - V_{BE17}}{R16 + R17} \cdot R16 \approx 350 \text{ mV}$$

Therefore at $T_j = 25^\circ\text{C}$ Q18 is off (since 600 mV is needed for it to start conducting). Since the V_{BE} of a silicon transistor decreases by about 2 mV/ $^\circ\text{C}$, Q18 starts conducting at the junction temperature :

$$T_j = \frac{600 - 350}{2} + 25 = 150^\circ\text{C}$$

CURRENT LIMITATION

The innovative feature of this device is the possibility of acting on the current regulation loop, i.e. of limiting the maximum current that can be supplied to the desired value by using a simple resistor (R3 in fig. 2). Obviously if $R3 = 0$ the maximum output cur-

rent is also the maximum current that the device can supply because of its internal limitation.

The current loop consists of a comparator circuit with fixed threshold whose value is V_{SC} . This comparator intervenes when $I_o \cdot R3 = V_{SC}$, hence

$$I_o = \frac{V_{SC}}{R3} \quad (V_{SC} \text{ is the voltage between pin 5 and 2 with typical value of } 0.45 \text{ V}).$$

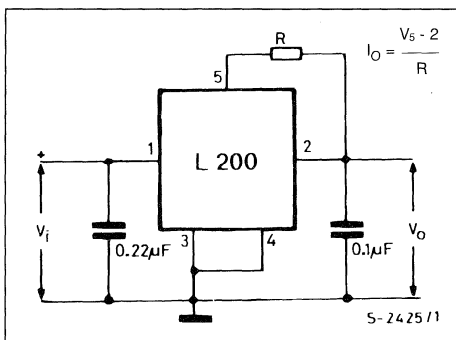
Special attention has been given to the comparator circuit in order to ensure that the device behaves as a current generator with high output impedance.

TYPICAL APPLICATIONS

PROGRAMMABLE CURRENT REGULATOR

Fig. 5 shows the device used as current generator. In this case the error amplifier is disabled by short-circuiting pin 4 to ground.

Figure 5.



The output current I_o is fixed by means of R :

$$I_o = \frac{V_{S-2}}{R}$$

The output voltage can reach a maximum value $V_i - V_{drop} \approx V_i - 2 \text{ V}$ (V_{drop} depends on I_o).

PROGRAMMABLE VOLTAGE REGULATOR

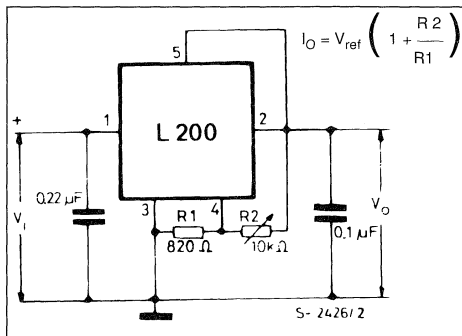
Fig. 6 shows the device connected as a voltage regulator and the maximum output current is the maximum current that the device can supply. The output voltage V_o is fixed using potentiometer $R2$. The equation which gives the output voltage is as follows :

$$V_o = V_{ref} \left(1 + \frac{R2}{R1} \right)$$

By substituting the potentiometer with a fixed resistor and choosing suitable values for $R1$ and $R2$, it is

possible to obtain a wide range of fixed output voltages.

Figure 6.



The following formulas and tables can be used to calculate some of the most common output voltages.

Having fixed a certain V_o , using the previous formula, the maximum value is :

$$V_{O \max} = V_{ref \max} \left(1 + \frac{R2_{\max}}{R1_{\min}} \right) \text{ and the}$$

minimum value is :

$$V_{O \min} = V_{ref \min} \left(1 + \frac{R2_{\min}}{R1_{\max}} \right)$$

The table below indicates resistor values for typical output voltages :

$V_o \pm 4 \%$	$R1 \pm 1 \%$	$R2 \pm 1 \%$
5 V	1.5 kΩ	1.2 kΩ
12 V	1 kΩ	3.3 kΩ
15 V	750 Ω	3.3 kΩ
18 V	330 Ω	1.8 kΩ
24 V	510 Ω	3.9 kΩ

PROGRAMMABLE CURRENT AND VOLTAGE REGULATOR

The typical configuration used by the device as a voltage regulator with external current limitation is shown in fig. 7. The fixed voltage of 2.77 V at the terminals of $R1$ makes it possible to force a constant current across variable resistor $R2$. If $R2$ is varied, the voltage at pin 2 is varied and so is the output voltage.

The output voltage is given by :

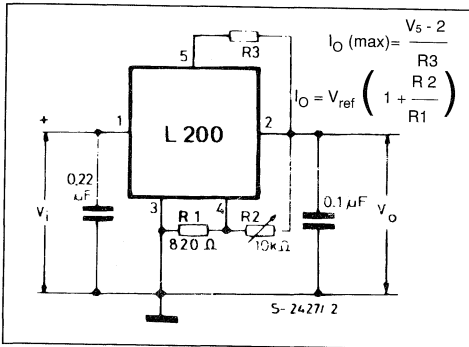
$$V_O = V_{ref} \cdot \left(1 + \frac{R_2}{R_1}\right), \text{ with } V_{ref} = 2.77 \text{ V typ}$$

and the maximum output current is given by :

$$I_{O \max} = \frac{V_{5-2}}{R_3} \text{ with } V_{5-2} = 0.45 \text{ V typ.}$$

To maintain a sufficient current for good regulation the value of R_1 should be kept low. When there is no load, the output current is V_{ref}/R_1 . Suitable values of R_1 are between 500Ω and $1.5 \text{ k}\Omega$. If the load is always present the maximum value for R_1 is limited by the current value ($10 \mu\text{A}$) at the input of the error amplifier (pin 4).

Figure 7.



DIGITALLY SELECTED REGULATOR WITH INHIBIT

The output voltage of the device can be regulated digitally as shown in fig. 8. The output voltage depends on the divider formed by R_5 and a combination of R_1 , R_2 , R_3 and P_2 . The device can be switched off with a transistor.

When the inhibit transistor is saturated, pin 2 is brought to ground potential and the output voltage does not exceed 0.45 V.

REDUCING POWER DISSIPATION WITH DROPPING RESISTOR

It may sometimes be advisable to reduce the power dissipated by the device. A simple and economic method of doing this is to use a resistor connected in series to the input as shown in fig. 9. The input-output differential voltage on the device is thus reduced.

The formula for calculating R is as follows :

$$R = \frac{V_{i \min} - (V_O + V_{drop})}{I_O}$$

Figure 8.

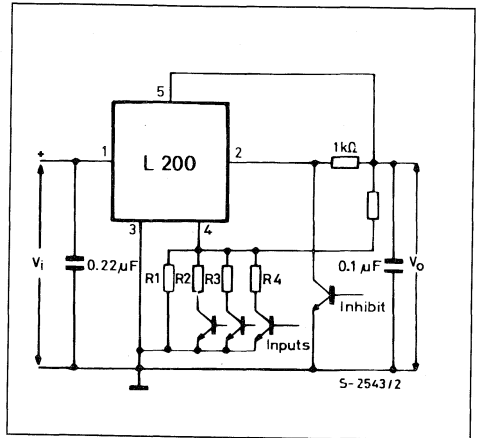
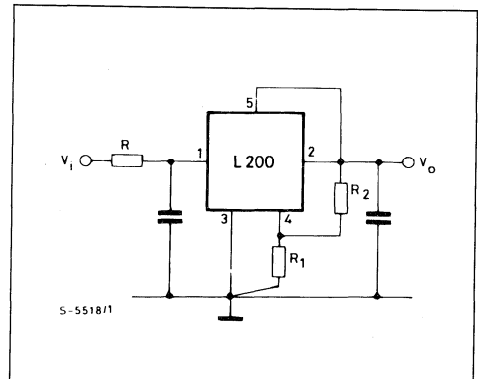


Figure 9.

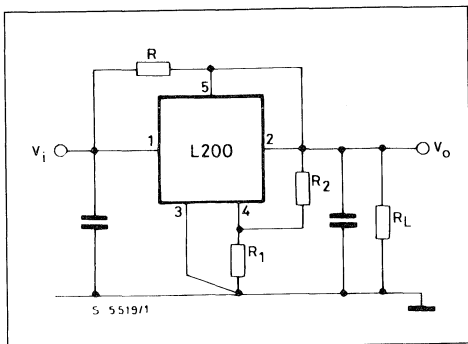


Where V_{drop} is the minimum differential voltage between the input and the output of the device at current I_O . $V_{i \min}$ is the minimum voltage. V_O is the output voltage and I_O the output current.

With constant load, resistor R can be connected between pins 1 and 2 of the IC instead of in series with the input (fig. 10). In this way, part of the load current flows through the device and part through the resistor. This configuration can be used when the minimum current by the load is :

$$I_{O \min} = \frac{V_{drop}}{R} \quad (\text{instant by instant})$$

Figure 10.



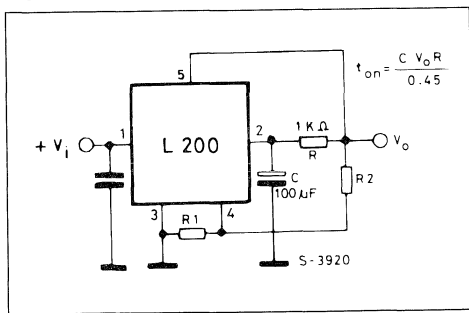
SOFT START

When a slow rise time of the output voltage is required, the configuration in fig. 11 can be used. The rise time can be found using the following formula :

$$t_{on} = \frac{CV_o R}{0.45}$$

At switch on capacitor C is discharged and it keeps the voltage at pin 2 low ; or rather, since a voltage of more than 0.45 V cannot be generated between pins 5 and 2, the V_o follows the voltage at pin 2 at less than 0.45 V.

Figure 11.



Capacitor C is charged by the constant current i_c .

$$i_c = \frac{V_{sc}}{R}$$

Therefore the output reaches its nominal value after the time t_{on} :

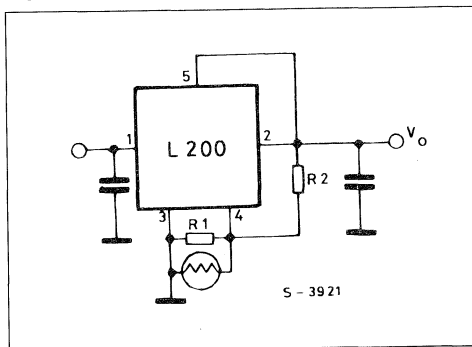
$$V_o - V_{sc} = \frac{i_c \cdot t_{on}}{C}$$

$$t_{on} = C \cdot \frac{V_o - 0.45}{0.45} \cdot R \cong \frac{CV_o R}{0.45}$$

LIGHT CONTROLLER

Fig. 12 shows a circuit in which the output voltage is controlled by the brightness of the surrounding environment. Regulation is by means of a photo resistor in parallel with R_1 . In this case, the output voltage increases as the brightness increases. The opposite effect, i.e. dimming the light as the ambient light increases, can be obtained by connecting the photoresistor in parallel with R_2 .

Figure 12.



LIGHT DIMMER FOR CAR DISPLAY

Although digital displays in cars are often more aesthetically pleasing and frequently more easily read they do have a problem. Under varying ambient light conditions they are either lost in the background or alternatively appear so bright as to distract the driver. With the system proposed here, this problem is overcome by automatically adjusting the display brightness during daylight conditions and by giving the driver control over the brightness during dusk and darkness conditions.

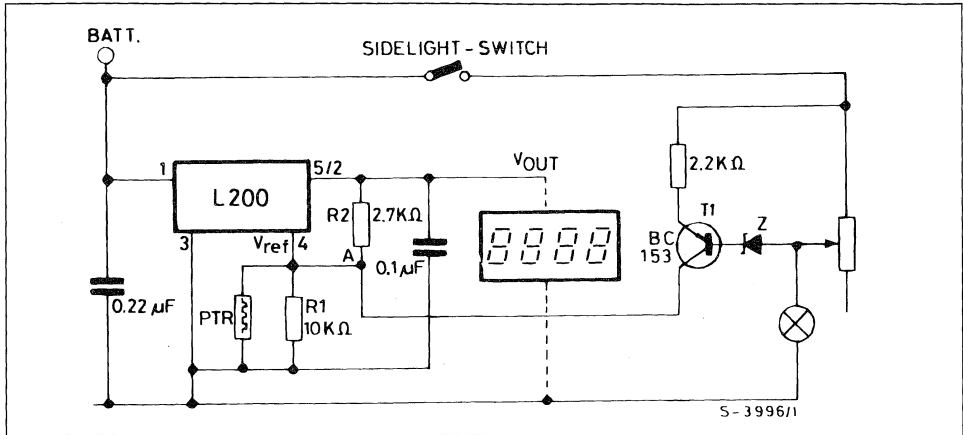
The circuit is shown in fig. 13. The primary supply is shown taken straight from the car battery however it is worth noting that in a car there is always the risk of dump voltages up to 120 V and it is recommended that some form of protection is included against this.

Under daylight conditions i.e. with sidelights off and T1 not conducting the output of the device is determined by the values of R_1 , R_2 and the photoresistor (PTR). The output voltage is given by

$$V_{out} = V_{ref} \left(1 + \frac{R_2}{PTR/R_1} \right)$$

If the ambient light intensity is high, the resistance of the photoresistor will be low and therefore V_{out} will be high. As the light decreases, so V_{out} decreases dimming the display to a suitable level.

Figure 13.



In dusk conditions, when the sidelights are switched on, T1 starts to conduct with its conduction set by the potentiometer wiper at its uppermost position the sidelights are at their brightest and current through T1 would be a minimum. With the wiper at its lowest position obviously the opposite conditions apply.

The current through T1 is felt at the summing node A along with the currents through R2 and the parallel network R1, PTR. Since V_{ref} is constant the current flowing through R1, PTR must also be constant. Therefore any change in the current through T1 causes an equal and opposite change in the current through R2. Therefore as I_{T1} increases, V_{out} decreases i.e. as the brightness of the side-lights is increased or decreased so is the brightness of the display.

The values of R2 and PTR should be selected to give the desired minimum and maximum brightness levels desired under both automatic and manual conditions although the minimum brightness under manual conditions can also be set by the maximum current flowing through T1 and, in any case, this should not exceed the maximum current through R2 under automatic operation.

The circuit shown with a small modification can also be used for dimmers other than in a car. Fig. 15 shows the modification needed. The zener diode should have a $V_F \geq 2.5$ V at $I = 10$ μ A.

HIGHER INPUT OR OUTPUT VOLTAGES

Certain applications may require higher input or output voltages than the device can produce. The problem can be solved by bringing the regulator back

Figure 14.

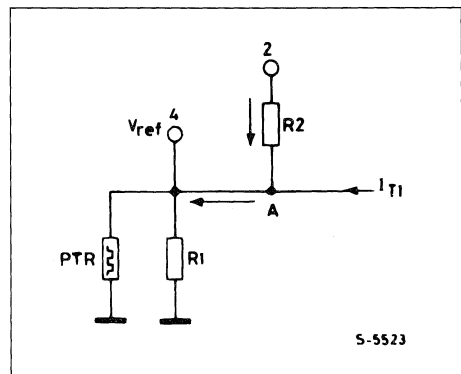
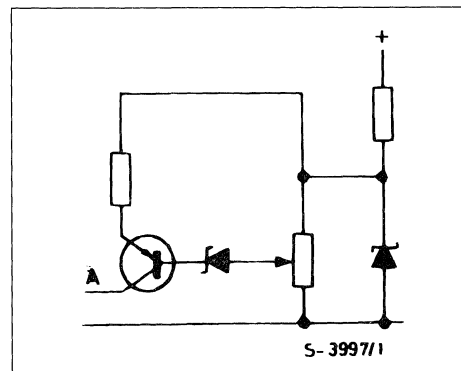


Figure 15.



into the normal operating units with the help of external components.

When there are high input voltages, the excess voltage must be absorbed with a transistor. Figs. 16 and 17 show the two circuits :

Figure 16.

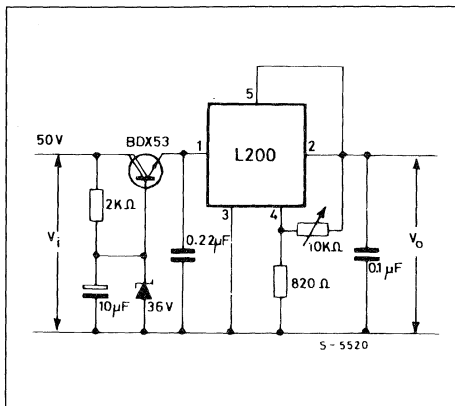
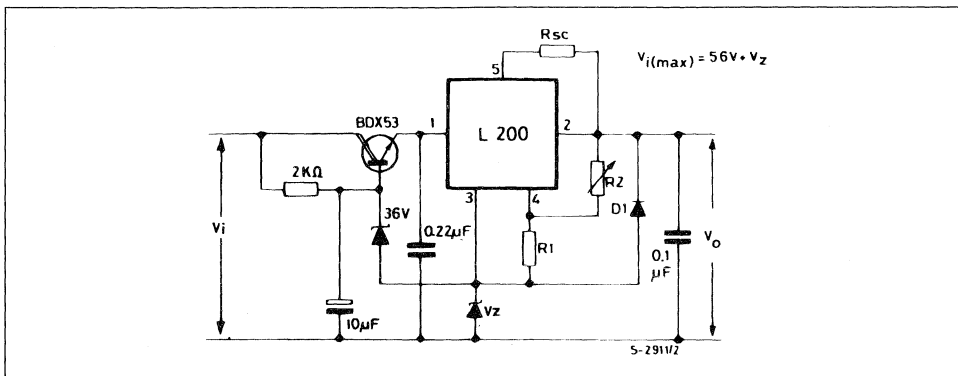


Figure 18.

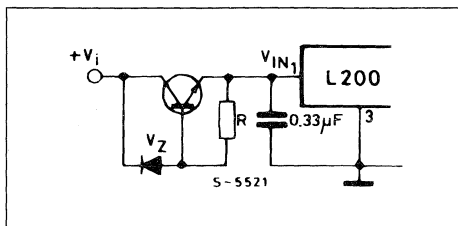


POSITIVE AND NEGATIVE VOLTAGE REGULATORS

The circuit in fig. 19 provides positive and negative balanced, stabilized voltages simultaneously. The L200 regulator supplies the positive voltage while the negative is obtained using an operational amplifier connected as follower with output current booster.

Tracking of the positive voltage is achieved by putting the non-inverting input to ground and using the inverting input to measure the feedback voltage coming from divider R1-R2.

Figure 17.



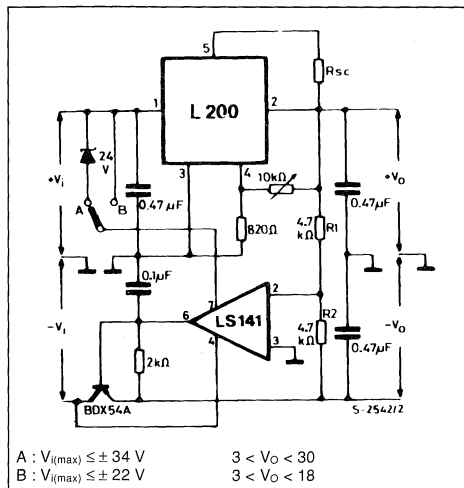
The designer must take into account the dissipated power and the SOA of the preregulation transistor. For example, using the BDX53, the maximum input voltage can reach 56 V (fig. 16). In these conditions we have 20 V of V_{CEon} the transistor and with a load current of 2 A the operation point remains inside the SOA. The preregulation used in fig. 16 reduces the ripple at the input of the device, making it possible to obtain an output voltage with negligible ripple.

If high output voltages are also required, a second zener, V_z , is used to refer the ground pin of an IC to a potential other than zero ; diode D1 provides output shortcircuit protection (fig. 18).

The system is balanced when the inputs of the operational amplifier are at the same voltage, or, since one input is at fixed ground potential, when the voltage of the intermediate point of the divider goes to 0 Volts. This is only possible if the negative voltage, on command of the op-amp, goes to a value which will make a current equal to that in R1 flows in R2. The ratio which expresses the negative output voltage is :

$$V^- = V^+ \cdot \frac{R_2}{R_1} \quad (\text{If } R_2 = R_1, \text{ we'll get } V^- = V^+)$$

Figure 19.



Since the maximum supply voltage of the op amp used is ± 22 V, when pin 7 is connected to point B output voltages up to about 18 V can be obtained. If on the other hand pin 7 is connected to point A, much higher output voltages, up to about 30 V, be obtained since in this case the input voltage can rise to 34 V.

Fig. 20 shows a diagram in which the L165 power op amp is used to produce the negative voltage. In this case (as in fig. 19) the output voltage is limited by the absolute maximum rating of the supply voltage of the L165 which is ± 18 V. Therefore to get a higher V_{out} we must use a zener to keep the device supply within the safety limits.

If we have a transformer with two separate secondaries, the diagram of fig. 21 can be used to obtain independent positive and negative voltages. The two output diodes, D1 and D2, protect the devices from shortcircuits between the positive and negative outputs.

Figure 20.

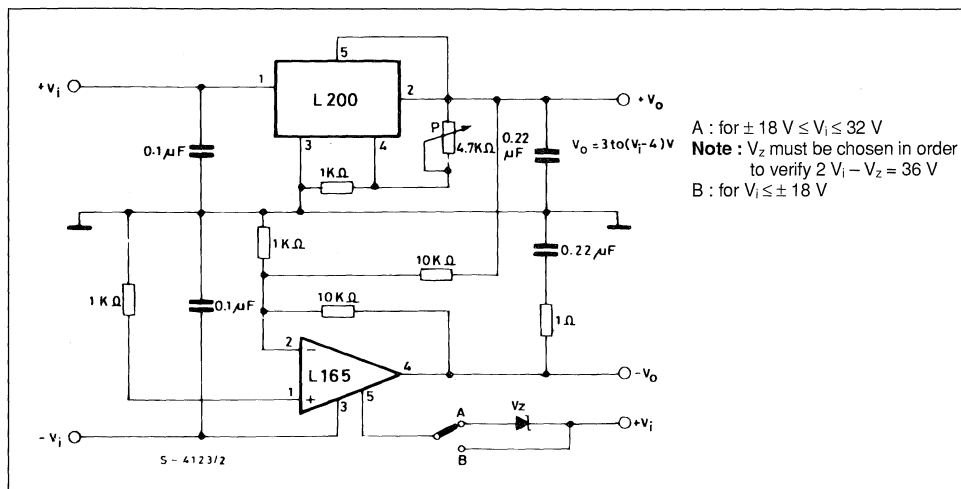
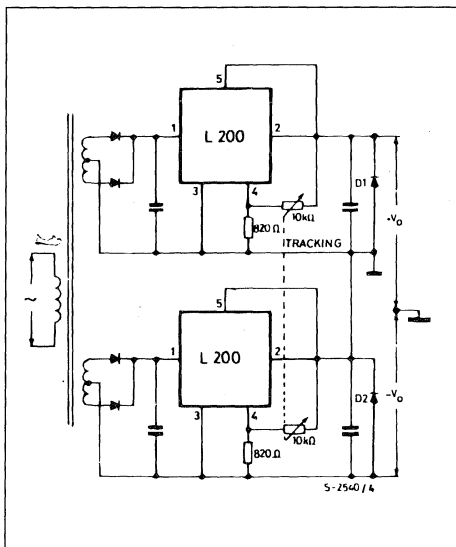


Figure 21.



COMPENSATION OF VOLTAGE DROP ALONG THE WIRES

The diagram in fig. 22 is particularly suitable when a load situated far from the output of the regulator has to be supplied and when we want to avoid the use of two sensing wires. In fact, it is possible to compensate the voltage drop on the line caused by the load current (see the two curves in fig. 23 and 24). R_K transforms the load current I_L into a proportional voltage in series to the reference of the L200. $R_K I_L$ is then amplified by the factor

$$\frac{R_2 + R_1}{R_1}$$

With the values of R_Z , R_2 and R_1 known, we get :

$$R_K = R_Z \frac{R_1}{R_1 + R_2}$$

R_Z , R_1 and R_2 are assumed to be constant.

If R_K is higher than 10Ω , the output voltage should be calculated as follows :

$$V_O = I_d R_K + V_{ref} \frac{R_2 + R_1}{R_1}$$

Figure 22.

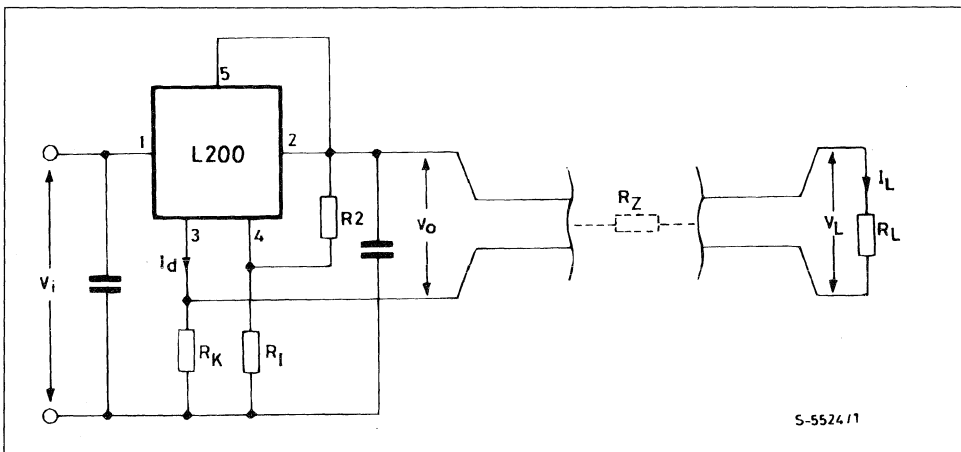


Figure 23.

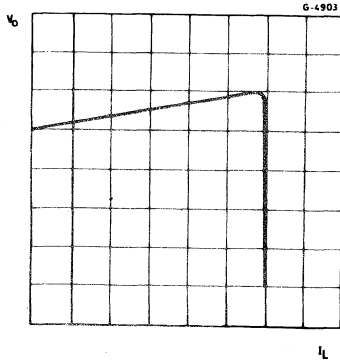
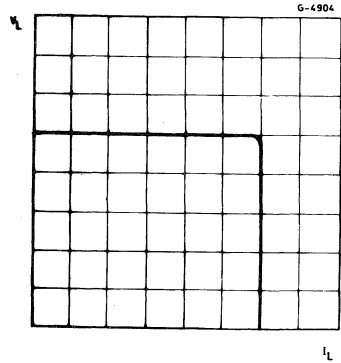


Figure 24.



MOTOR SPEED CONTROL

Fig. 25 shows how to use the device for the speed control of permanent magnet motors. The desired speed, proportional to the voltage at the terminal of the motor, is obtained by means of R1 and R2.

$$V_M = V_{ref} \left(1 + \frac{R_2}{R_1} \right)$$

To obtain better compensation of the internal motor resistance, which is essential for good regulation, the following equation is used :

$$R_3 \leq \frac{R_1}{R_2} \cdot R_M$$

This equation works with infinite R4. If R4 is finite, the motor speed can be increased without altering the ratio R2/R1 and R3. Since R4 has a constant voltage (V_{ref}) at its terminals, which does not vary as R4 varies, this voltage acts on R2 as a constant current source variable with R4. The voltage drop on R2 thus increases, and the increase is felt by the voltage at the terminals of the motor. The voltage increase at the motor terminals is :

$$V_M = \frac{V_{ref}}{R_4 + R_3} \cdot R_2$$

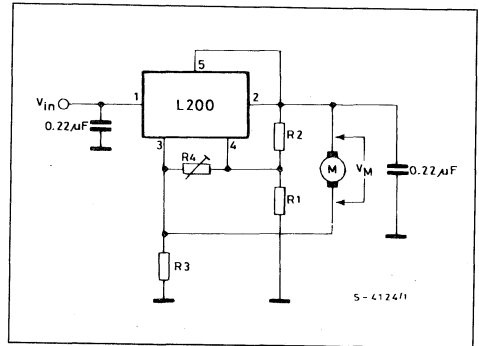
A circuit for a 30 W motor with R_M = 4 Ω, R1 = 1 kΩ, R2 = 4.3 kΩ, R4 = 22 kΩ and R3 = 0.82 Ω has been realized.

POWER AMPLITUDE MODULATOR

In the configuration of fig. 26 the L200 is used to send a signal onto a supply line. Since the input signal V_i is DC decoupled, the V_o is defined by :

$$V_O = V_{ref} \left(1 + \frac{R_2}{R_1} \right)$$

Figure 25.



The amplified signal V_i whose value is :

$$G_V = - \frac{R_2}{R_3}$$

is added to this component. By ignoring the current entering pin 4, we must impose i₁ = i₂ + i₃ (1) and since the voltage between pin 4 and ground remains fixed (V_{ref}) as long as the device is not in saturation, i₁ = 0 and equation (1) becomes :

$$i_2 = -i_3 \text{ with } i_3 = \frac{V_i}{R_3} \quad (\text{for } X_c \ll R_3) \quad \text{Therefore}$$

$$V_O = R_2 \quad i_2 = - \frac{V_i}{R_3} \cdot R_2$$

An application is shown in fig. 27. If the DC level is to be varied but not the AC gain, R1 should be replaced by a potentiometer.

Figure 26.

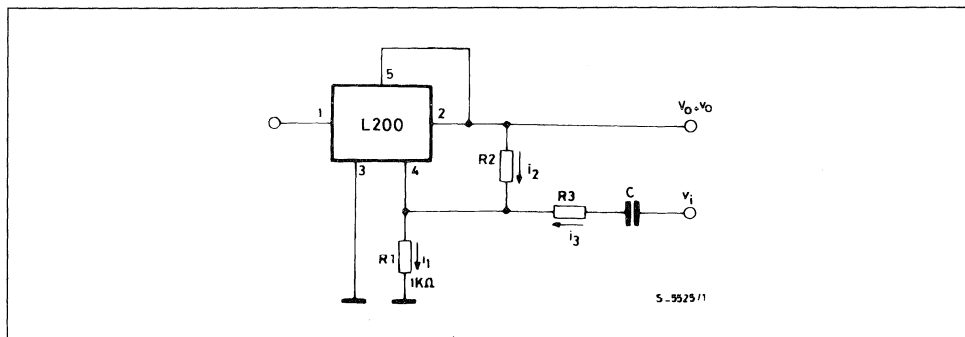
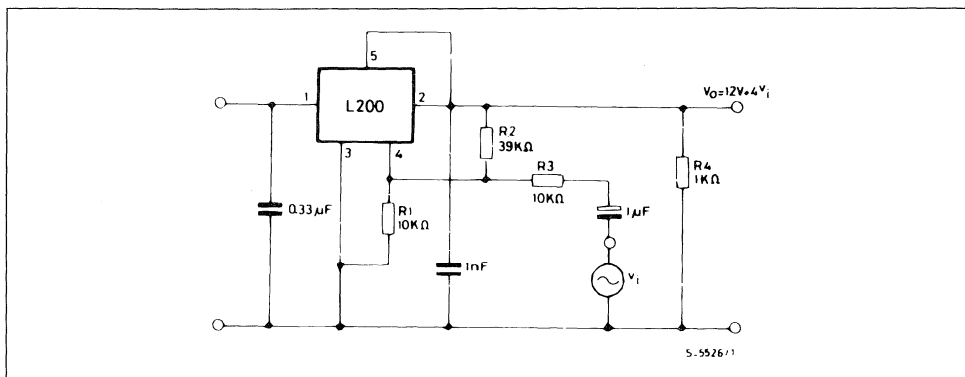


Figure 27.



HIGH CURRENT REGULATORS

To get a higher current than can be supplied by a single device one or more external power transistors must be introduced. The problem is then to extend all the device's protection circuits (short-circuit protection, limitation of T_j of external power devices and overload protection) to the external transistors. Constant current or foldback current limitation therefore becomes necessary.

When the regulator is expected to withstand a permanent shortcircuit, constant current limitation becomes more and more difficult to guarantee as the nominal V_o increases. This is because of the increase in V_{CE} at the terminals of the transistor, which leads to an increase in the dissipated power. The heatsink has to be calculated in the heaviest working conditions, and therefore in shortcircuit. This increases weight, volume and cost of the heatsink and increase of the ambient temperature (because of high power dissipation). Besides heatsink, power

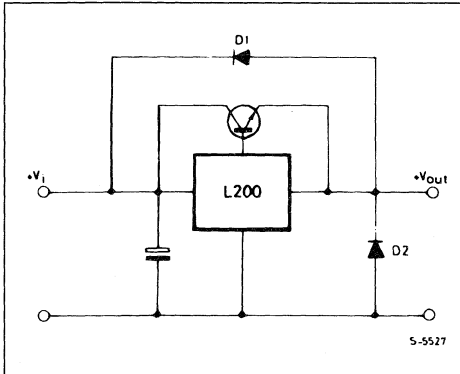
transistors must be dimensioned for the short-circuit.

This type, of limitation is suited, for example, with highly capacitive loads. Efficiency is increased if pre-regulation is used on the input voltage to maintain a constant drop-out on the power element for all V_{out} , even in shortcircuit. Foldback limitation, on the other hand, allows lighter shortcircuit operating conditions than the previous case. The type of load is important.

If the load is highly capacitive, it is not possible to have a high ratio between I_{max} and I_{sc} because at switch-on, with load inserted, the output may not reach its nominal value.

Other protection against input shortcircuit, mains failure, overvoltages and output reverse bias can be realized using two diodes, D1 and D2, inserted as indicated in fig. 28.

Figure 28.



USE OF A PNP TRANSISTOR

Fig. 29 shows the diagram of a high current supply using the current limitation of the L200. The output current is calculated using the following formula :

$$I_o = \frac{V_{SC}}{R_{SC}} \cong \frac{0.45 \text{ V}}{0.1 \Omega} = 4.5 \text{ A}$$

Constant current limitation is used ; so, in output shortcircuit conditions, the transistor dissipates a power equal to :

$$P_D = V_i \cdot I_o = V_i \cdot \frac{V_{SC}}{R_{SC}}$$

The operating point of the transistor should be kept well within the SOA ; with $R_{SC} = 0.1 \Omega$, V_i must not exceed 20 V. Part of the I_o crosses the transistor and part crosses the regulator.

Figure 30.

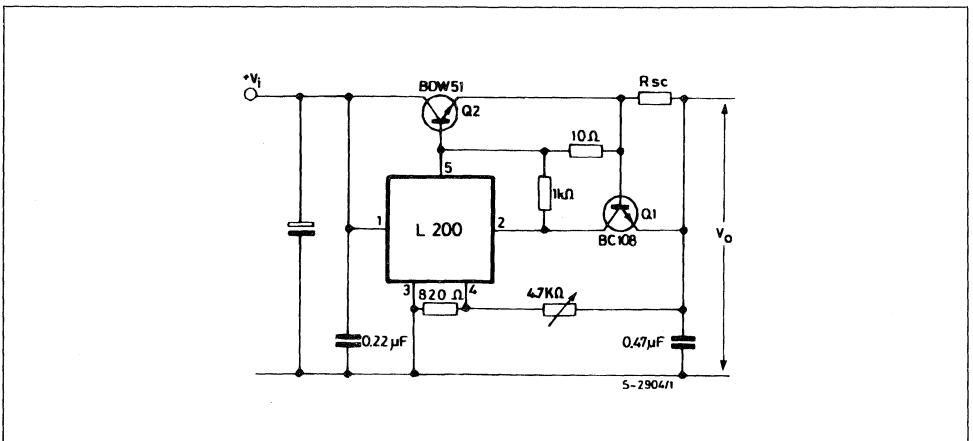
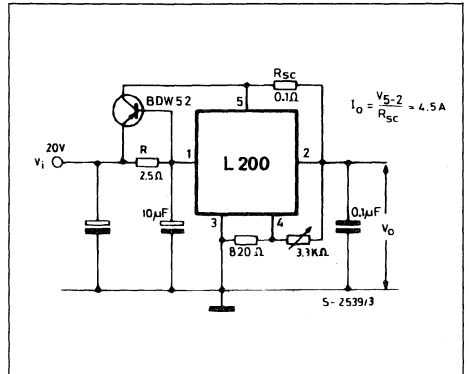


Figure 29.



The latter is given by : $I_{REG} = I_B + \frac{V_{BE}}{R}$

where I_B is the base current of the transistor (-100 mA at $I_C = 4 \text{ A}$) and V_{BE} is the base-emitter voltage (-1 V at $I_C = 4 \text{ A}$) ; with $R = 2.5 \Omega$, $I_{REG} \cong 500 \text{ mA}$.

USE OF AN NPN POWER TRANSISTOR

Fig. 30 shows the same application as described in figure 29, using an NPN power transistor instead of a PNP. In this case an external signal transistor must be used to limit the current. Therefore :

$$I_o = \frac{V_{BE} Q1}{R_{SC}}$$

As regards the output shortcircuit, see par. 1.5.

12 V 4 A POWER SUPPLY

The diagram in fig. 31 shows a supply using the L200 and the BD705. The 1 k Ω potentiometer, PT1, together with the 3.3 k Ω resistor are used for fine regulation of the output voltage.

Current limitation is of the type shown in fig. 32. Trimmer PT2 acts on stretch AB of characteristic. With the values indicated (PT2 = 1 k Ω , PT3 = 470 Ω , R = 3 k Ω), currents from 3 to 4 A can be limited. The field of variation can be increased by increasing the value of R_{sc} or by connecting one terminal of PT to the base of the power transistor, which, however, provides less stable limitation. If section AB is moved, section BC will also be moved.

The slope of BC can be varied using PT3. The voltage level at point B is fixed by the voltage of the zener diode. The capacitor in parallel to the zener ensures correct switch-on with full load. The BD705 should always be used well within its safe operating area. If this is not possible two or more BD705s should be used, connected in parallel (fig. 33).

Further protection for the external power transistor can be provided as shown in fig. 34. The PTC resistor, whose temperature intervention point must prevent the T_j of the power transistor from reaching its maximum value, should be fixed to the dissipator near the power transistor. Dimensioning of R_A and R_B depends on the PTC used.

Figure 31.

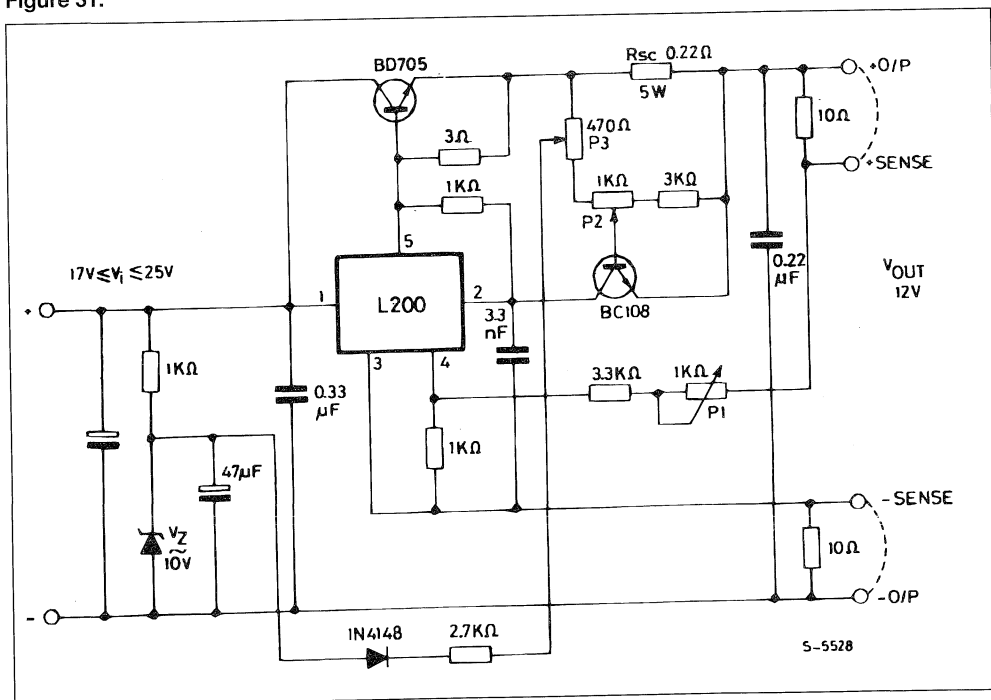


Figure 32.

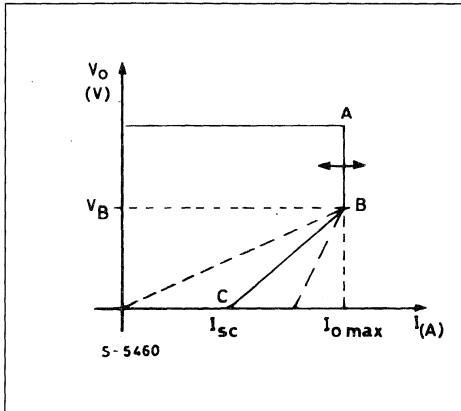


Figure 33.

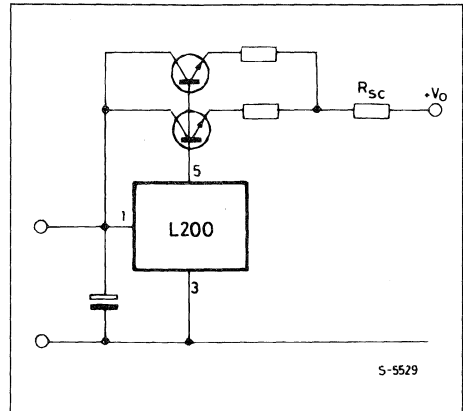
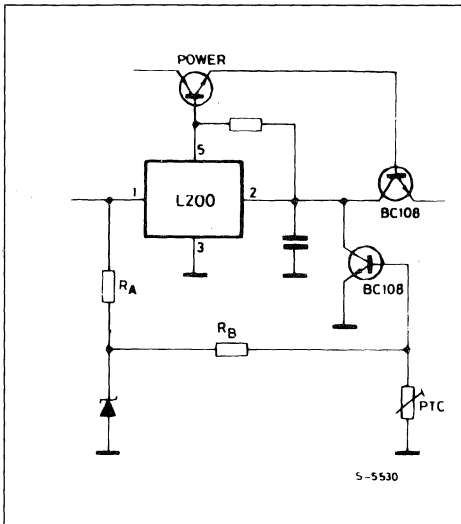


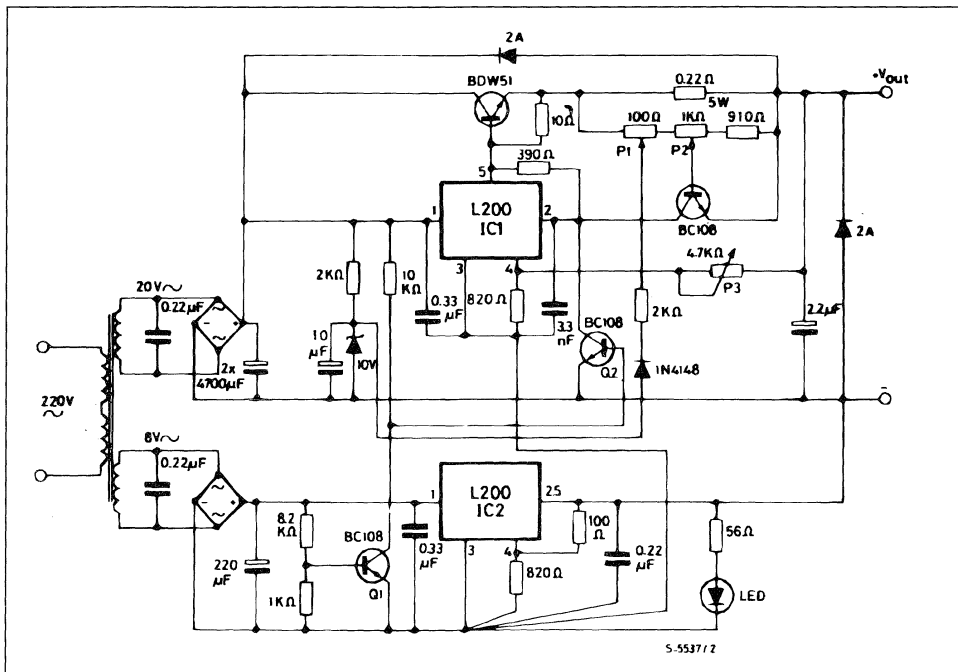
Figure 34.



VOLTAGE REGULATOR FROM 0 V TO 16 V - 4.5 A

Fig. 35 shows an application for a high current supply with output voltage adjustable from 0 V to 16 V, realized with two L200 regulators and an external power transistor. With the values indicated, the current can be regulated from 2 A to 4.5 A by potentiometer PT2. PT1, on the other hand, is used for constant current or foldback current limitation. The integrated circuit IC2, which does not require a heat-sink and has excellent temperature stability, is used to obtain the 0 V output. It is connected so as to lower pin 3 of IC1 until pin 4 reaches 0 V. Q1 and Q2 ensure correct operation of the supply at switch-on and switch-off.

Figure 35.



POWER SUPPLY WITH $V_o = 2.8$ TO 18 V, $I_o = 0$ TO 2.5 A

The diagram in fig. 36 shows a supply with output voltage variable from 2.8 V to 18 V and constant current limitation from 0 A to 2.5 A. The output current can be regulated over a wide range by means of the op. amp. and signal transistor TR₂. The op. amp. and the transistor are connected in the voltage-current converter configuration. The voltage is taken at the terminals of R₃ and converted into current by PT₂.

I_0 is fixed as follows :

$$\frac{R_4 I_0}{PT_2} = I_1 (*) \quad (**) I_{sc} = \frac{V_{sc}}{R_2}$$

When $I_1 = I_{SC}$, the regulator starts to operate as a

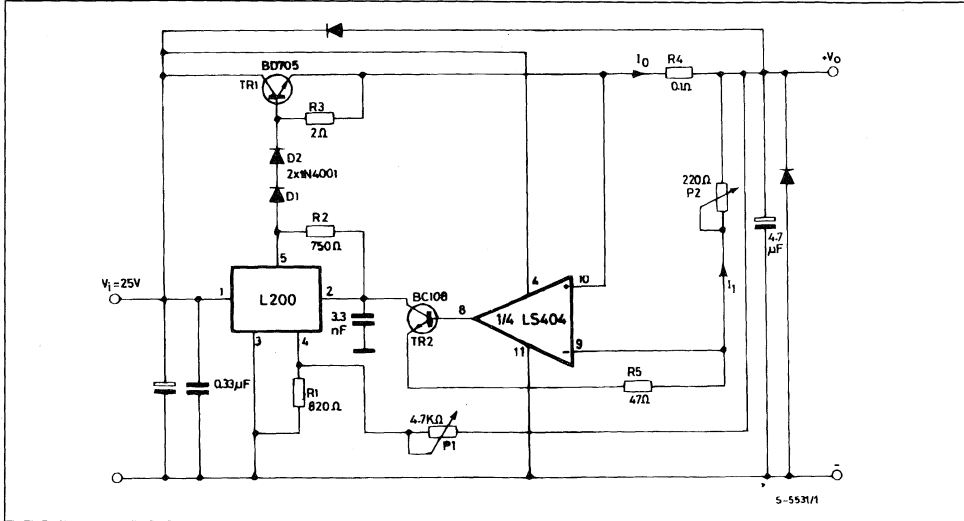
current generator. By making (*) equal to (**) we get :

$$\frac{R_4 I_o}{P T_2} = \frac{V_{SC}}{R_2} \quad \text{Therefore } I_o = \frac{V_{SC}}{R_2 \cdot R_4} \cdot P T_2$$

Diodes D1 and D2 keep transistor TR_2 in linear condition in the case of small output currents. If it is not necessary to limit the current to zero, one of the diodes can be eliminated : the second diode could also be eliminated if TR_1 were a darlington instead of a transistor.

The op. amp. must have inputs compatible with ground in order to guarantee current limitation even in shortcircuit. With a negative voltage available, even of only a few volts, current limitation is simplified.

Figure 36.



LAYOUT CONSIDERATIONS

The performance of a regulator depends to a great extent on the case with which the printed circuit is produced. There must be no impulsive currents (like the one in the electrolytic filter capacitor at the input of the regulator) between the ground pin of the device (pin 3) and the negative output terminal because these would increase the output ripple. Care must also be taken when inserting the resistor connected between pin 4 and pin 3 of the device.

The track connecting pin 3 to a terminal of this resistor should be very short and must not be crossed

by the load current (which, since it is generally variable, would give rise to a voltage drop on this stretch of track, altering the value of V_{ref} and therefore of V_o).

When the load is not in the immediate proximity of the regulator output "+ sense" and "- sense" terminals should be used (see fig. 37). By connecting the "+ sense" and "- sense" terminals directly at the charge terminals the voltage drop on the connection cable between supply and load are compensated. Fig. 37 shows how to connect supply and load using the sensing clamps terminals.

Figure 37.

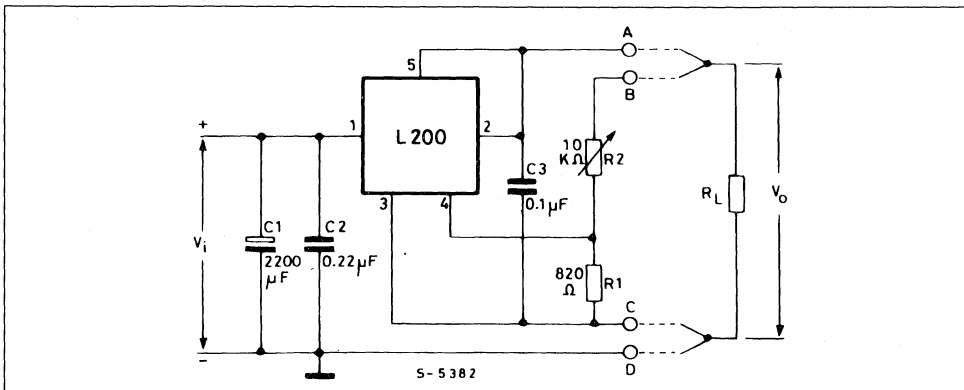
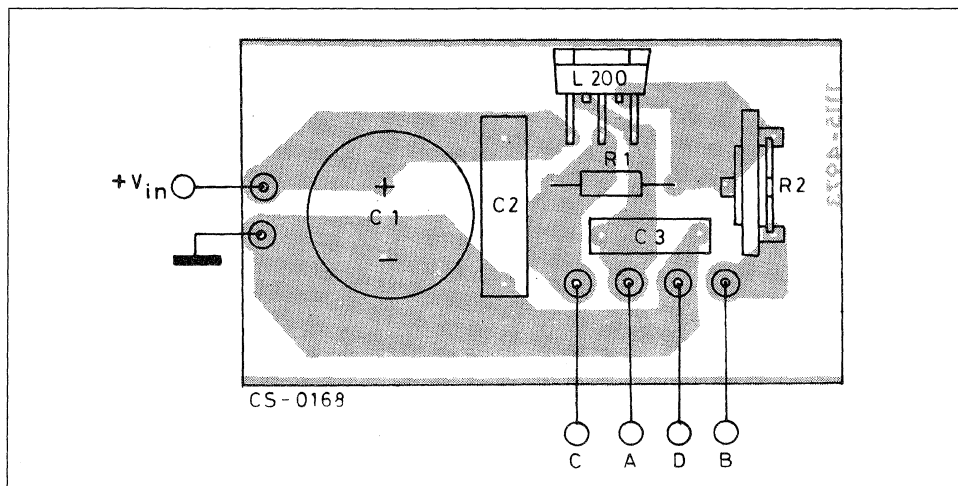


Figure 38.



HEATSINK DIMENSIONING

The heatsink dissipates the heat produced by the device to prevent the internal temperature from reaching value which could be dangerous for device operation and reliability.

Integrated circuits in plastic package must never exceed 150 °C even in the worst conditions. This limit has been set because the encapsulating resin has problems of vitrification if subjected to temperatures of more than 150 °C for long periods or of more than 170 °C for short periods (24 h). In any case the temperature accelerates the ageing process and therefore influences the device life ; an increase of 10 °C can halve the device life. A well designed heatsink should keep the junction temperature between 90 °C and 110 °C. Fig. 39 shows the structure of a power device. As demonstrated in thermodynamics, a thermal circuit can be considered to be an electrical circuit where R1, 2 represent the thermal resistance of the single elements (expressed in C/W) ;

Figure 39.

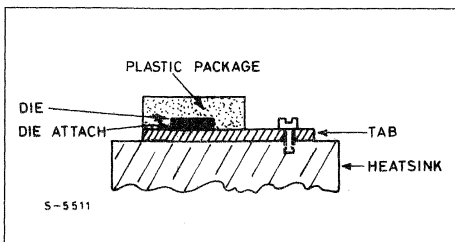
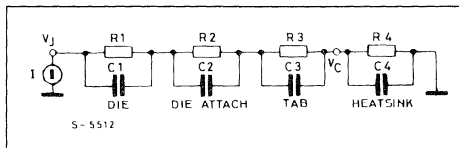


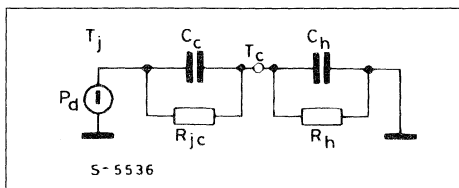
Figure 40.



- C1, 2 the thermal capacitance (expressed in °C/W)
- I the dissipated power
- V the temperature difference with respect to the reference (ground)

This circuit can be simplified as follows :

Figure 41.

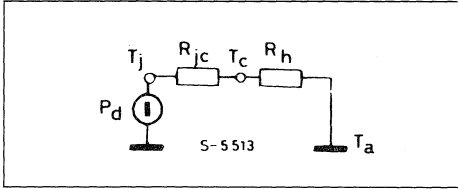


Where C_e is the thermal capacitance of the die plus that of the tab.

- C_h is the thermal capacitance of the heatsink
- R_{jc} is the junction case thermal resistance
- R_h is the heatsink thermal resistance

But since the aim of this section is not that of studying the transistors, the circuit can be further reduced.

Figure 42.



If we now consider the ground potential as ambient temperature, we have :

$$T_j = T_a + (R_{jc} + R_h) P_d \quad (1)$$

$$R_{th} = \frac{T_j - T_a - R_{jc} \cdot P_d}{P_d} \quad (1a)$$

$$T_c = T_a + R_h \cdot P_d \quad (2)$$

For example, consider an application of the L200 with the following characteristics :

$V_{in\ typ} = 20\ V$
 $V_o = 14\ V$
 $I_o\ typ = 1\ A$
 $T_a = 40\ ^\circ C$

typical conditions

$V_{in\ max} = 22\ V$
 $V_o = 14\ V$
 $I_o\ max = 1.2\ A$
 $T_a = 60\ ^\circ C$

overload conditions

$$P_{d\ typ} = (V_{in} - V_o) \cdot I_o = (2014) \cdot 1 = 6\ W$$

$$P_{d\ max} = (2214) \cdot 1.2 = 9.6\ W$$

Imposing $T_j = 90\ ^\circ C$ of (1a) we get (from L200 characteristics we get $R_{jc} = 3\ ^\circ C/W$).

$$R_h = \frac{90 - 40 - 3 \cdot 6}{6} = 5.3\ ^\circ C/W$$

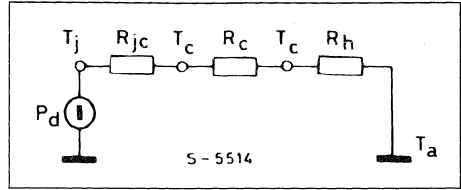
Using the value thus obtained in (1), we get that the junction temperature during the overload goes to the following value :

$$T_j = 60 + (3 + 5.3) \cdot 9.6 = 140\ ^\circ C$$

If the overload occurs only rarely and for short periods, dimensioning can be considered to be correct. Obviously during the shortcircuit, the dissipated power reaches much higher values (about 40 W for the case considered) but in this case the thermal protection intervenes to maintain the temperature below the maximum values allowed.

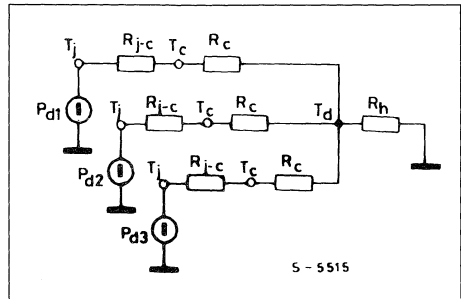
Note 1 : If insulating materials are used between device and heatsink, the thermal contact resistance must be taken into account (0.5 to 1 $^\circ C/W$, depending on the type of insulant used) and the circuit in fig. 43 becomes :

Figure 43.



Note 2 : In applications where one or more external transistors are used together with the L200, the dissipated power must be calculated for each component. The various junction temperatures can be calculated by solving the following circuit :

Figure 44.



This applies if the various dissipating elements are fairly near to one another with respect to the heat-sink dimensions, otherwise the heatsink can no longer be considered as a concentrated constant and the calculation becomes difficult.

This concept is better explained by the graph in fig. 45 which shows the case (and therefore junction) temperature variation as a function of the distance between two dissipating elements with the same type of dissipator and the same dissipated power. The graph in fig. 45 refers to the specific case of two elements dissipating the same power, fixed on a rectangular aluminium plate with a ratio of 3 between the two sides. The temperature jump will depend on the dissipated power and on the device geometry but we want to show that there exists an optimal position between the two devices :

$$d = \frac{1}{2} \cdot \text{side of the plate}$$

Fig. 46 shows the trend of the temperature as a function of the distance between two dissipating elements whose dissipated power is fairly different (ratio 1 to 4).

APPLICATION NOTE

This graph may be useful in applications with the L200 + external transistor (in which the transistor generally dissipates more than the L200) where the temperature of the L200 has to be kept as low as possible and especially where the thermal protection of the L200 is to be used to limit the transistor temperature in the

case of an overload or abnormal increase in the ambient temperature. In other words the distance between the two elements can be selected so that the power transistor reaches the $T_{j\max}$ (200 °C for a TO-3 transistor) when the L200 reaches the thermal protection intervention temperature.

Figure 45.

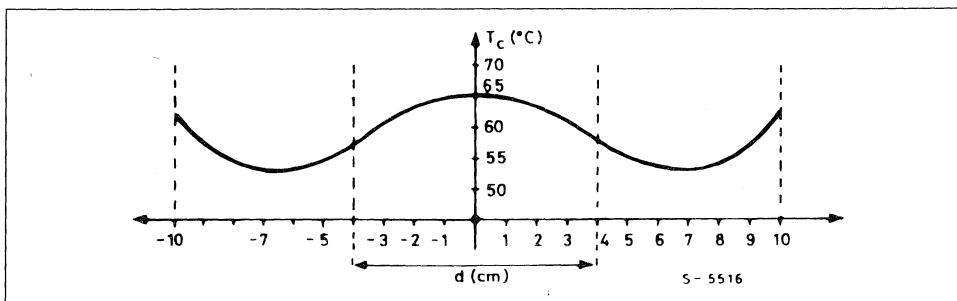
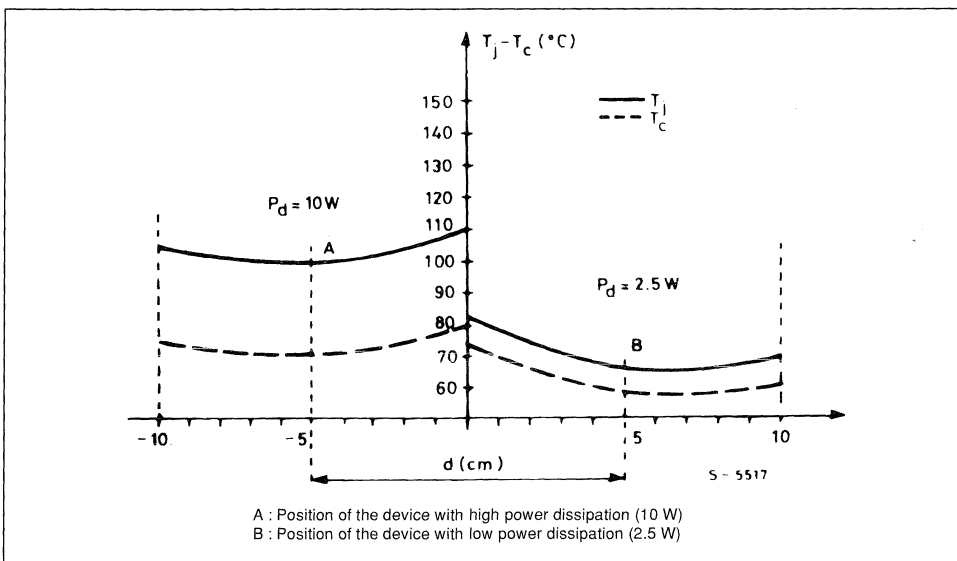


Figure 46.



DUAL REGULATORS SIMPLIFY MICRO SYSTEM SUPPLY DESIGN

Combining two 5 V regulators and a reset circuit on a single chip, special purpose regulator chips simplify the design of power supplies for microprocessor systems incorporating battery backup RAMs or shadow-type NV RAMs.

Power supplies for microprocessor systems are often complicated by the need to take care of the special requirements of non-volatile read/write memory. Where battery backup CMOS RAMs are used, for example, it is important to ensure that the RAMs are disabled when the primary supply is removed. And when shadow-type NV memory is included the backup transfer must be initiated and completed when the supply is interrupted. Designed specifically for such applications, the SGS-THOMSON Microelectronics L4901, and L4902 dual voltage regulators combine two 5 V regulators plus a reset circuit on a single chip, simplifying the designer's task.

Assembled in the SGS-THOMSON Heptawatt [TM] 7-lead package, the L4901 and L4902 contain separate voltage regulators rated at 5 V/300 mA (the "V1" output) and 5 V/400 mA (the "V2" output).

Both the V1 and V2 regulators have an output voltage precision of $\pm 2\%$ and include protection against output short circuits and 60 V input transients.

Also included on the chip is a reset circuit with externally programmable timing which depends on the input voltage and the output of the V1 regulator.

Functionally, the two devices are identical except that the L4901 has separate inputs to the two regulators and the L4902 has a common input plus a disable input which controls the V2 output (fig. 1).

Generally the V1 regulator is used to supply circuits which must be powered continuously - volatile memory, a time-of-day clock and so on - while the V2 output supplies other 5 V circuits which may be powered down when the equipment is inactive.

The V1 output features a very low leakage current at the output - less than $1\mu\text{A}$ - to allow the use a backup battery. The V1 regulator also features a low quiescent current at the input (0.6 mA typical) to minimize battery drain in applications where the V1 regulator is permanently connected to a battery supply.

Figure 1a : TWO 5V OUTPUTS - The L4901 Dual Regulator Provides 300 mA and 400 mA 5 V Outputs and Includes a Microprocessor Reset Function. This Device is Ideal for Microprocessor Systems with Battery Backup or Shadow RAM.

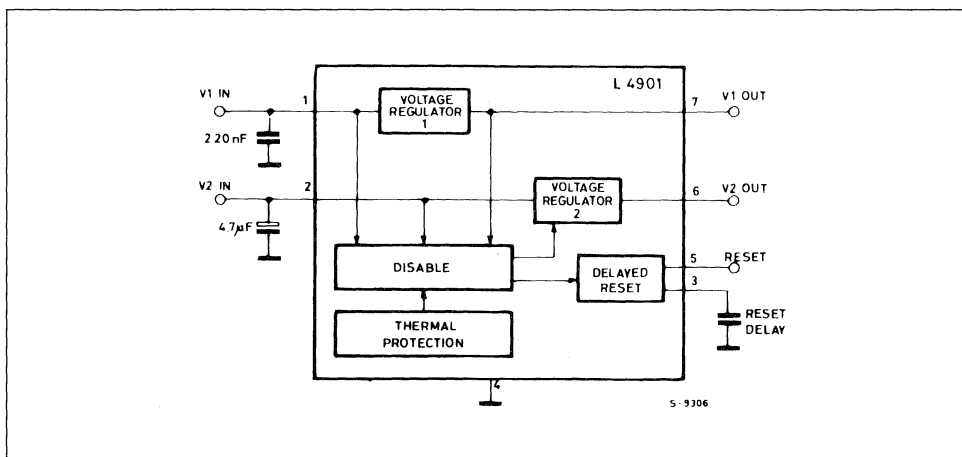


Figure 1b : DISABLE INPUT - The L4902 is Similar to the L4901 but also Features a Disable Input for the V2 Regulator.

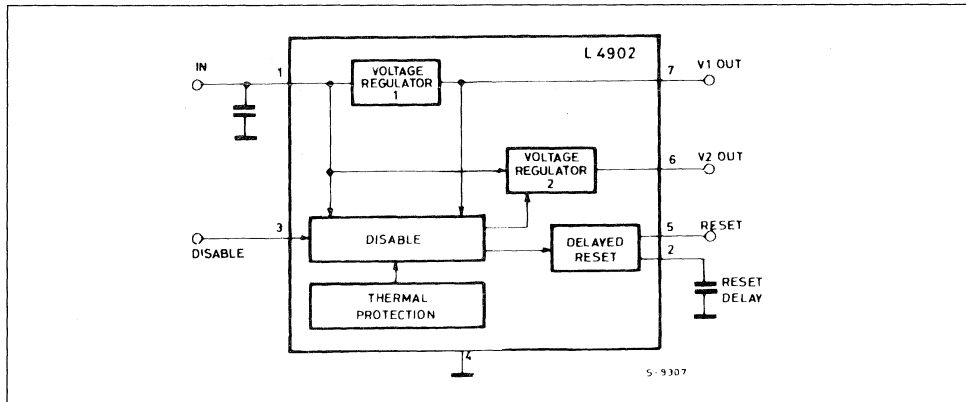
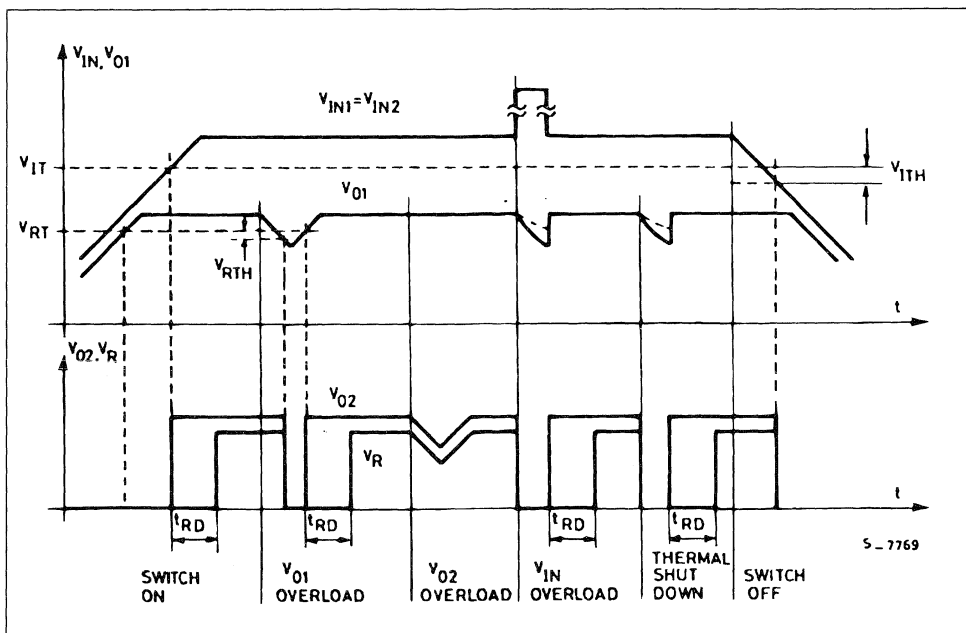


Figure 2 : WAVEFORMS - An Important Feature of the L4901 Series Regulators is that the Reset Circuit Monitors the Input Voltage.



VERSATILE DEVICES

The L4901 and L4902 are versatile devices which simplify the supply circuitry of many systems and can be used in a number of different ways.

One possibility, outlined in figure 3, is to connect the V1 regulator permanently to a battery to supply a CMOS time-of-day clock and a CMOS microcomputer chip with volatile memory. In this example the V2 output supplies non-essential 5 V circuits. A typical use of this scheme is in trip computers or car radios with programmable tuning.

An alternative, shown in figure 4, is to use the L4901 with a backup battery on the V1 output to maintain a CMOS clock and a standby-type NMOS microcomputer chip. In this case the main on/off switch disconnects both the V1 and V2 regulators from the battery.

Figure 5 illustrates how the L4902's disable input may be used in a CMOS microcomputer application. In this example the V2 output, supplying non-essential circuits, is turned off under control of the micro-

processor circuit. Configurations of this type are used in products where the "OFF" switch is part of a keypad scanned by a micro which operates continuously, even in the "OFF" state.

The L4901 is also ideal for microcomputer systems using battery backup CMOS static RAMs. As shown in figure 6 the V1 output supplies the CMOS RAMs and the V2 output supplies the microprocessor plus other 5 V circuits. The L4901's reset output is used both to reset the Z80 and, through the M74HC138 address decoder, to ensure that the RAMs are disabled as soon as the main supply voltage starts to fall. Note that the M74HC138 is supplied from the backup battery.

It is important to make sure that the RAMs are disabled because the lithium cells used as backup batteries have a high internal resistance. If the RAMs were not forced into the low consumption standby state the battery voltage could drop so low that memory contents are corrupted. Moreover, to prevent latch up, no input of a CMOS RAM should ever be higher than the supply voltage.

Figure 3 : LOW QUIESCENT CURRENT at the V1 Input makes the L4901 Useful in Applications like this where the V1 Regulator is always connected to the Battery.

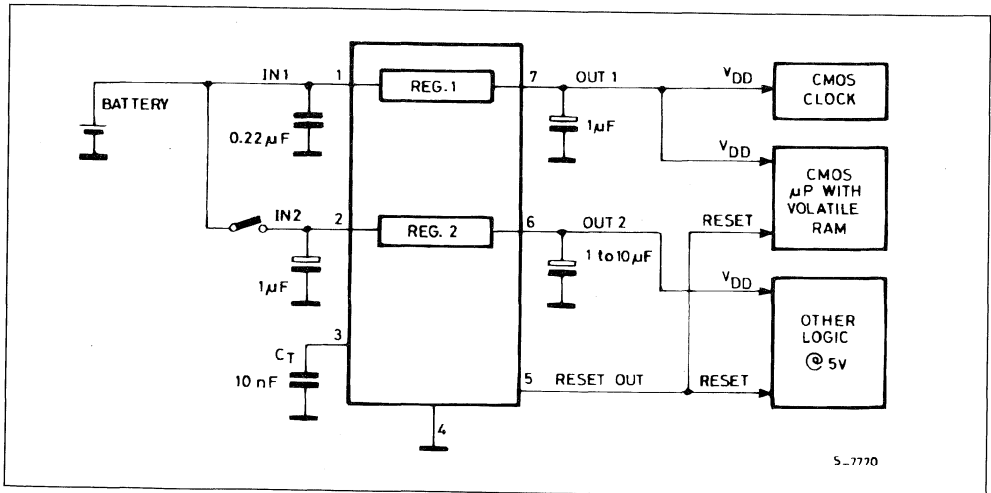
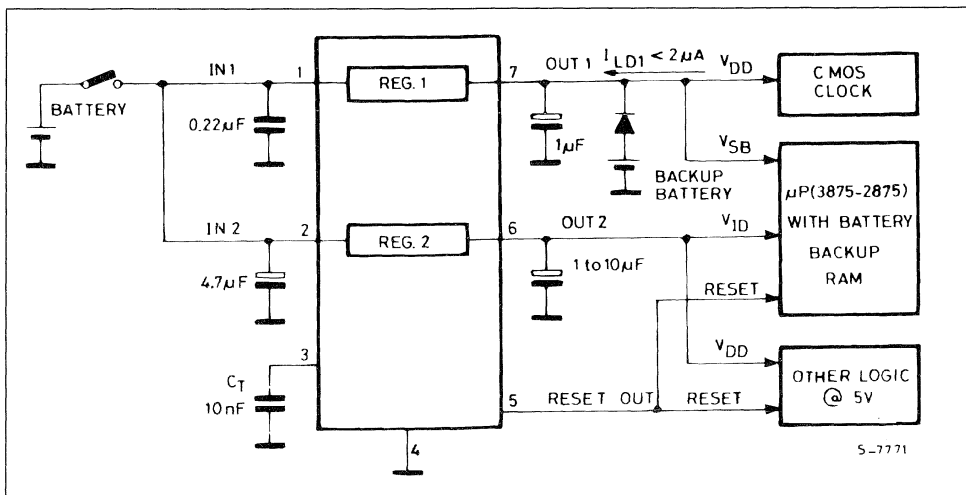
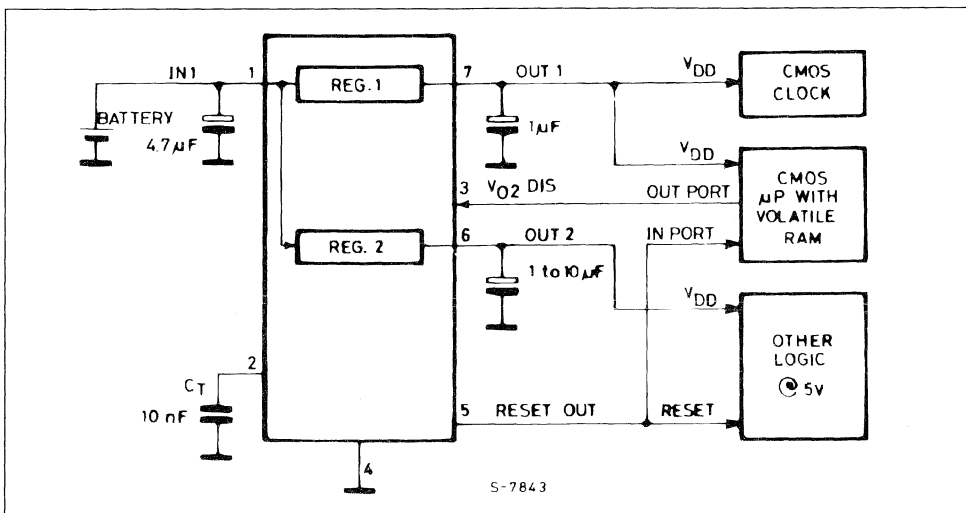


Figure 4 : LOW LEAKAGE at the V1 Output makes the L4901 Ideal for Battery Backup Operation.**Figure 5 :** STANDBY - The L4902 can be used in Applications where the Supply is connected Permanently and the Disable Function Used to Turn Off on-essential Circuits in the Standby State.

IDEAL FOR SHADOW MEMORIES

Another interesting application for the L4902 is supplying a shadow-ram microcomputer chip like the SGS-THOMSON M38SH72 where a fast non-volatile memory is backed up on-chip by a slow EEPROM (figure 7). For these chips it is important to

ensure that the backup command is generated when the supply is removed, a function which the L4902's reset output can perform. Since the L4902's reset function depends on the INPUT voltage the power fail condition is sensed early enough to guarantee that the backup transfer will be successful.

In figure 7 the reset output is forced low when the input voltage falls below 6.3 V or when the V1 output goes below 4.8 V. This allows 10 μ s for the backup transfer (with 10 μ F capacitors) which is more than sufficient.

Similarly, the L4902 can be used with shadow-type RAMs such as the Xicor X2201. In the figure 8 circuit a capacitor on the V1 input ensures that the X2201 is powered during the transfer operation. When the input voltage is removed or goes below 6.3 V the L4902's reset output, connected to the 8085's TRAP input, forces the execution for a service routine which saves the state of the machine in the RAM then issues a backup command. The V2 output drops immediately while the 680 μ F capacitor on the V1 input provides enough energy to keep the X2201 running for the 10 ms needed to com-

plete the backup transfer. The low consumption of the V1 regulator allows the use of a relatively small capacitor for this function.

ADDING A WATCHDOG

By adding a few components and two Schmitt trigger gates a watchdog function can be added to the L4902 (figure 9). Normally an output port of the micro will supply a software-generated pulse at least every 10 ms. If something has gone wrong in the software or hardware and these pulses are missing the disable input will be activated after a period set by R1.C1, disabling all the circuitry connected to the V2 output of the L4902. The disable period could be useful to prevent spurious operation of motors and solenoids while the control processor is malfunctioning.

Figure 6 : CMOS RAMs - The L4901 is Useful in Systems with Battery Backup CMOS RAMs Because the Reset Output can be used to Ensure that the RAM Chips are disabled to Reduce Battery Drain when the Main Supply is removed.

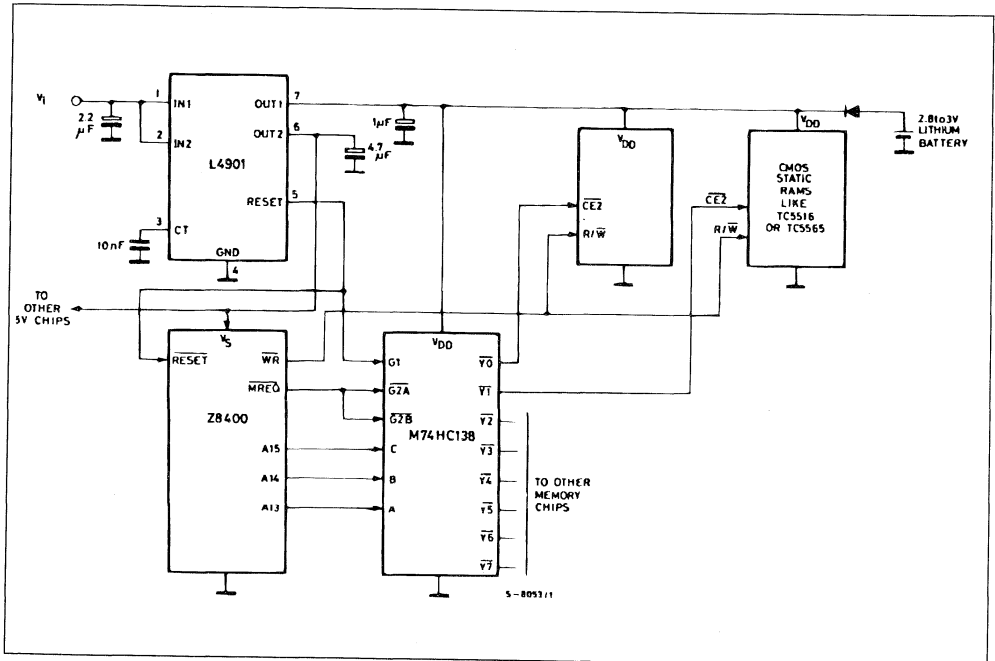
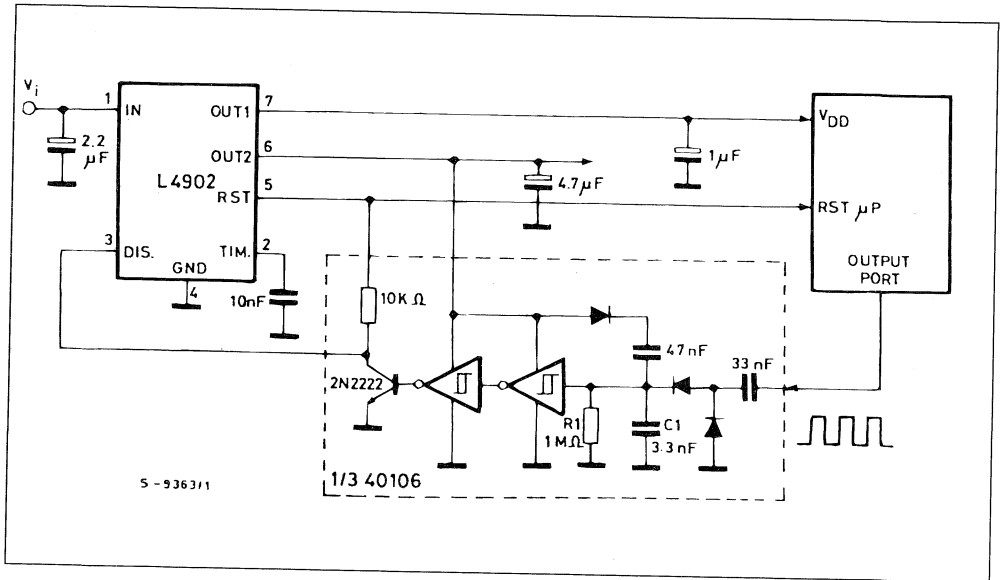


Figure 9 : With a CMOS Schmitt Trigger and a few Components a Watchdog Function can be added for Critical Application.



A NEW VOLTAGE REGULATOR SERIES - THE L7800H

by S. Sueri
J. Eadie

Three terminal linear regulators have been available for a considerable time and offer designers ease of use, built-in overcurrent, and thermal protection together with low cost. They do not suffer from the noise problems associated with switching power supplies and therefore are straight forward to use in precision instruments and analogue circuits where stable power supplies are required. Additionally they need no in - circuit adjustment. They are however limited in that they only cover certain fixed voltage and current ratings. The voltage cannot easily be trimmed to a precise value in between these fixed outputs.

With the increasing demand for better and more cost effective voltage regulators a new series of $\pm 1\%$ regulators with greatly improved output voltage versus current characteristic, the L7800H series, has been developed by SGS - THOMSON.

The most important features of this new device, with respect to the previous ones, are :

- an output voltage regulated to within $\pm 1\%$ of the nominal value,
- a load regulation that is about 10 times better than the first L78 series of linear regulators.

Because of the improved current regulation the L7805H is ideal for regulating the supply to TTL logic circuits where it minimises the likelihood of voltage excursions below 4.8V or over 5.2V caused by current surges. Figure 1 compares the voltage regulation with a 1A transient of the L7805CV (standard) with the L7805HBV (1%). Figure 2 shows the test circuit used to obtain figure 1. Other parameters are the same or slightly better than the standard L7800 regulator series.

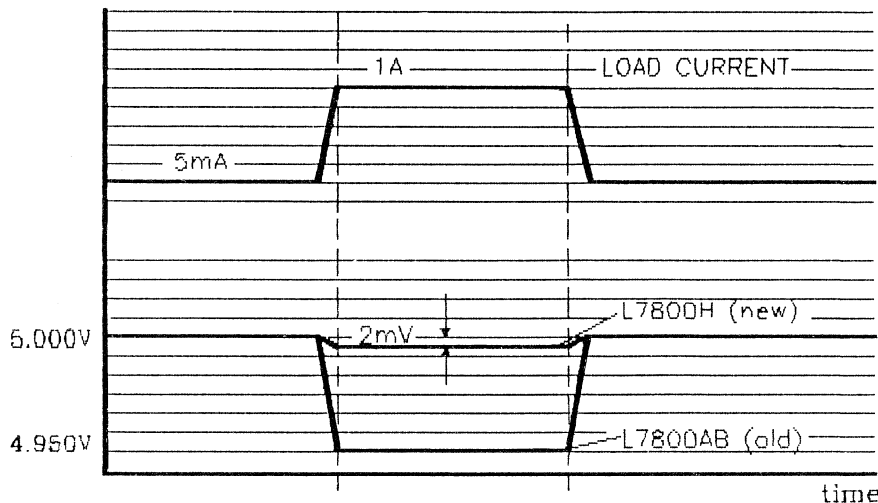


Figure 1. Load regulation - voltage variation on a 1A current pulse.

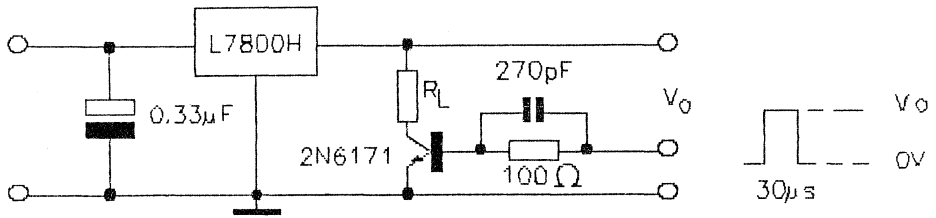


Figure 2. Load regulation test circuit

The very high precision of V_{out} together with excellent load and line regulation make this regulator highly suitable for applications where stability of V_{out} is a mandatory requirement. The typical drop out voltage for $I_{out} = 1A$ is 2V, figure 3.

The precision of this integrated circuit has been achieved by preventing piezoelectric effects in the resistors that have a primary influence on the band gap voltage and avoiding parasitic MOS structures that have a detrimental effect on the long term stability of the circuit. In fact the stability of the IC is such that the values of the input and

output capacitors are not critical.

The precision with which the output voltage regulation is achieved is obtained by trimming two resistors that adjust the output voltage of the band gap reference. The band gap reference is the part of the circuit that generates a voltage that is independent of temperature, load current and input voltage. The output voltage is fed back and compared with this reference, the error voltage is then used to control the device regulation.

Looking at the schematic, (figure 4), we can see

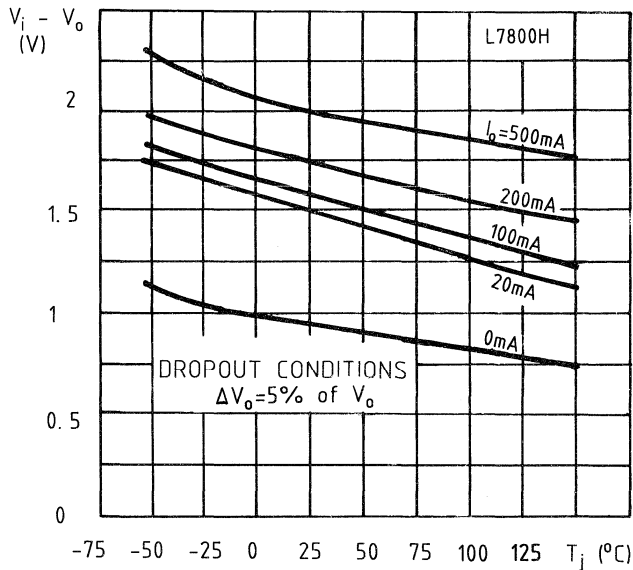


Figure 3. Dropout voltage versus junction temperature.

that V_{out} is given by:

$$V_{out} = 4 V_{be} + \frac{R_2}{R_3} \cdot \frac{kT}{q} \ln \frac{R_2}{R_1}$$

(where: K = Boltzmann constant,
 T = absolute temperature,
 q = charge on an electron)

If we decrease the value of R_2 , V_{out} decreases;
 decreasing the value of R_3 increases V_{out} .

The resistors R_2 and R_3 can be trimmed by zener zapping a process where sections of resistors within the silicon chip can be short circuited by fusing a zener diode. This process is carried out on the wafer during testing.

Using this kind of trimming technique, we can adjust the value of V_{out} over the range ± 200 mV in 50 mV steps. This enables all the devices with an output voltage in the range of 4.75 - 5.25V to be brought back to within $\pm 1\%$ of the nominal output voltage.

The layout in figure 5 shows the areas where the multi - resistor networks (R_2 and R_3 of figure 4) and the zeners for trimming them lie.

The second feature of this device, the improved load regulation, is obtained by the introduction of a SENSE PAD. The output of the band gap circuit is connected through the SENSE PAD directly to the output pin, thus eliminating any voltage drop in the bonding wire due to the effect of changing load current.

The introduction of the SENSE PAD dramatically improves the load regulation to less than 5 mV, about ten times lower than first generation regulators.

The excellent load regulation of this voltage regulator makes it suitable for those applications where a very stable reference voltage is required. Typical applications include the power supplies for printer motors where good speed regulation is required as the load on the motor varies and in instrumentation power supplies.

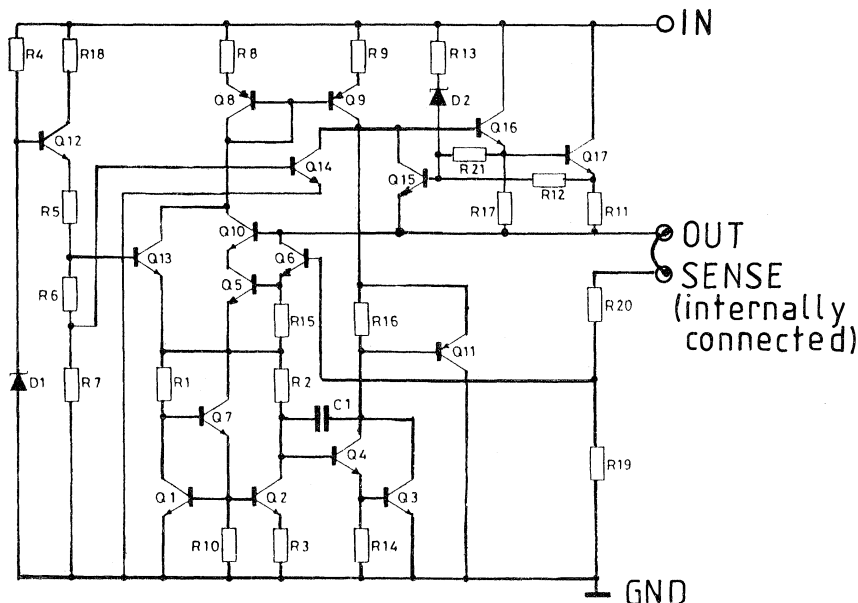


Figure 4. Circuit diagram for the L7800H

In actual application the normal circuit requirements for the standard L7800 series should be followed. Any by-pass capacitor should be chosen to reduce the input ripple and should be mounted with the shortest possible leads close to the regulator. Normal good construction techniques should be used to minimise ground loops and lead resistance voltage drops. With adequate heat sinking over 1A can be taken from the output.

The extra cost of the L7800HB series is very small compared to the improvements it offers in circuit operation.

CONCLUSION

The new 1% L7800HB regulator offers designers improved current regulation with reduced voltage excursions. In applications where too high or too low power supply voltages can lead to incorrect circuit function, such as TTL circuits or small motor drives, the improved stability and in the future the option of the fully isolated ISOWATT220 package can reduce component count and circuit costs.

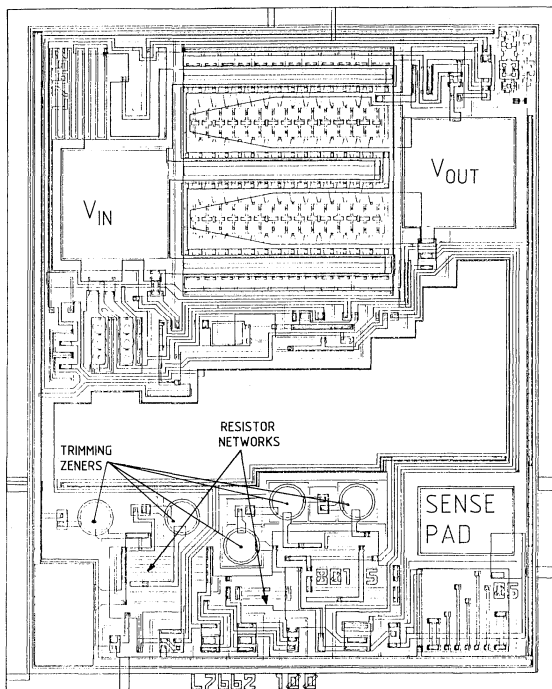


Figure 5. Layout of the L7800HB chip.

LOW DROP VOLTAGE REGULATORS FOR AUTOMOTIVE ELECTRONICS

By S. CISCATO

Linear voltage regulators with an input-output voltage drop of less than 2V are used to ensure continuity of the stabilized output in applications where a battery supply is used. This note describes the characteristics and operation of these devices.

Low drop linear voltage regulators are low voltage (5 to 12V) regulators which are able to provide effective stabilization of the output voltage even when the difference between input voltage and output voltage is less than 2V.

This situation can arise accidentally for a brief period when the main supply source is overloaded. It may also result from a deliberate design decision aimed at reducing the power dissipated in the supply - for example, when the device is used as a post regulator in portable instruments.

Low drop regulators are used widely in automotive applications, a field where integrated circuits have to be particularly rugged. For this reason most low drop devices include protection functions not found in standard regulators. Before describing the SGS THOMSON family of low drop regulators we will therefore begin with a brief description of the automotive electrical environment.

AUTOMOTIVE ENVIRONMENT

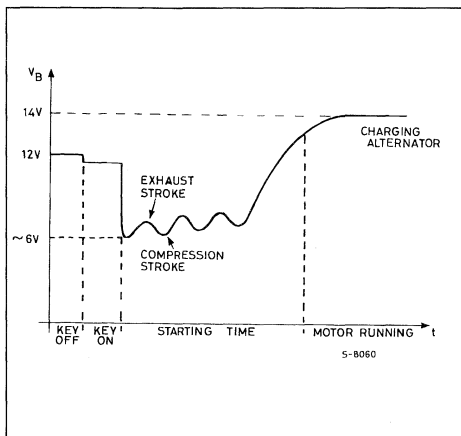
In addition to the battery voltage drop during starting, the automotive field presents a number of other serious problems concerning the regulator input voltage : positive and negative high energy / high voltage transients (load dump and field decay), positive and negative low energy/very-high-voltage spikes (switching spikes), battery reversal and battery voltage doubling.

All of these hazards must be withstood by the regulator without damage over an ambient temperature range very close to military standards (- 40 to + 125°C for underhood devices ; - 40 to + 85°C for other devices). Moreover, an output voltage precision of $\pm 4\%$ to $\pm 2\%$ is required over the whole temperature range and in all conditions of input voltage and load current.

BATTERY VOLTAGE DROP

During motor starting the battery is overloaded by a peak current of up to 100A drawn by the starter motor. In this condition, which persists for 20-30ms, the battery voltage drops to about 6V in very cold weather (figure 1).

Figure 1 : Cold Starting Supply Voltage Drop.



Using standard regulators with a dropout of 1.7V to 2.1V the minimum 4.75V supply necessary for essential functions such as ignition, injection and electronic engine control cannot be guaranteed. Another unfortunate consequence is the loss of RAM memory contents in car radios and trip computers.

A voltage regulator with a voltage drop of less than 1.2V is therefore necessary.

BATTERY VOLTAGE DOUBLING

To aid cold weather starting with a partially flat battery, sometimes two batteries are used in series, doubling the voltage. Regulators must therefore withstand input voltages of 24-26V without disturbing operation.

BATTERY REVERSAL

Voltage regulators must be protected internally against negative input voltages to guard against accidental battery reversal.

LOAD DUMP TRANSIENTS

Load dump transients are high voltage, high energy positive transients.

The response time of the output voltage of an alternator to load variations is very long because of the long time constant of the excitation winding and mechanical inertia.

When the load is reduced instantaneously (by turning off lights, cooling fans and so on) the output voltage of the alternator tends to present a positive peak, the amplitude of which depends on the speed of rotation and the excitation current.

During normal operation this does not cause problems because of the high capacity of the battery which, connected in parallel with the alternator output, is able to absorb the transient energy without a significant increase in voltage.

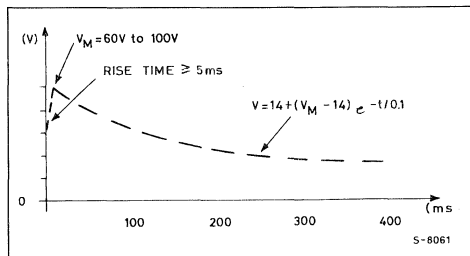
However, motor manufactures impose the standard that electronic devices must be protected against load dump transients because it is possible for the connection between battery and alternator to break.

The worst case voltage peak occurs when the battery-alternator cable is disconnected with the battery discharged and the motor running at its fastest rotation speed. In this case, the load variation is at a maximum and the voltage peak reaches a value comparable with the no-load output of the alternator running at maximum speed with the maximum excitation current.

Figure 2 shows a typical load dump waveform.

Motor manufacturers require that voltage regulators are able to protect themselves and the load against peak voltages of 60 - 100V with an equivalent series resistance of 0.1 to 1 Ω , depending on the type of alternator and external protection device used.

Figure 2 : Load Dump Transient.



FIELD DECAY TRANSIENTS

Field decay transients are high energy, high voltage negative transients.

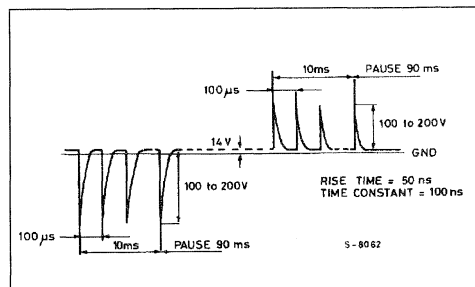
If the ignition switch is turned off while current is flowing in inductive loads (electric motors, alternator field coil and so on) a negative voltage transient appears

on the supply rail. The peak value in modulo of this transient is of the same order of magnitude as a load dump transient. In this case, too, the regulator must protect itself and the load.

SWITCHING SPIKES

Windscreen wiper motors, lamp flashers and ignition sparks behave as high frequency noise generators with an equivalent series resistance of 50 to 500 Ω . The energy associated with these transients is much lower than load dump or field decay transients but the negative and positive peaks can reach 200V. Figure 3 shows the voltage waveform which the regulators must withstand.

Figure 3 : Switching Spikes.



REGULATOR DESIGN

DROPOUT

The dropout voltage of a linear voltage regulator can be defined for a given output current, I_o , as the minimum difference between input and output voltage below which the output voltage is 100mV lower than the voltage measured at I_o with the nominal input voltage. The current I_o must be specified since the dropout voltage increases as the load current increases.

To obtain a dropout voltage of 0.05 to 1V with an output current of 10 to 50mA, the regulator types L387A, L487, L47XX, L48XX, L4920, L4921, LM2930A and LM2931A are configured with a PNP series-pass transistor as shown in figure 4. The PNP transistor is connected in the common emitter configuration and can therefore operate in saturation, yielding the low dropout voltage desired.

For higher dropout values an NPN series-pass element in emitter follower configuration may be used. This approach, shown in Figure 5, is used in the L2600 series regulators which have a maximum dropout voltage of 1.9V at 500mA.

Figure 4 : PNP Series Pass Transistor in Common Emitter Configuration for very Low Drop Out Voltage Regulators.

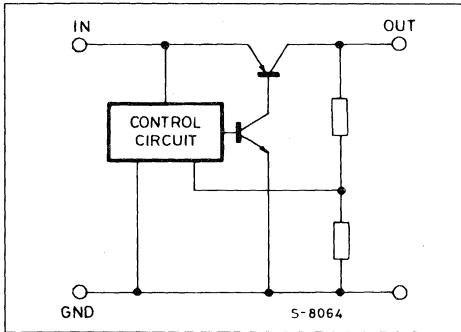
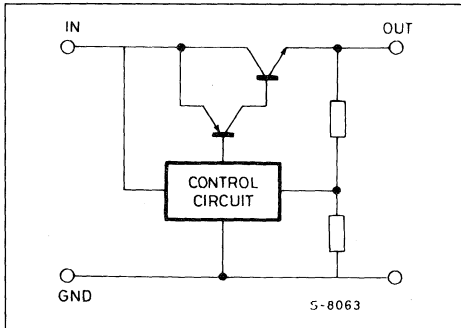


Figure 5 : NPN Series Pass Transistor in Emitter Follower Configuration.



CURRENT CONSUMPTION/QUIESCENT CURRENT

The circuit configurations shown in figures 4 and 5 behave differently as far as concerns the current consumed by the device but not delivered to the load. In the case of figure 5, this current is that necessary for the functioning of the auxiliary circuitry of the regulator (voltage reference, op amp and so on). The base current of the output transistor flows into the load.

In the Figure 4 circuit, in contrast, the base current of the output transistor does not flow through the load and, particularly in saturation, depends heavily on the load current.

Normally lateral PNP transistors are chosen for ICs because they can withstand high positive and negative overvoltages. When negative overvoltages at the input do not occur, or are eliminated by external protection devices, vertical PNP transistors can be used in place of lateral types.

Since vertical PNP transistors have higher gain the current consumed in the regulator is significantly reduced. Vertical PNP transistors will be used in future designs.

VOLTAGE REFERENCE

The wide operating range of input voltage (6 to 26V) and ambient temperature (40 to 125 °C) over which high output voltage precision is required means that a well stabilized voltage reference must be used.

All low drop regulators use bandgap type voltage references (see figure 6). In this structure the two transistors Q_2 and Q_1 have an emitter area ratio of 10 and carry equal collector currents imposed by the current mirror Q_3 , Q_4 , Q_5 . In these conditions the base-emitter voltages of Q_1 and Q_2 differ (at 25 °C) by :

$$V_{BE} = \frac{KT}{q} \ln \frac{A(Q_2)}{A(Q_1)} = 60 \text{ mV}$$

$$\text{where } \frac{A(Q_2)}{A(Q_1)} = 10 \text{ (emitter area ratio)}$$

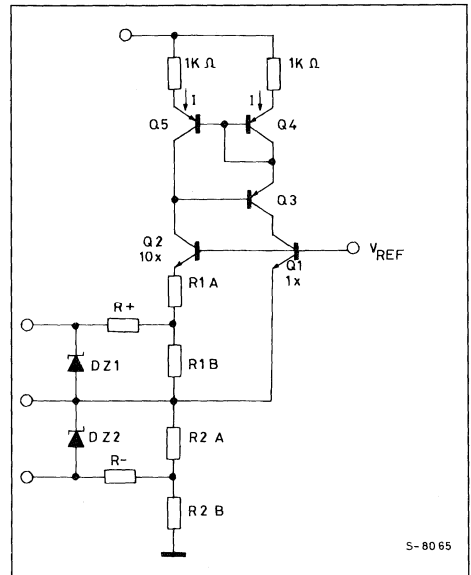
$$\frac{KT}{q} = 26 \text{ mV}$$

K = Boltzmann's constant

T = Temperature in Kelvin

q = Charge on an electron

Figure 6 : Bandgap Voltage Reference Circuit in Low Drop Voltage Regulators.



APPLICATION NOTE

The rejection of V_{ref} to variations in the supply voltage is improved by supplying the reference circuit from a stabilized voltage. This is achieved in the L26XX, L48XX, L4920, L4921, LM2930A and LM2931A regulators by means of a preregulator. In the L487, analysing the Figure 6 circuit gives :

$$V_{ref} = V_{BE}(Q_1) + 2 \frac{R_1}{R_2} \Delta V_{BE}(Q_2, Q_1)$$

To maintain V_{ref} constant as temperature varies it

is necessary that $\frac{dV_{ref}}{dT} = 0$ which implies choosing $\frac{R_2}{R_1}$ so that $\frac{2R_2}{R_1} \cdot \frac{60}{T(25^\circ)} + \frac{dV_{BE}(Q_1)}{dT} = 0$

where $T(25^\circ) = 298 \text{ K}$

$\frac{dV_{BE}(Q_1)}{dT}$ = negative temperature coefficient of

the base-emitter voltage.

In L387A and L47XX regulators, in contrast, the supply to the bandgap is switched from the input to the output as soon as the nominal output voltage is reached (figures 7, 8, 9). The variation in output voltage with temperature is shown in figure 10.

Figure 7: Block Diagram of L2600 Series Regulators.

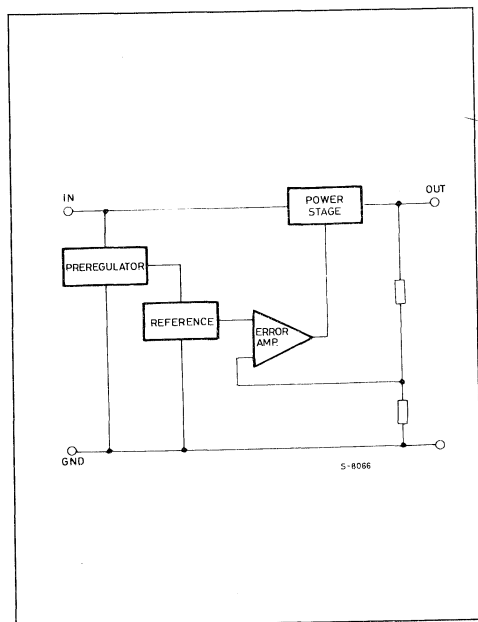


Figure 8: Block Diagram of L387A and L487 Series Regulators.

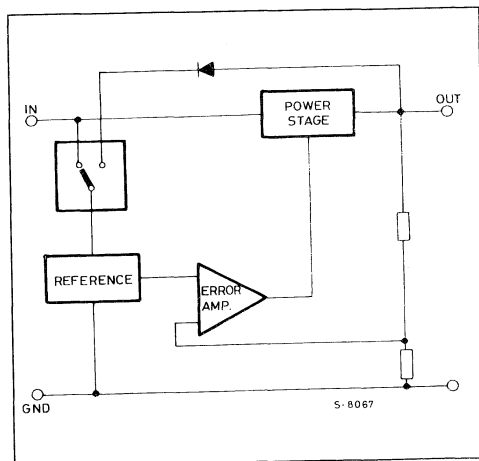


Figure 9: Block Diagram of LM2930A, LM2931A and L4800 Series Regulators.

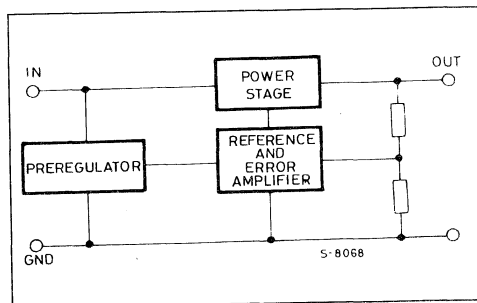
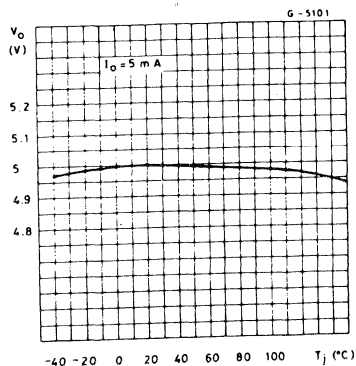


Figure 10: Outputs Voltage vs. Temperature.



PROTECTION AGAINST HIGH ENERGY TRANSIENTS

To protect the LM2930A, LM2931A, L4920, L4921 and L48XX regulators against high-voltage, high-energy positive transients the basic circuit shown in Figure 11 is used. The zeners in this circuit limit the supply voltage to the maximum operating value and turn off the output stage. The output transistor can thus withstand voltages up to the BV_{CES} , breakdown voltage.

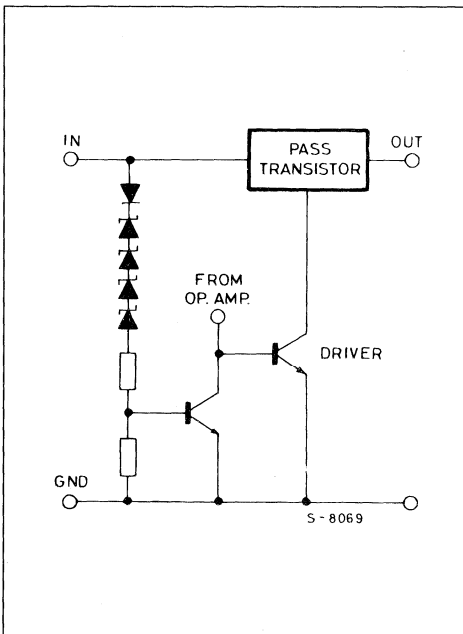
In the other regulators (L487, L387A, L47XX and L26XX) the supply to the internal circuits is also turned off.

The speed of intervention of these protection schemes is fast enough to ensure that the regulator can withstand high energy transients with a rising slope of 10V/ μ s without problems, interrupting normal operation only momentarily.

Protection against negative transients is provided by the high series impedance of the possible current paths and the reverse BV_{BEO} breakdown voltage of the lateral PNP transistors (BV_{CBO}).

The breakdown voltages BV_{CES} and BV_{CBO} depend on the technology therefore the transient capability is $\pm 60V$, $\pm 80V$ or $\pm 100V$ for the various types.

Figure 11 : Overvoltage Protection Circuit.

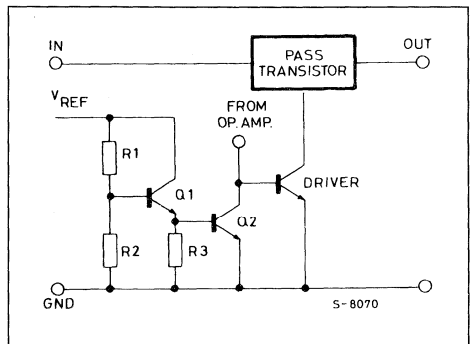


PROTECTION AGAINST LOW ENERGY OVERVOLTAGES

As shown in figure 3, the low energy overvoltages which the devices must resist have very brief rise time and can exceed the breakdown voltages. The protection schemes described above are therefore insufficient. However, since the energy associated with these transients is very low, the regulators can withstand them without problems. Nevertheless it is advisable to place a capacitor of around 100nF at the input.

All of the low drop regulators except the L26XX types need a compensation capacitor at the output. This capacitor also provides extra filtering for low energy transients because it has a low impedance at high frequencies.

Figure 12 : Thermal Protection Circuit.



THERMAL PROTECTION

When the junction temperature exceeds the safe maximum for the device a thermal protection circuit (figure 12) holds the output transistor off until the overtemperature condition has passed.

In the figure 12 circuit the resistors R1, R2 and R3 are calculated so that the base voltage of Q₁ is 600mV, thus preventing the conduction of Q₁ and Q₂.

As the junction temperature increases the minimum V_{BE} for conduction of the two transistors fall until, at about 15°C , $2 V_{BE} = 600\text{mV}$, the two transistors conduct and Q_2 turns off the output transistor driver.

CURRENT PROTECTION

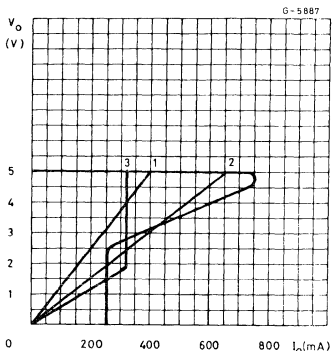
In the L487, L387A and L26XX regulators the output current is limited to its maximum value in the event of a short circuit. A special circuit acts on the base of the output transistor, preventing the output current from exceeding the limit set for the duration of the overload.

In the L4920, L4921, LM2930A, LM2931A and L48XX regulators a foldback circuit (figure 13) is used to limit the power dissipated in both the devices and the load in short circuit conditions. The current is limited to a low value (I_{sc}) of about 200 mA as soon as it exceeds the maximum value. The output voltage in this condition reaches a value corresponding to the current I_{sc} flowing through the load.

When the overload condition is removed the output voltage only returns to the nominal load value if the new static load line does not intersect the negative slope region of the curve in figure 13. If it does, the new operating point will be at the intersection.

It is important to note that when power is applied, if the load line intersects the curve in the negative slope region, the regulator will operate with a lower-than-nominal voltage. This can happen with a passive load greater than the normal load (even if it is less than the maximum load I_M) or with active loads such as a current sinker which draw more than I_{sc} even at low voltages (figure 13, curve 3).

Figure 13 : 1) Acceptable Load Line for Turn-on
2) Unacceptable Load Line for Turn-on.



EXTERNAL COMPENSATION

Since the purpose of a voltage regulator is to supply a fixed output voltage in spite of supply and load variations, the open loop gain of the regulator must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shifts due to other poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be the capacitor used to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequency

too low to be compensated by a capacitor which can be integrated. For the L487, L47XX, L48XX, L387A, LM2930A and LM2931A external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The parasitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is 47 F (100 μ F for L4800 series).

In the L2600, which uses an NPN power transistor, the stabilization capacitor is small enough to be integrated so no output capacitor is needed. Indeed, if an output capacitor is used it may cause oscillation unless it is greater than 100 μ F, in which case it would itself be the dominant pole. If an electrolytic capacitor of more than 100 μ F is used, a small capacitor must not be added in parallel or with the ESR of the electrolytic it would form another pole, worsening the stability of the system.

TURN-ON WITH CAPACITIVE LOADS

A load which presents a significant capacity between the output and ground (including the external compensation capacitor) will be seen by the regulator as a short circuit when power is applied. The regulator therefore delivers the short circuit current until the load capacitor has been charged to the nominal value.

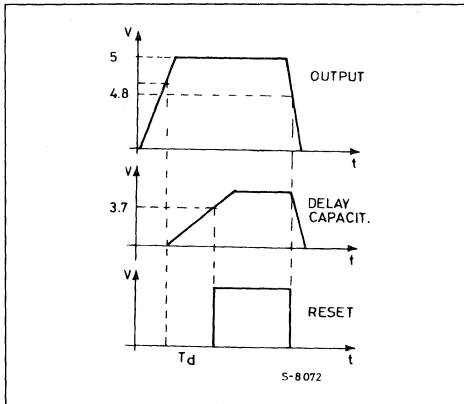
This factor is extremely important for the dimensioning of the power source. Even a very small DC load can in such cases behave like a maximum load and the power drained from the supply is the sum of the short circuit current delivered to the load and the maximum current consumed in the regulator.

Moreover, as explained above, in regulators with foldback protection the static load line must not cross the negative slope region of figure 13 or the output voltage will not reach the nominal value when power is applied.

SPECIAL FUNCTIONS

RESET

The L387A and L487 include a power on/off reset function which inhibits the operation of circuits supplied by the regulator when the output voltage is too low (4.75V) to guarantee correct operation of logic (figure 14). To avoid malfunctions a delay is also introduced so that the enable signal is only issued some time after the safe output voltage has been reached.

Figure 14 : Reset Timing Waveforms.

The reset circuitry (figure 15) consists of :

- a comparator connected between the voltage reference and a tap of the output divider, the voltage of which is higher than the feedback voltage ;
- an SCR to memorize any brief glitches in the output voltage that can cause some trouble with the logic.
- a delay circuit with an external capacitor charged by an internal current source

This function has been integrated into the voltage regulator to exploit the basic advantage of taking information at the source. The use of double calibrations can thus be avoided.

For the correct operation of the reset function, two basic relations must be satisfied in all cases

$$\begin{aligned} V_{res \max} &< V_{out \min} & (1) \\ V_{res \min} &> 4.75 \text{ V} & (2) \end{aligned}$$

where $V_{res \max}/V_{res \min}$ are maximum/minimum value for the reset signal going high-low.

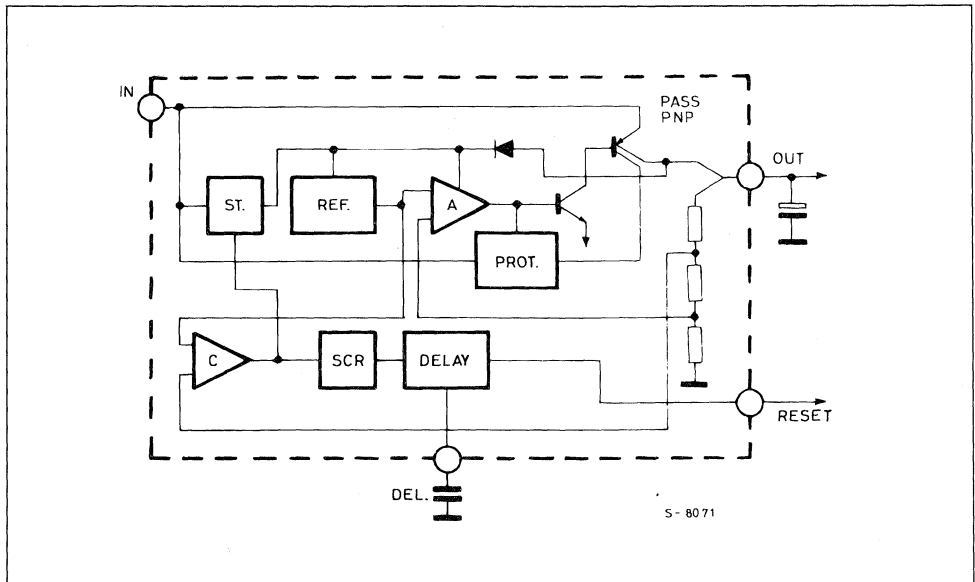
(1) means that the RESET signal must be high when the device is regulating

(2) means that the RESET signal must be low when the output voltage goes under 95 % of the nominal (5V). Expressions (1) and (2) can be rewritten as :

$$(V_{res \max} - V_{res \min}) + (V_{nom} - V_{out \min}) < V_{nom} - 4.75 \text{ V} \quad (3)$$

This means that the sum of all the errors in the worst case must be less than 5 % (250mV).

- absolute spread of the reference
- error due to the load regulation (1 % max)
- error due to the offset of the reset comparator and error amplifier (0.5 %)
- errors due to the output divider (0.5 %)
- hysteresis of the comparator to speed up the transitions (50mV that is 1 % referred to 5V output)

Figure 15 : Schematic Block Diagram of a Voltage Regulator with Reset Function.

APPLICATION NOTE

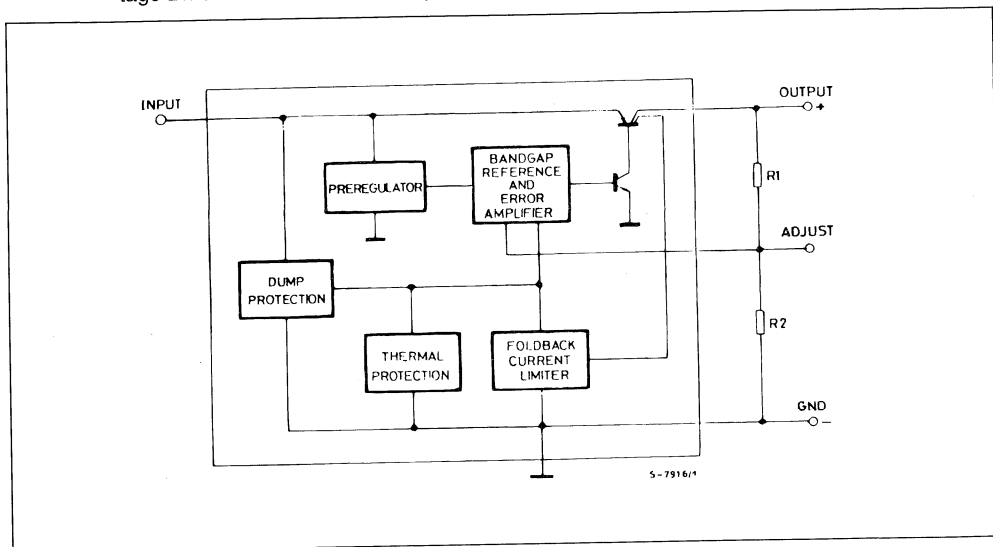
VARIABLE OUTPUT VOLTAGE

The L4920 and L4921 are structurally identical to L48XX series regulators except that the voltage divider in the feedback loop is available externally (figure 16). The output voltage can therefore be varied from 1.25V (the reference voltage) to 20V. It should be noted, however, that the minimum input voltage is 5.1V for operation with output voltages

below 4.5V (otherwise the internal circuits will not work). For output voltages above 4.5V the input voltage must be at least equal to the output voltage plus the dropout voltage. The L4920 and L4921 are therefore low dropout regulators only for voltages above 4.5V.

A value of 6 K Ω is recommended for R2 to match the internal circuitry.

Figure 16 : The L4920 and L4921 are Structurally Identical to L48XX Series Regulators Except that the Voltage Divider in the Feedback Loop is Available Externally.



THERMAL MANAGEMENT

DESIGNING WITH THERMAL IMPEDANCE

BY T.HOPKINS, C.COZZETTI, R.TIZIANI

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ABSTRACT

Power switching techniques used in many modern control systems are characterized by single or repetitive power pulses, which can reach several hundred watts each. In these applications where the pulse width is often limited to a few milliseconds, cost effective thermal design considers the effect of thermal capacitance. When this thermal capacitance is large enough, it can limit the junction temperature to within the ratings of the device even in the presence of high dissipation peaks. This paper discusses thermal impedance and the main parameters influencing it. Empirical measurements of the thermal impedance of some standard plastic packages showing the effective thermal impedance under pulsed conditions are also presented.

INTRODUCTION

Power switching applications are becoming very common in many industrial, computer and automotive ICs. In these applications, such as switching power supplies and PWM inductive load drivers, power dissipation is limited to short times, with single or repeated pulses. The normal description of the thermal performance of an IC package, $R_{th(j-a)}$ (junction to ambient thermal resistance), is of little help in these pulsed applications and leads to a redundant and expensive thermal design.

This paper will discuss the thermal impedance and the main factors influencing it in plastic semiconductor packages. Experimental evaluations of the thermal performance of small signal, medium power, and high power packages will be presented as case examples. The effects of the thermal capacitance of the packages when dealing with low duty cycle power dissipation will be presented and evaluated in each of the example cases.

THERMAL IMPEDANCE MODEL FOR PLASTIC PACKAGES

The complete thermal impedance of a device can be modeled by combining two elements, the thermal resistance and the thermal capacitance.

The thermal resistance, R_{th} , quantifies the capability of a given thermal path to transfer heat. The general definition of resistance of the thermal path, which includes the three different modes of heat dissipation (conduction, convection and radiation), is the ratio between the temperature increase above the reference and the heat flow, DP , and is given by the equation :

$$R_{th} = \frac{\Delta T}{\Delta P} = \frac{\Delta T}{\frac{\Delta Q}{\Delta t}}$$

Where : ΔQ = heat
 Δt = time

Thermal capacitance, C_{th} , is a measure of the capability of accumulating heat, like a capacitor accumulates a charge. For a given structural element, C_{th} depends on the specific heat, c , volume V , and density d , according to the relationship :

$$C_{th} = c d V$$

The resulting temperature increase when the element has accumulated the heat Q , is given by the equation :

$$\Delta T = \Delta Q / C_{th}$$

The electrical analogy of the thermal behaviour for a given application consisting of an active device, package, printed circuit board, external heat sink and external ambient is a chain of RC cells, each having a characteristic time constant :

$$\tau = RC$$

To show how each cell contributes to the thermal impedance of the finished device consider the simplified example shown in figure 1. The example device consists of a dissipating element (integrated circuit) soldered on a copper frame surrounded by a plastic compound with no external heat sink. Its equivalent electrical circuit is shown in figure 2.

The first cell, shown in figure 2, represents the thermal characteristics of the silicon itself and is characterized by the small volume with a correspondingly low thermal capacitance, in the order of a few mJ/C. The thermal resistance between the junction and

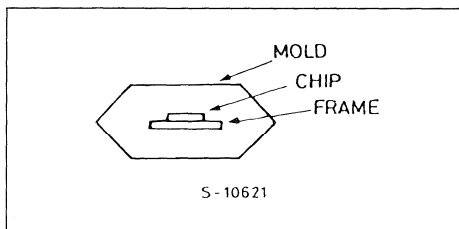
the silicon/slug interface is of about 0.2 to 2 °C/W, depending on die size and on the size of the dissipating elements existing on the silicon. The time constant of this cell is typically in the order of a few milliseconds.

The second cell represents the good conductive path from the silicon/frame interface to the frame periphery. In power packages, where the die is often soldered directly to the external tab of the package, the thermal capacitance can be large. The time constant for this cell is in the order of seconds.

From this point, heat is transferred by conduction to the molded block of the package, with a large thermal resistance and capacitance. The time constant of the third cell is in the order of hundreds of seconds.

After the plastic has heated, convection and radiation to the ambient starts. Since a negligible capacitance is associated with this phase, it is represented by a purely resistive element.

Figure 1 : Simplified Package Outline.



When power is switched on, the junction temperature increase is ruled by the heat accumulation in the cells, each following its own time constant according with the equation :

$$\Delta T = R_{th} P_d [1 - e^{(t/\tau)}]$$

The steady state junction temperature, T_j , is a function of the $R_{th(j-a)}$ of the system, but the temperature increase is dominated by thermal impedance in the transient phase, as is the case in switching applications.

A simplified example of how the time constants of each cell contribute to the temperature rise is shown in figure 3 where the contribution of the cells of figure 2 is exaggerated for a better understanding.

When working with actual packages, it is observed that the last two sections of the equivalent circuit are not as simple as in this model and possible changes will be discussed later. However, with switching times shorter than few seconds, the model is sufficient for most situations.

Figure 2 : Equivalent Thermal Circuit of Simplified.

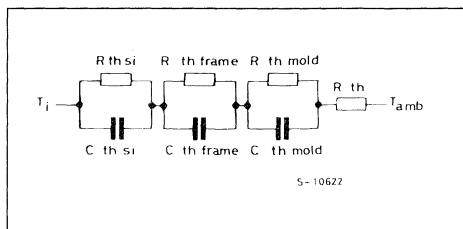
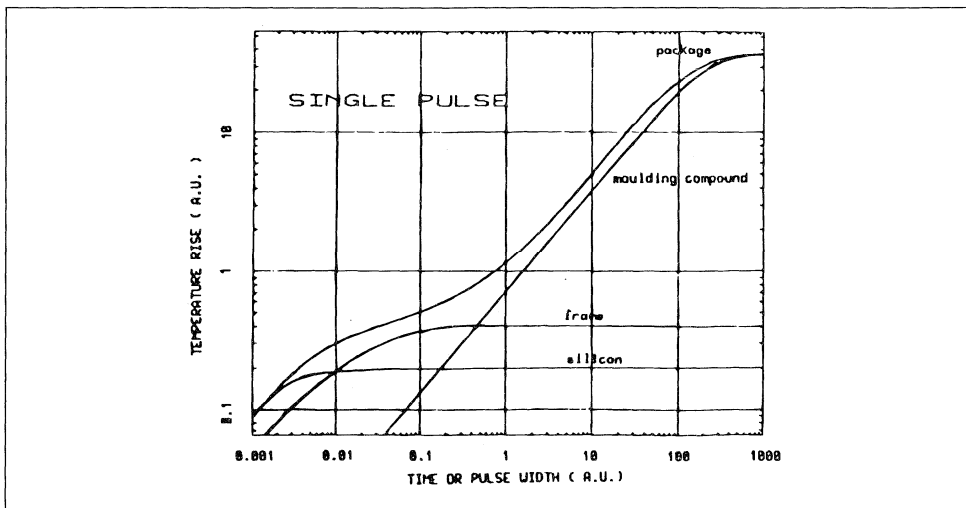


Figure 3 : Time Constant Contribution of Each Thermal Cell (qualitative example).



EXPERIMENTAL MEASUREMENTS

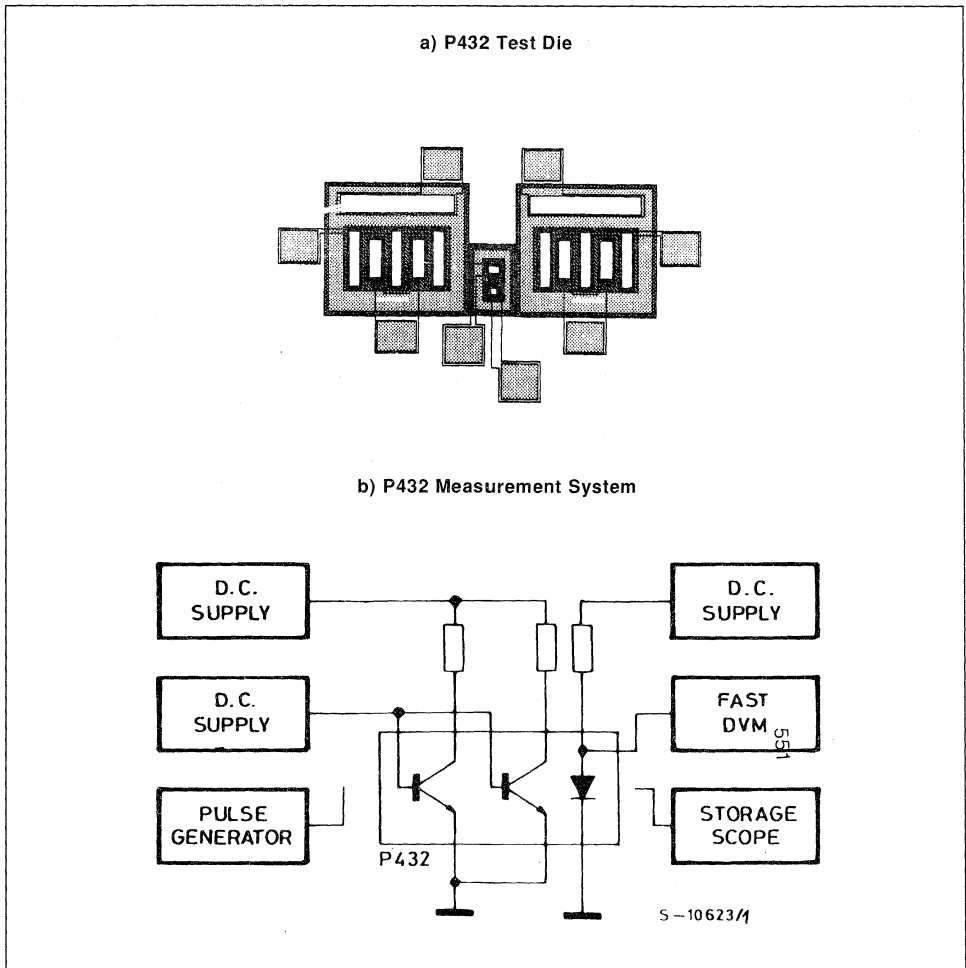
When thermal measurements on plastic packages are performed, the first consideration is the lack of a standard method. At present, only draft specifications exist, proposed last year and not yet standardized (1).

The experimental method used internally for evaluations since 1984 has anticipated these preliminary recommendations to some extent, as it is based on test patterns having, as dissipating element, two power transistors and, as measurement element, a sensing diode placed in the thermal plateau arising when the transistors are biased in parallel.

The method used has been presented elsewhere (2) for the pattern P432 (shown in figure 4), which uses two small (1000 sq mils) bipolar power transistors and has a maximum DC power capability of 40 W (limited by second breakdown of the dissipating elements).

A similar methodology was followed with the new H029 pattern, based on two D-Mos transistors (3) having a total size of 17.000 sq mils and a DC power capability of 300 W on an infinite heat sink at room temperature (limited by thermal resistance and by max operating temperature of the plastics).

Figure 4.



APPLICATION NOTE

Using the thermal evaluation die, four sets of measurements were performed on an assortment of insertion and surface mount packages produced by SGS-Thomson Microelectronics. The complete characterization is available elsewhere (4). The four measurements taken were :

- 1) Junction to Case Thermal Resistance (Power Packages)
- 2) Junction to Ambient Thermal Resistance
- 3) Transient Thermal Impedance (Single Pulse)
- 4) Peak Transient Thermal Impedance (Repeated Pulses)

Figure 5.

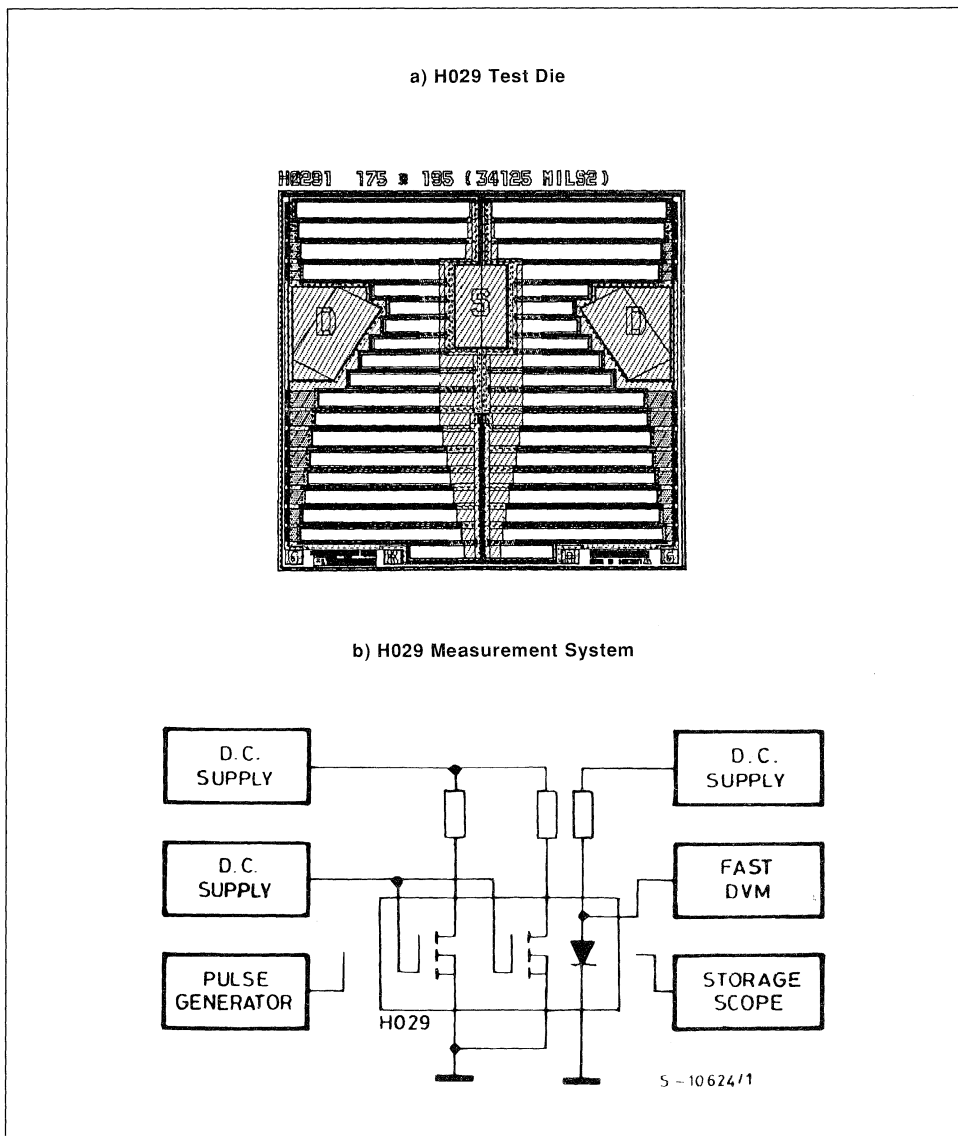
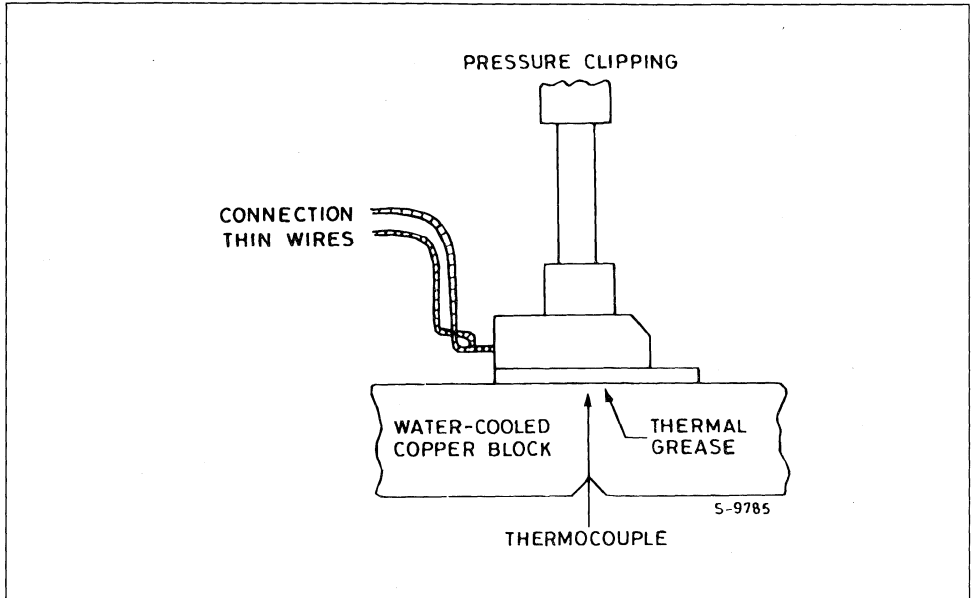


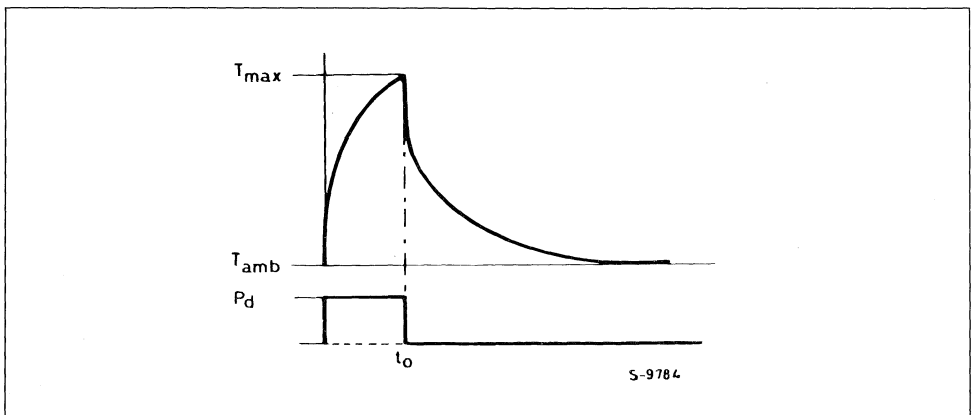
Figure 6 : Set-up for $R_{th(j-c)}$ Measurement.

The junction to case thermal resistance measurements were taken using the well known setup shown in figure 6 where the power device is clamped against a large mass of controlled temperature.

The junction to ambient thermal resistance in still air, was measured with the package soldered on standard test boards, described later, and suspended in 1 cubic foot box, to prevent air movement.

The single pulse transient thermal impedance was

measured in still air by applying a single power pulse of duration t_0 to the device. The exponential temperature rise in response to the power pulse is shown qualitatively in figure 7. In the presence of one single power pulse the temperature, ΔT_{max} , reached at time t_0 , is lower than the steady state temperature calculated from the junction to ambient thermal resistance. The transient thermal impedance R_0 , is obtained from the ratio $\Delta T_{max}/P_d$.

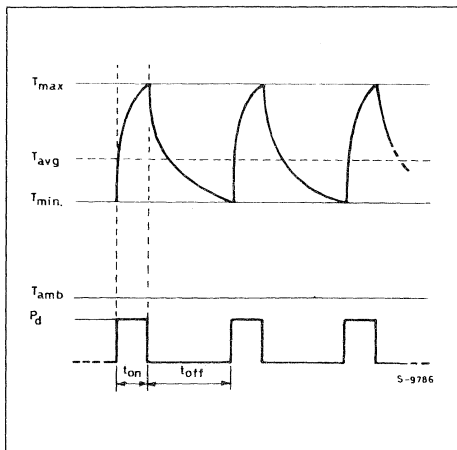
Figure 7 : Transient Thermal Response for a Single Pulse.

APPLICATION NOTE

The peak transient thermal impedance for a series of repetitive pulses was measured by applying a string of power pulses to the device in free air. When power pulses of the same height, P_d , are repeated with a given duty cycle, DC, and the pulse length, t_p , is shorter than the total time constant of the system, the train of pulses is seen as a continuous source with mean power level given by the equation :

$$P_{davg} = P_d DC$$

Figure 8 : Transient Thermal Response for Repetitive Pulses.



On the other hand, the silicon die has a thermal time constant of 1 to 2 ms and the die temperature is able to follow frequencies of some kHz. The result is that T_j oscillates about the average value :

$$\Delta T_{javg} = R_{th} P_{davg}$$

The resulting die temperature excursions are shown qualitatively in figure 8. The peak thermal impedance, R_{thp} , corresponding to the peak temperature, ΔT_{max} , at the equilibrium can be defined :

$$R_{thp} = \Delta T_{max} / P_d = F(t_p, DC)$$

The value of R_{thp} is a function of pulse width and duty cycle. Knowledge of R_{thp} is very important to avoid a peak temperature higher than specified values (usually 150°C).

EXPERIMENTAL RESULTS

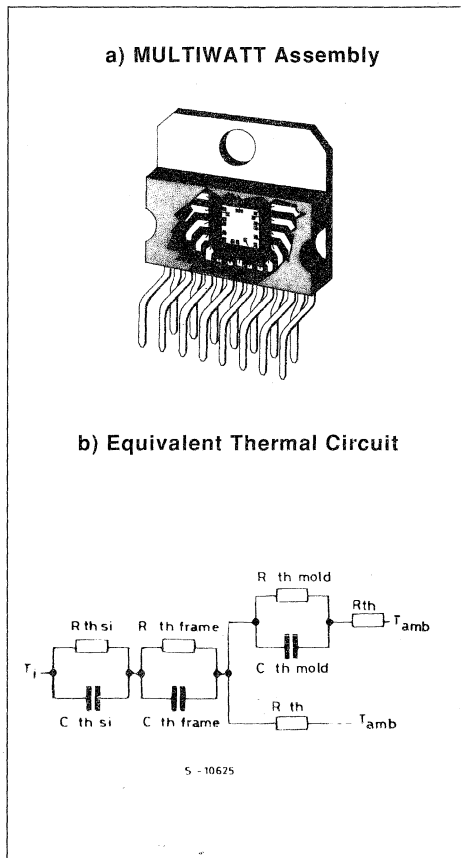
The experimental measurements taken on several of the packages tested are summarized in the following sections.

MULTIWATT PACKAGE

The MULTIWATT (R) package, shown in figure 9a, is a multileaded power package in which the die is attached directly to the tab of package using a soft solder

(Pb/Sn) die attach. The tab of the package is a 1.5 mm thick copper alloy slug. The thermal model of the MULTIWATT, shown in figure 9b, is not much different from that shown in figure 2. The main difference being that when heat reaches the edge of the slug, two parallel paths are possible ; conduction towards the molding compound, and convection and radiation towards the ambient. After a given time, convection and radiation take place from the plastic.

Figure 9.



Using the two test die, the measured junction to case thermal resistance is :

$$P432 \quad R_{th(j-c)} = 2^{\circ}C/W$$

$$H029 \quad R_{th(j-c)} = 0.4^{\circ}C/W$$

The measured time constant is approximately 1 ms for each of the two test patterns, but the two devices have a different steady state temperature rise.

The second cell shown in figure 9 is dominated by the large thermal mass of the slug. The thermal resistance of the slug, R_{thslug} is about $1\text{ }^{\circ}\text{C/W}$ and the thermal time constant of the slug is in the order of 1 second.

The third RC cell in the model has a long time constant due to the mass of the plastic molding and its low thermal conductivity. For this cell the steady state is reached after hundreds of seconds.

For the MULTIWATT the DC thermal resistance of the package in free air, R_{thja} , is $36\text{ }^{\circ}\text{C/W}$ with the P432 die and $34.5\text{ }^{\circ}\text{C/W}$ with the H029 die.

Figure 10 shows the single pulse transient thermal impedance for the MULTIWATT with both the P432 and H029 test die. As can be seen on the graph, the package is capable of high dissipation for short periods of time. For a die like the H029 the power device is capable of 700 to 800 W for pulse widths in the range of 1 to 10 ms. For times up to a few seconds the effective thermal resistance for a single pulse is still in the range of 1 to $3\text{ }^{\circ}\text{C/W}$.

The peak transient thermal impedance for the MULTIWATT package containing the P432 die in free air is shown in figure 11.

POWER DIP PACKAGE

The power DIP package is a derivative of standard small signal DIP packages with a number of leads connected to the die pad for heat transfer to external heat sinks. With this technique low cost heat sinks can be integrated on the printed circuit board as shown in figure 12a. The thermal model of the power DIP, shown in figure 12b accounts for the external heat sink on the circuit board by adding a second RC cell in parallel with the cell corresponding to the molding compound.

In this model, the second cell has a shorter time constant than for the MULTIWATT package, due in large part to the smaller quantity of copper in the frame (the frame thickness is 0.4 mm compared to 1.5 mm). Thus the capacitance is reduced and the resistance increased.

The increased thermal impedance due to the frame can partially be compensated by a better thermal exchange to the ambient by adding copper to the heat sink on the board. The DC thermal resistance between the junction and ambient can be reduced to the same range as the MULTIWATT package in free air, as shown in figure 13.

Figure 10 : Transient Thermal Response MULTIWATT Package.

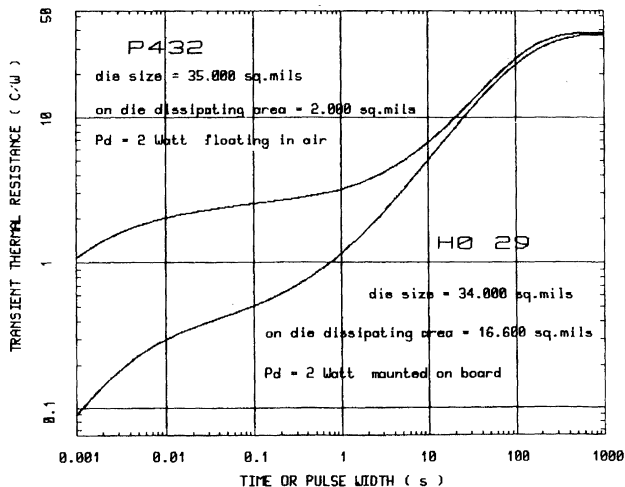


Figure 11 : Peak Thermal Resistance MULTIWATT Package.

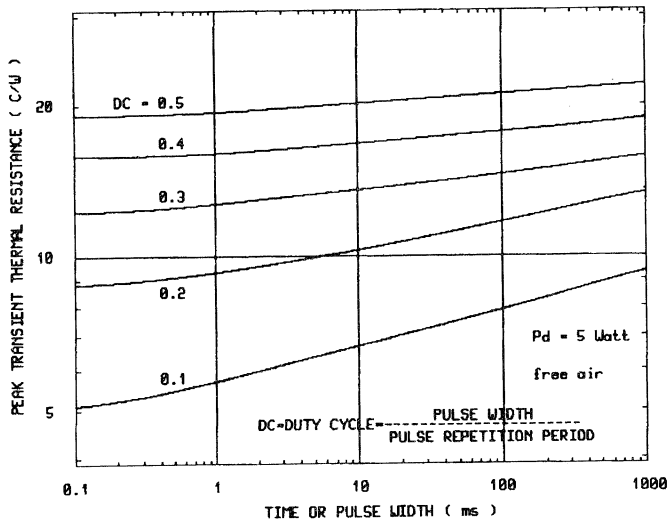
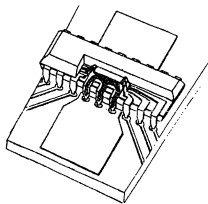
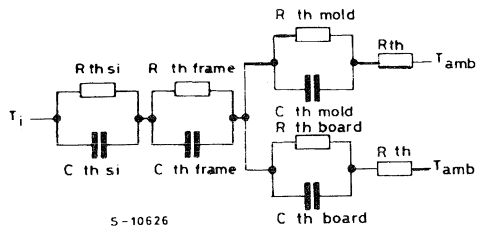


Figure 12.

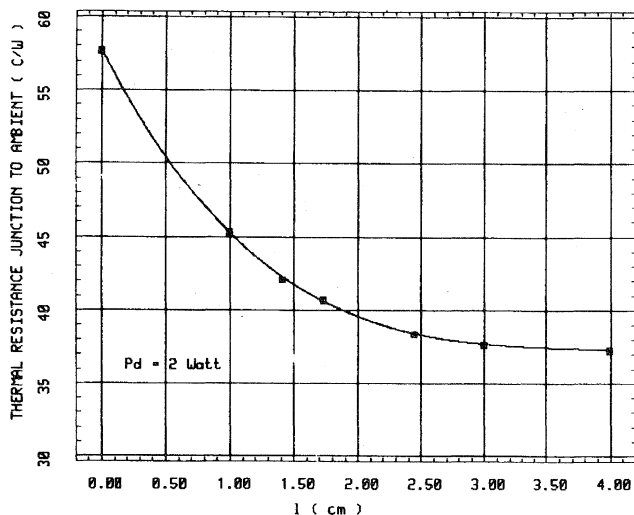


a) Power DIP Package



b) Equivalent Thermal Circuit

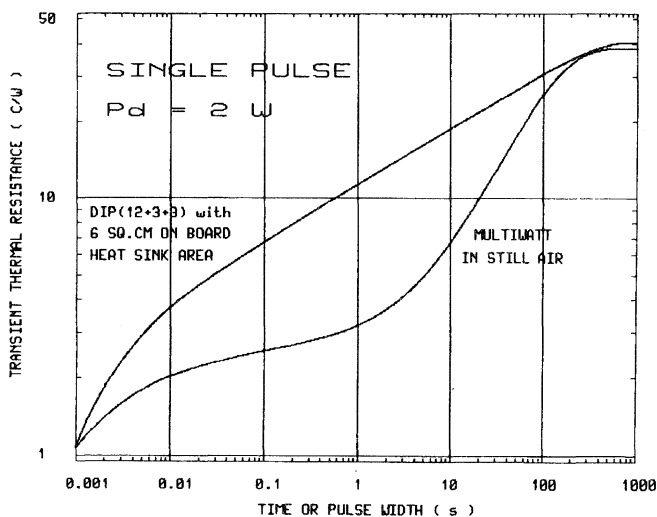
Figure 13 : $R_{th}(j - a)$ vs. PCB Heat Sink Size 12 + 3 + 3 Power Dip.



As a comparison, figure 14 compares the thermal performance of the power DIP and the MULTIWATT package. It is clearly seen that even though the DC

thermal resistance may be similar, the MULTIWATT is superior in its performance for pulsed applications.

Figure 14 : Transient Thermal Impedance for Single Pulses in Power DIP and MULTIWATT Packages.



STANDARD SIGNAL PACKAGES

In standard, small signal, packages the easiest thermal path is from the die to the ambient through the molding compound. However, if a high conductivity frame, like a copper lead frame, is used another path exists in parallel. Figure 15 shows the equivalent thermal model of such a package. The effectiveness of a copper frame in transferring heat to the board

can be seen in the experimental results in DC conditions.

Table 1 shows the thermal resistance of some standard signal packages in two different conditions ; with the device floating in still air connected to the measurement circuit by thin wires and the same device soldered on a test board.

Table 1 : Thermal Resistance of Signal Packages

Package	Frame Thickness & Material	R _{th} (j-a) Floating	°C/W on Board
DIP 8	(0.4 mm Copper)	125-165	78-90
DIP 14	(0.4 mm Copper)	98-128	64-73
DIP 16	(0.4 mm Copper)	95-124	62-71
DIP 20	(0.4 mm Copper)	85-112	58-69
DIP 14	(0.25 mm Copper)	115-147	84-95
DIP 20	(0.25 mm Copper)	100-134	76-87
DIP 24	(0.25 mm Copper)	67-84	61-68
DIP 20	(0.25 mm Alloy 42)	158-184	133-145
SO 14	(0.25 mm Copper)	218-250	105-180
PLCC 44	(0.25 mm Copper)	66-83	48-72

The transient thermal resistance for single pulses for the various packages are shown in figures 16 through 20.

The results of the tests, as shown in the preceding figures, show the true capabilities of the packages. For example, the DIP 20 with a Alloy 42 frame is a typical package used for signal processing applications and can dissipate only 0.5 to 0.7 W in steady state conditions. However, the transient thermal impedance for short pulses is low (11 C/W for $t_p = 100$ ms) and almost 7 Watts can be dissipated for 100 ms while keeping the junction temperature rise below 80°C.

The packages using a 0.4 mm Copper frame have a low steady state thermal resistance, especially in

the case of the DIP 20. The thicker lead frame increases the thermal capacitance of the die flag, which greatly improves the transient thermal impedance. In the case of the DIP 20, which has the largest die pad, the transient R_{th} for 100 ms pulses is about 4.3°C/W. This allows the device to dissipate an 18 Watt power pulse while keeping the temperature rise below 80°C.

As with the previous examples the peak transient thermal impedance for repetitive pulses depends on the pulse length and duty cycle as shown in figure 14. With the signal package, however, the effect of the duty cycle becomes much less effective for longer pulses, due primarily to the lower thermal capacitance and hence lower time constant of the frame.

Figure 15.

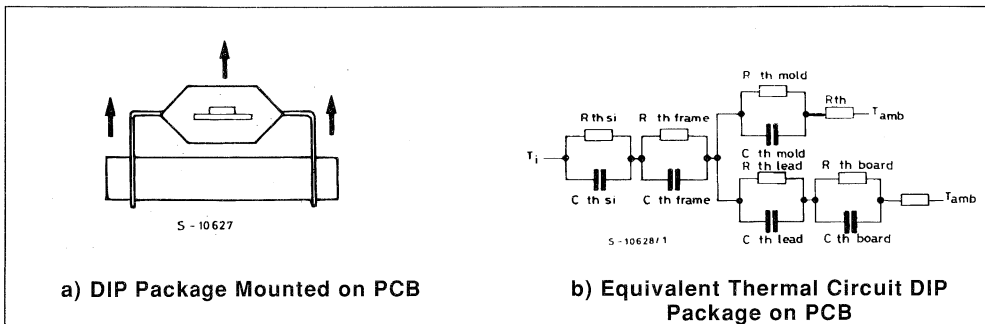


Figure 16 : Transient Thermal Impedance DIP 20 (alloy 42).

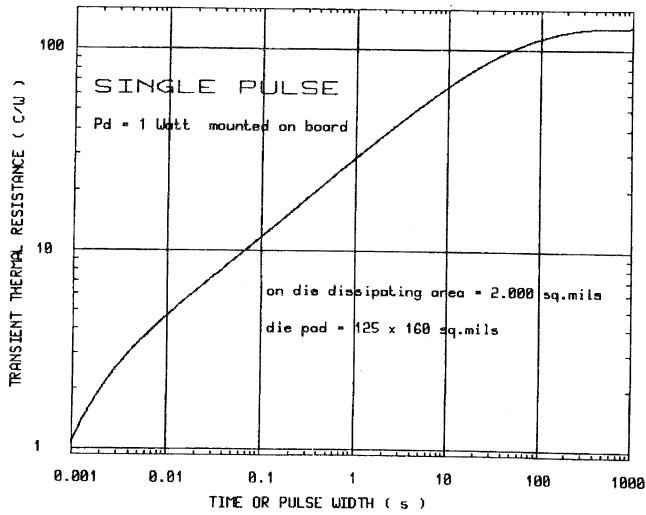


Figure 17 : Transient Thermal Impedance 0.4 mm Copper Frame DIP Packages.

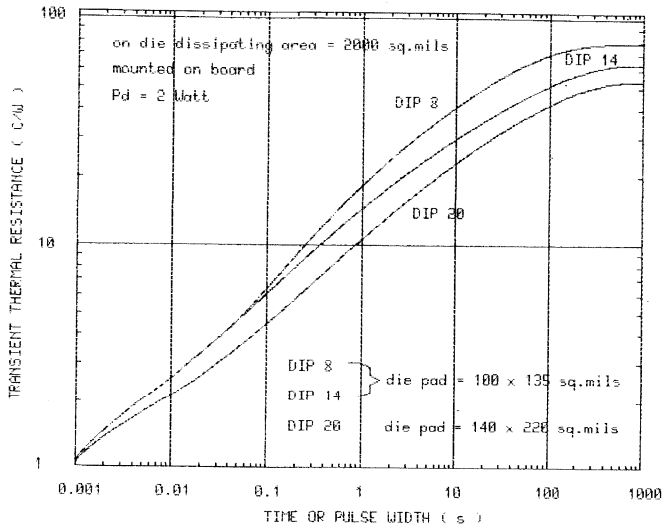


Figure 18 : Transient Thermal Impedance 0.25 mm Copper Frame DIP Packages.

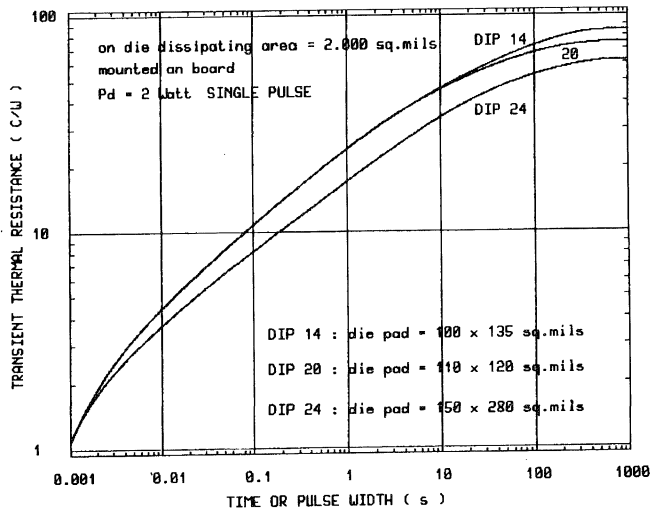


Figure 19 : Transient Thermal Impedance 0.25 mm Frame PLCC Package.

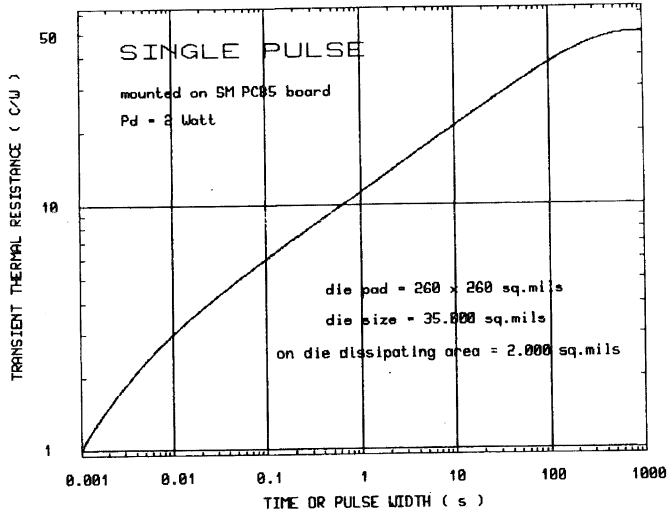


Figure 20 : Transient Thermal Impedance 0.25 mm Copper Frame SO14 Package.

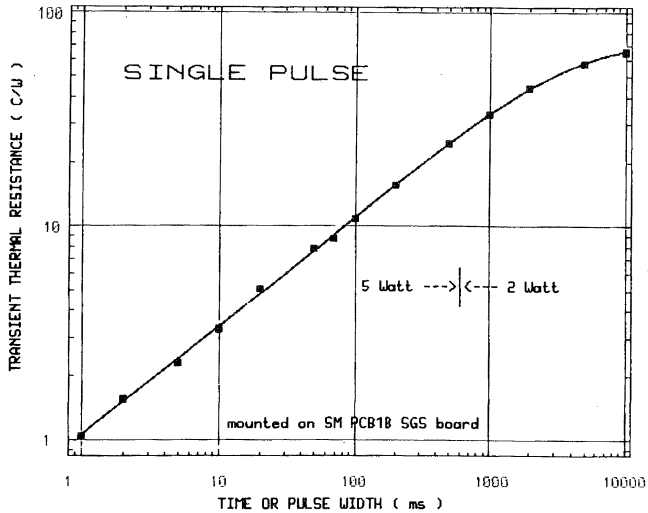
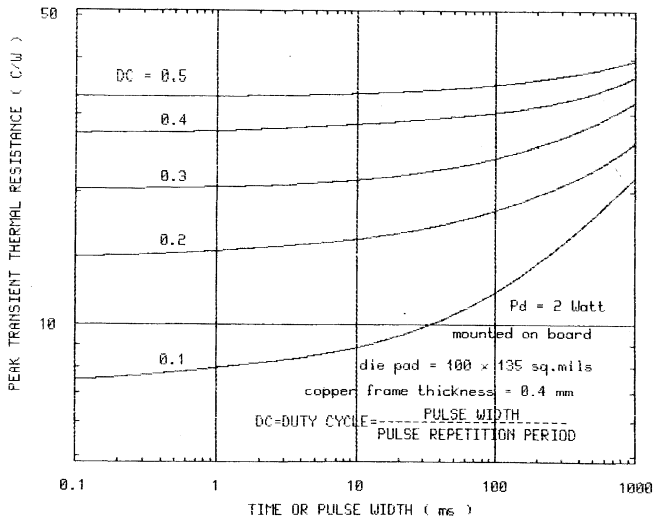


Figure 21 : Peak Thermal Impedance 0.25 mm Copper Frame 14 Lead DIP.



CONCLUSION

This paper has discussed a test procedure for measuring and quantifying the thermal characteristics of semiconductor packages. Using these test methods the thermal impedance of standard integrated circuit packages under pulsed and DC conditions were evaluated. From this evaluation two important considerations arise :

- 1) The true thermal impedance under repetitive pulsed conditions needs to be considered to maintain the peak junction temperature within the rating for the device. A proper evaluation will result in junction temperatures that do not exceed the specified limits under either steady state or pulsed conditions.
- 2) The proper evaluation of the transient thermal characteristics of an application should take into account the ability to dissipate high power pulses

allowing better thermal design and possibility reducing or eliminating expensive external heat sinks when they are oversized or useless.

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- (1) SEMI Draft Specifications 1377 and 1449, 1986
- (2) T. Hopkins, R. Tiziani, and C. Cognetti, "Improved thermal impedance measurements by means of a simple integrated structure", presented at SEMITHERM 1986
- (3) C. Cini, C. Diazzi, D. Rossi and S. Storti, "High side monolithic switch in Multipower-BCD technology", Proceedings of Microelectronics Conference, Munchen November 1986
- (4) Application Notes 106 through 110, SGS-THOMSON Microelectronics, 1987

THERMAL MANAGEMENT IN SURFACE MOUNTING

The evolutionary trends of integrated circuits and printed circuits boards are, in both cases, towards improved performance and reduced size. From these points of view, a factor of major importance has been mutual thermal interaction between ICs, even those with low dissipation.

It follows then that thermal design of medium and high density applications has evolved to include factors such as power effects, die size, package thermal resistance, **integration level of active devices** and substrate type. Added to this a trend towards greater use of switching techniques exists.

Today, in order to design reliable application circuits, it is necessary to have complete data on package thermal response characteristics. In fact, it is a well known and long established fact that device life-time has an exponential relationship with junction temperature.

PRELIMINARY CONSIDERATIONS

Heat dissipation for DIPs with a low thermal conductivity frame (e.g. Alloy42) is due to convection and **irradiation** from an emitting area corresponding to the silicon die and the package die pad.

Since heat transmission through the lead frame is very poor, dissipation does not depend greatly on substrate type. In fact, samples soldered on printed circuit boards, or inserted in **connectors** have nearly the same dissipation capability as samples suspended in air. The difference, in the range of just 10%, is commonly ignored and specifications for insertion ICs only give one thermal resistance value, which is more than adequate for good thermal design.

The question then arises, is the approximation valid for SO and PLCC packages ?

The answer is no ! Thermal characteristics for these devices are influenced by many factors.

1) Device Related Factors

- size of the dissipating element
- dissipation level
- pulse length and duty cycle

2) Package Related Factors

- thermal conductivity of the frame
- frame design

3) Substrate Related Factors

- thermal conductivity of the substrate
- layout

Therefore a number of parameters can change the thermal characteristics. These cannot be described by a single thermal resistance, in fact a set of experimental curves gives the best presentation.

JUNCTION TO AMBIENT THERMAL RESISTANCE $R_{th(j-a)}$

$R_{th(j-a)}$ represents the thermal resistance of the system and comprises the silicon die, the package, and any thermal mass in contact with the package to dissipate heat to the ambient.

At a given dissipation level P_d , the increase in junction temperature ΔT_j over ambient temperature T_a is given by :

$$\Delta T_j = R_{th(j-a)} \times P_d$$

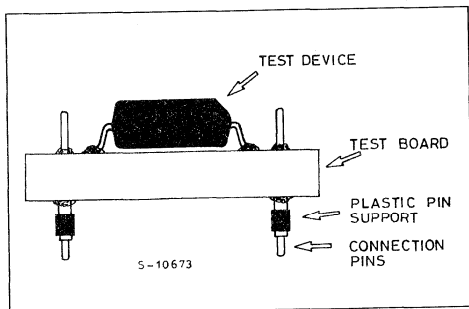
$R_{th(j-a)}$ is made up of many elements both within the device and external to it.

If the device is considered alone, $R_{th(j-a)}$ is given by the dissipation path from the silicon die to the lead-frame, to the molding compound, to the ambient.

Experimental values are very large in this condition, especially for small packages such as Small Outline types.

However, this situation is not met in practice and experimental data included in the present work indicates the worst case (floating samples). In most applications, Surface Mount Devices are soldered onto a substrate (commonly epoxy glass (FR4) and are in thermal contact with it through the soldered joints and the copper interconnections. In this case, the heat generated by the active circuit is transferred to the leadframe and then to the substrate. A new dissipation path thus exists in parallel with the previous one whose efficiency depends on the thermal conductivity of the frame and on the length of the printed circuit's copper tracks. Figure A shows the experimental module.

Figure A : Device Soldered to the Best Board, for Junction to Ambient Thermal Resistance Measurement.

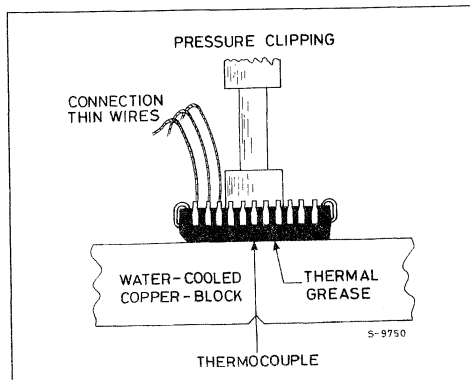


JUNCTION TO CASE THERMAL RESISTANCE $R_{th(j-c)}$

$R_{th(j-c)}$ is the thermal resistance from the junction to a given area of the package's external surface where a heatsink is applied.

In signal packages, a suitable area is its upper surface. **Measurements are made with the samples in good thermal contact with an infinite heatsink (fig. B).**

Figure B : Junction to Case Thermal Resistance Measurement.



When a heatsink of thermal resistance R_{hs} is attached to the package, the following relationship is valid :

$$R_{th(j-a)} = R_{th(j-c)} + \frac{R_{hs} \times R^*}{R_{hs} + R^*}$$

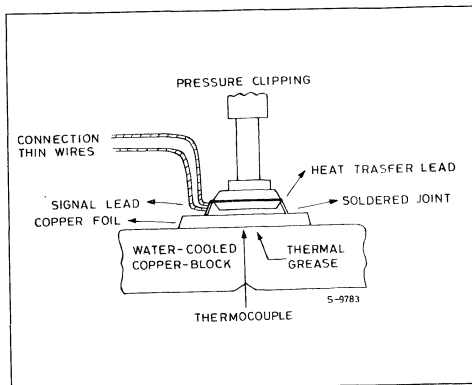
Where R^* takes into account all the other dissipation paths (i.e. junction/frame/substrate). R^* is the lowest with low thermal conductivity frames.

In high power applications $R^* = R_{hs}$ and $R_{th(j-a)} = R_{th(j-c)} + R_{hs}$

JUNCTION TO PIN THERMAL RESISTANCE $R_{th(j-p)}$

In medium power packages $R_{th(j-p)}$ is the thermal resistance of the heat transfer leads, from the junction to the external heatsink. In most cases the external heatsink is integrated on the board. Figure C shows the experimental setup.

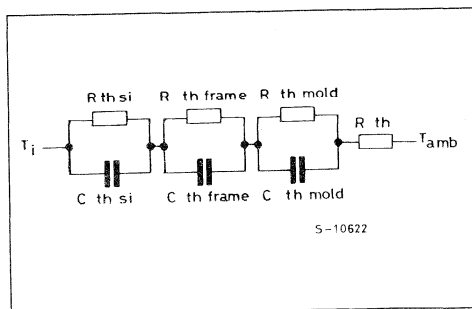
Figure C : Junction to Pin Thermal Resistance Measurement.



TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

The electrical equivalent of heat dissipation for a module formed by an active device, its package, a PCB and the ambient, is a chain of RC cells, as shown in fig. D, each with a characteristic rise time (τ) = RC.

Figure D : Equivalent Thermal Circuit Simplified Package.

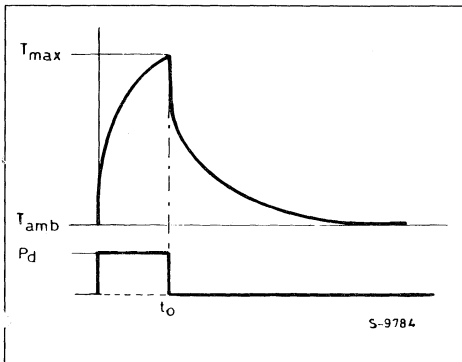


The thermal capacitance of each cell is a measure of its ability to accumulate heat and depends on the specific heat, volume and density of the constituent materials.

When power is switched on, the junction temperature after time it is governed by the heat impedance of the cells, each of which follows its own time constant - this is analogous to the exponential charge of RC cells in an electrical circuit.

For a pulse length t_o , the effective T_j can be significantly lower than the steady state T_j (fig. E) and the transient thermal resistance $R_{th(t_o)}$ can be defined from the ratio between the junction temperature at the end of the pulse and the dissipated power.

Figure E : Temperature Rise for Single Power Pulse.



Obviously, this parameter is smaller for shorter pulses and higher power can be dissipated without exceeding the maximum junction temperature defined from a reliability point of view.

The knowledge of transient thermal data is an important tool for cost effective thermal design of switching applications.

PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES

When pulses of the same height P_d are repeated with a duty cycle, DC, and a pulse width t_o , which is shorter than the overall system time constant, the train of pulses is seen as a continuous source of mean power P_{davg} , where :

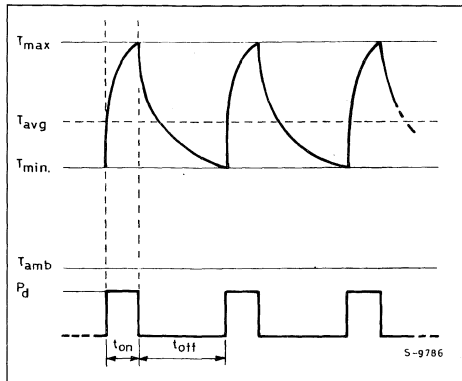
$$P_{davg} = P_d \times DC$$

However the silicon die has a time constant in the order of 1 to 2ms and is able to follow frequencies in the kHz range. Thus junction temperature oscillates about an average value given by :

$$T_{javg} = R_{th} \times P_{davg}$$

as is graphically shown in fig. F.

Figure F : Temperature Rise for Repeated Power Pulses.



The thermal resistance corresponding to the peak of the steady state oscillations (peak thermal resistance indicates the maximum temperature reached by the junction and, depending on duty cycle and pulse width, may be much lower than the DC thermal resistance).

EXPERIMENTAL METHOD

Measurements were performed by means of the especially developed thermal test pattern P432, which is designed according to the Semiconductor Equipment and Materials Institute (SEMI) G32 guideline. Test chip P432 is based on a dissipating element formed by two npn transistors, each with 10W power capability, and one sensing diode (fig. G). The diode is placed on the temperature plateau generated when the two transistors are biased in parallel, and gives the actual junction temperature T_j of the dissipating element, through the calibration curve (fig. H) of its forward voltage V_f versus temperature at a constant current of 100 μ A.

Figure G : Thermal Test Pattern P432.

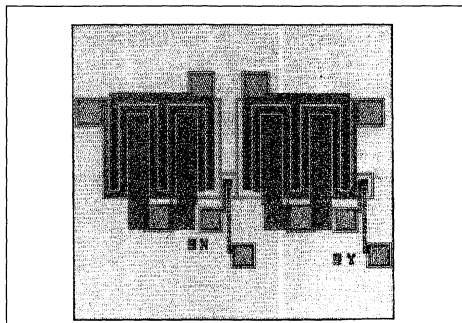
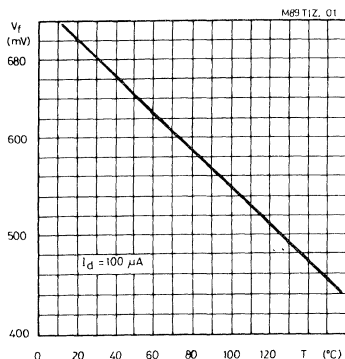


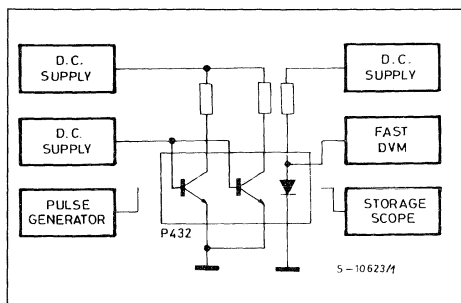
Figure H : Calibration Curve of P432 Temperature Sensing Diode.



Transistor size is intentionally limited to 1000sq. mils, in order to simulate high power density, characterizing a worst case. Die size, which is found to have little influence on thermal resistance when a copper frame is used, is slightly smaller than the die pad size and never exceeds 30k sq mils even in the largest packages such as high pin count PLCCs.

The measurement setup is shown in fig. I. it is compatible with DC and AC supplies and has an accuracy of better than 5%.

Figure I : Experimental Setup.



The advantages offered by the test pattern are :

- high power capability
- repeatable V_f and temperature coefficient (1.9mv/C) of the sensing element
- high resolution in pulsed conditions (100µs)
- better correlation from one package to another.

Both Alloy 42 and copper frames were considered for narrow SO packages (150mils body). For wide SO (300mils body) and PLCC packages only copper frames were examined. Suitable test boards were developed (figs J, K and L).

Figure J : Test Board Lay-out for SO Packages (150 mils body width)
Board size is : 23 x 42mm².

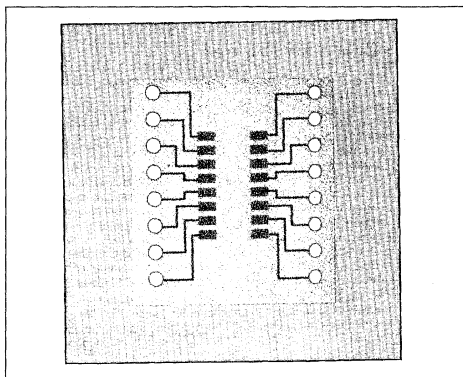


Figure K : Test Board Lay-out for SO Packages (3000 mils body width)
Board size is : 38 x 43mm².

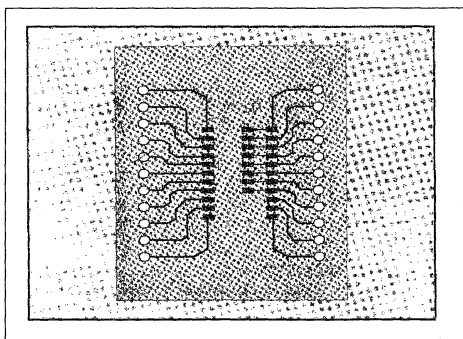
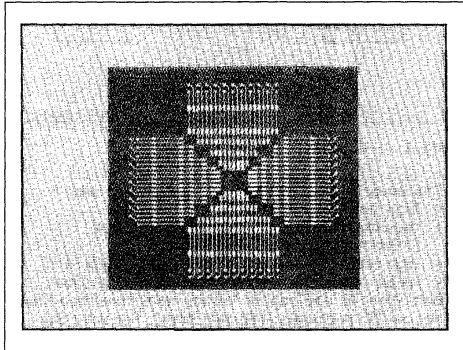


Figure K : Test Board for PLCCs
Board size is : 58 x 58mm².



MEDIUM POWER PACKAGES

While surface mount signal ICs are readily available, almost all power ICs are still assembled in traditional insertion packages.

Medium power SM packages ($P_d < 2W$) can readily be derived from existing small outline and chip carrier packages by modifying the leadframe - in much the same way that Powerdip packages were derived from standard Dips.

This approach is particularly attractive because the external dimensions of the package are identical to existing low power packages, allowing the use of standard automatic assembly and test equipment. Frame modification is aimed at obtaining a low junction to pin thermal resistance path for the transfer of heat to a suitable external heatsink. A number of leads are connected to the die pad for this purpose. Two possibilities are considered here : a medium power PLCC44 with 11 heat transfer leads (fig. M) and a medium power SO20 with 8 heat transfer leads (fig. N).

A cost effective heat spreader can be obtained on the board by means of suitably dimensioned copper areas. The heat transfer leads are soldered to there areas (fig. M1, N1).

Figure M : Lead Frame for Medium Power PLCC44.

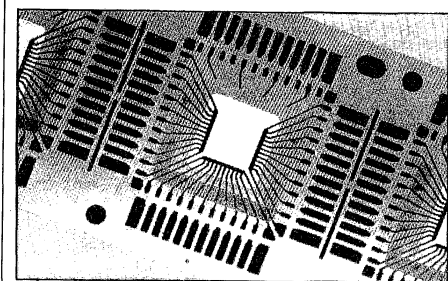


Figure N : Lead Frame for Medium Power SO20.

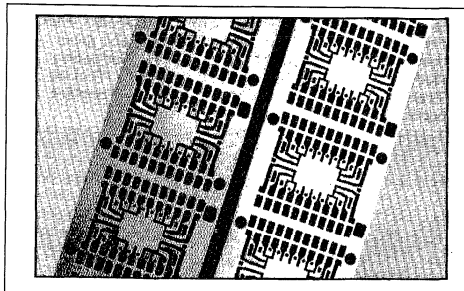


Figure M1 : Test Board for Medium Power PLCC44.

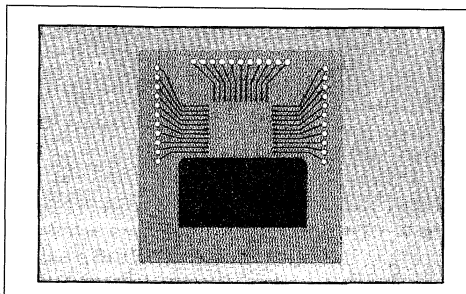
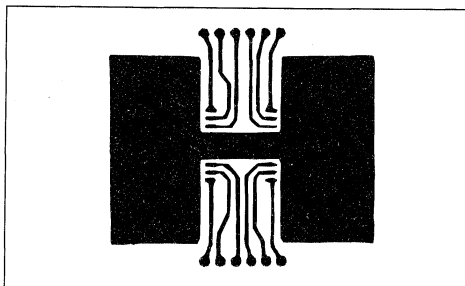


Figure N1 : Test Board for Medium Power SO20.



APPLICATION NOTE

THERMAL DATA OF SIGNAL PACKAGES

SUMMARY OF JUNCTION TO AMBIENT THERMAL RESISTANCE IN STEADY STATE POWER DISSIPATION (SGS-THOMSON test board)

	Die Size (millinches)	Power PD [W]	$R_{th(j-a)}$ [$^{\circ}\text{C/W}$] on Board
SO8 Alloy 42	90 x 100	0.2	250-310
	94 x 125	0.2	130-180
SO14 Alloy 42	98 x 100	0.3	200-240
	78 x 118	0.5	120-160
	98 x 125	0.7	105-145
SO16 Alloy 42	98 x 118	0.3	180-215
	94 x 185	0.5	95-135
SO16W Copper	120 x 160	0.7	90-112
SO20 Copper	140 x 220	0.7	77-97
PLCC-20 Cu	180 x 180	0.7	90-110
PLCC-44 Cu	260 x 260	1.5	50-60
PLCC-68 Cu	425 x 425	1.5	40-46
PLCC-84 Cu	450 x 450	2.0	36-41

$R_{th(j-a)}$ values correspond to low and high board density

SUMMARY OF JUNCTION TO CASE THERMAL RESISTANCE

	Die Pad Size (millinches)	$R_{th(j-a)}$ [$^{\circ}\text{C/W}$]
PLCC20	140 x 140	25
PLCC44	260 x 260	13
PLCC68	425 x 425	10
PLCC84	450 x 450	9

JUNCTION TO AMBIENT THERMAL RESISTANCE IN STEADY STATE POWER DISSIPATION

Figure 1 : SO8.

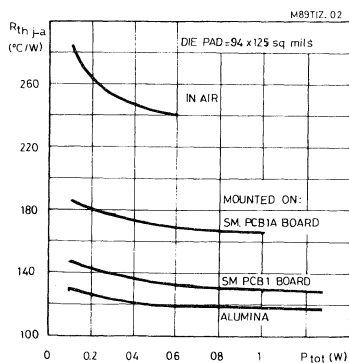


Figure 2 : SO14.

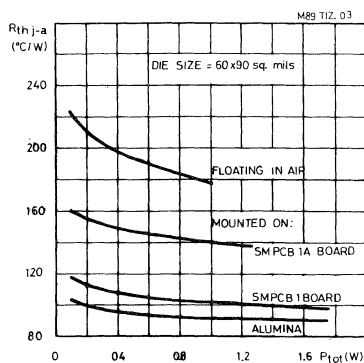


Figure 3 : SO16.

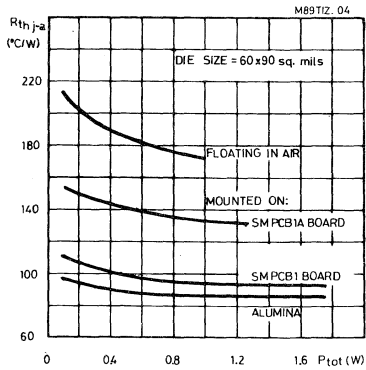


Figure 5 : PLCC20.

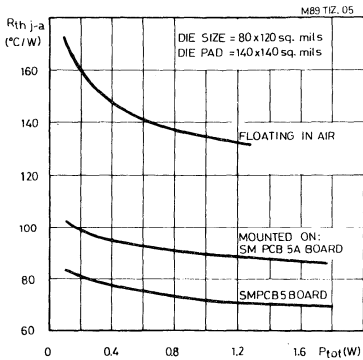


Figure 7 : PLCC68.

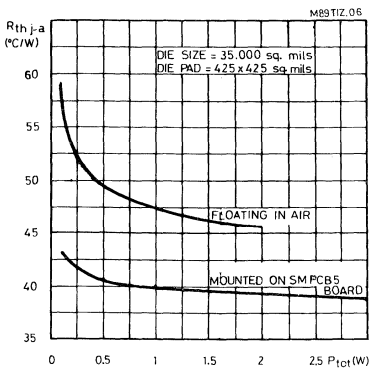


Figure 4 : SO20.

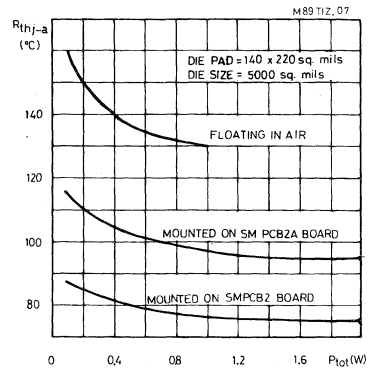


Figure 6 : PLCC44.

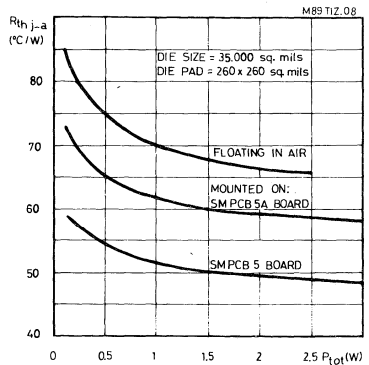
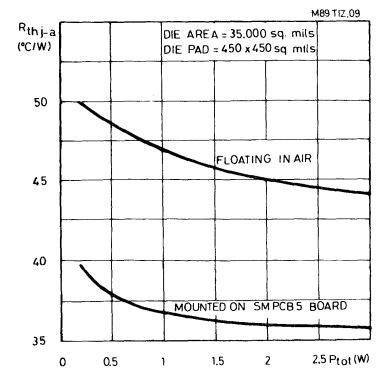


Figure 8 : PLCC84.



JUNCTION TO AMBIENT THERMAL RESISTANCE VS BOARD LAY-OUT (area of copper tracks on the board)

Figure 9 : SO16.

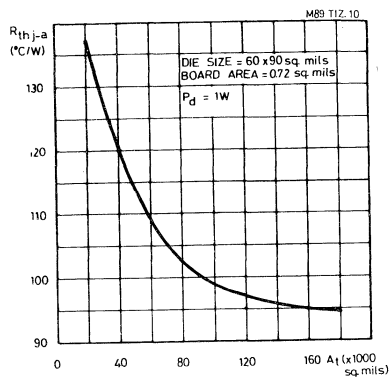


Figure 11 : PLCC44.

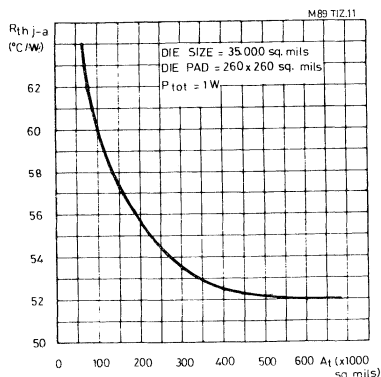


Figure 10 : SO20.

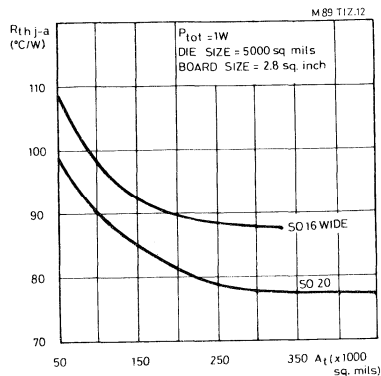
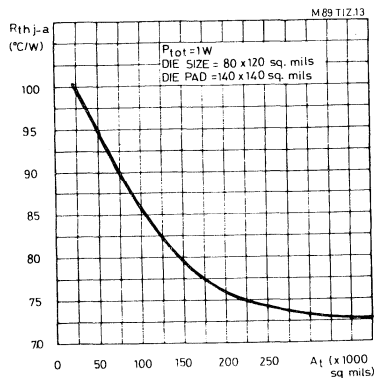


Figure 12 : PLCC20.



TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

Figure 13 : SO8.

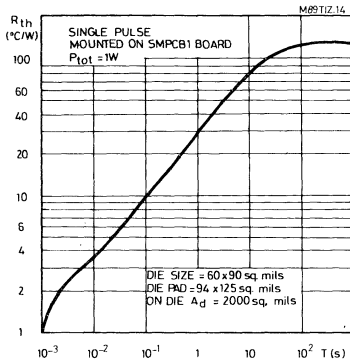


Figure 14 : SO14, 16.

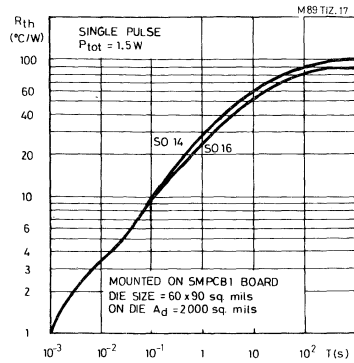


Figure 15 : SO20.

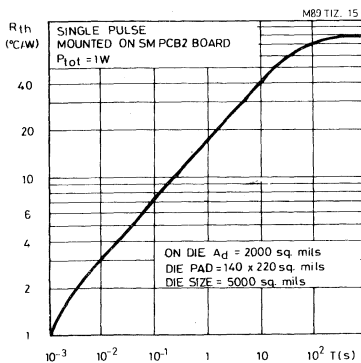


Figure 16 : PLCC44.

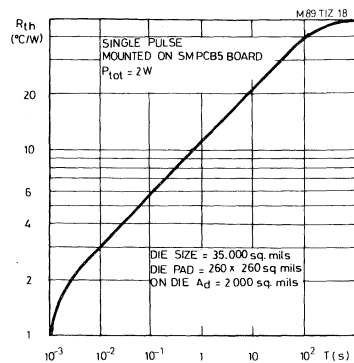


Figure 17 : PLCC68.

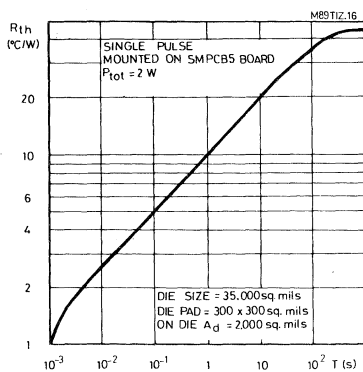
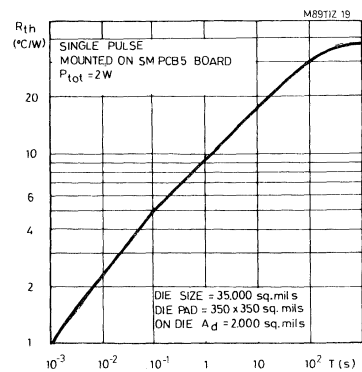


Figure 18 : PLCC84.



PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES

Figure 19 : SO14.

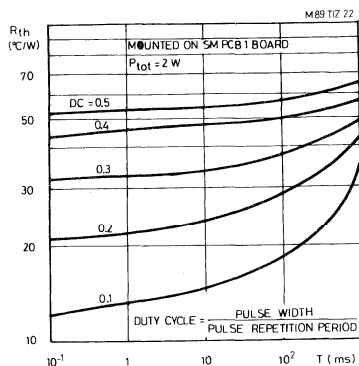


Figure 20 : SO20.

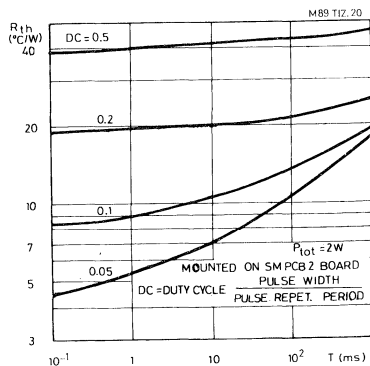


Figure 21 : PLCC44.

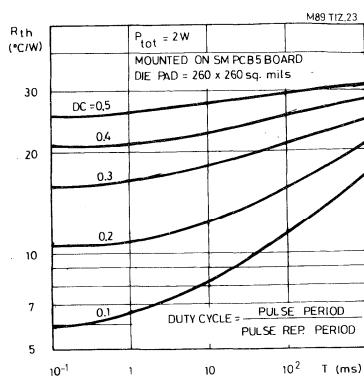


Figure 22 : PLCC68.

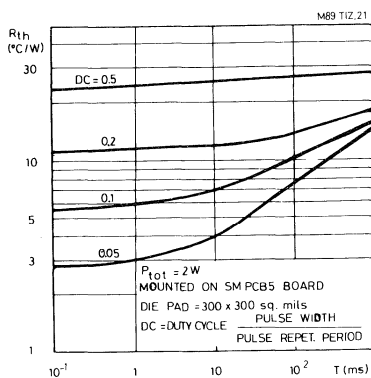
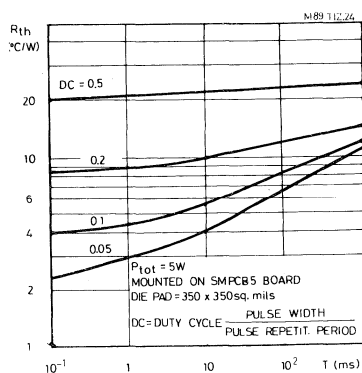


Figure 23 : PLCC84.



THERMAL DATA OF MEDIUM POWER PACKAGES

	$R_{th(j-p)}$ [$^{\circ}\text{C}/\text{W}$] (AVERAGE)	$R_{th(j-a)^*}$ [$^{\circ}\text{C}/\text{W}$]
SO (12 + 4 + 4)	14	50
PLCC (33 + 11)	12	41

* with 6 sq. cm. on board heat-sink.

JUNCTION TO PINS THERMAL RESISTANCE VS ON DIE DISSIPATING AREA

Figure 24 : SO (12 + 4 + 4).

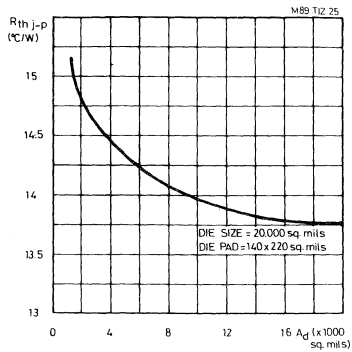
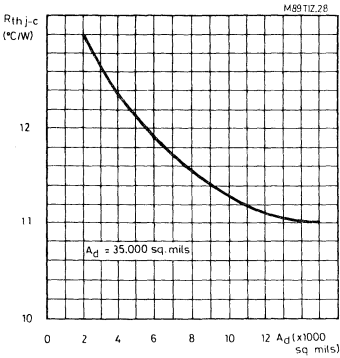


Figure 25 : PLCC (33 + 11).



JUNCTION TO AMBIENT THERMAL RESISTANCE VS AREA ON BOARD HEAT-SINK

Figure 26 : SO (12 + 4 + 4).

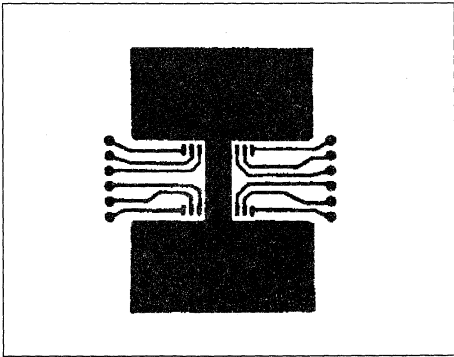
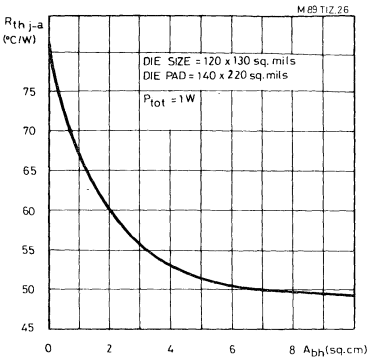
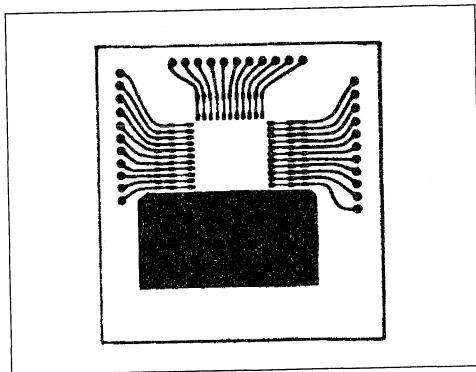
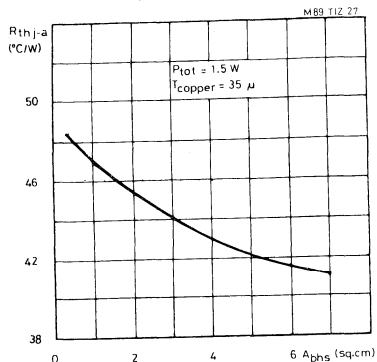


Figure 27 : PLCC (33 + 11).



TRANSIENT THERMAL RESISTANCE FOR SINGLE PULSES

Figure 28 : SO (12 + 4 + 4).

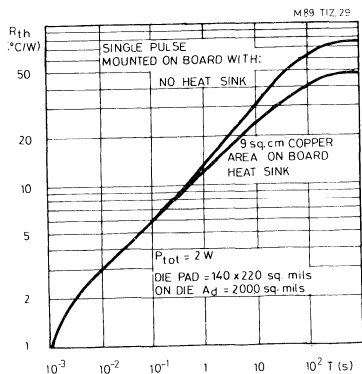
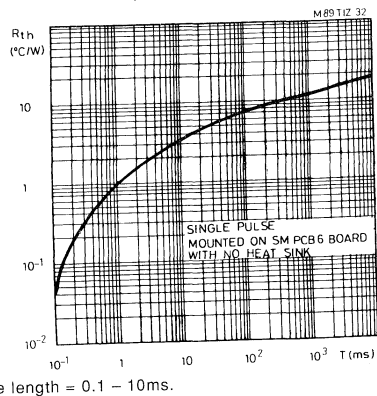
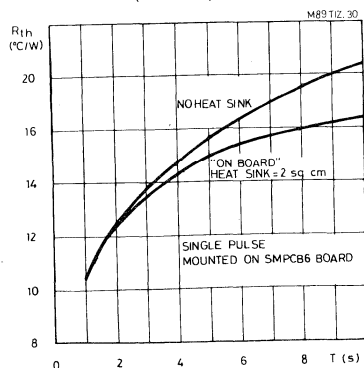


Figure 29 : PLCC (33 + 11).



pulse length = 0.1 – 10ms.

Figure 30 : PLCC (33 + 11).



pulse length = 1 – 10s.

PEAK TRANSIENT THERMAL RESISTANCE FOR REPEATED PULSES.

Figure 31 : PLCC (12 + 4 + 4).

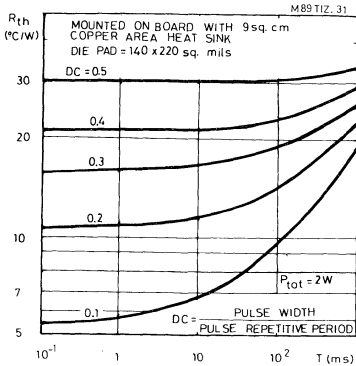
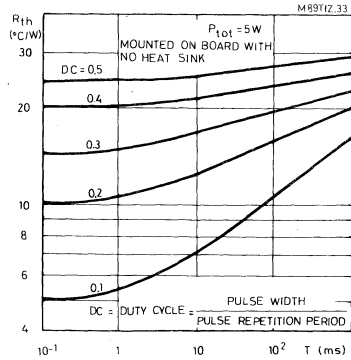


Figure 32 : PLCC (33 + 11).



APPLICATION EXAMPLES OF THERMAL DATA

Good thermal design begins with system and reliability considerations. This turn is based on correct consideration of ambient and device temperature parameters.

The ambient temperature T_a defined for applications can range from 50 to 55°C, as is common in many consumer and computer applications, through to 80°C or more in applications such as automotive systems. The ambient temperature depends on the various heat and cooling sources surrounding the device. An important factor in device lifetime is junction temperature - lifetime is approximately halved when junction temperature T_j is increased by 10°C. The maximum junction temperature commensurate with

good reliability, takes into account the activation energy of the failure mechanisms which may differ for various silicon and packaging technologies.

In plastic packages the maximum T_{jmax} is 150°C, but lower values (100 to 120°C) may be specified in high rel applications such as telecoms.

When T_{jmax} and T_a are known, their difference ΔT_j indicates the permissible junction temperature rise for a given device. For a given power dissipation P_d , the thermal design must ensure that the product $P_d \times R_{th(j-a)}$ is lower than ΔT_j ; where $R_{th(j-a)}$ is the thermal resistance of the device from the junction to the ambient at temperature T_a . This takes into consideration the many elements connected to the heat source and includes the leadframe, moulding compound, substrate and heatsink, if used.

EXAMPLE 1 : Maximum dissipation for SO16 packaged device soldered onto an FR4 board (1 oz copper) under the following conditions :

- Ambient temperature : $T_a = 70^\circ\text{C}$
- Maximum Junction Temperature : $T_{jmax} = 130^\circ\text{C}$

The average length of the 12mils wide copper line connected to each pin is 80mils, soldering pads are 30 x 40mils. The total area is thus :

$$A = [(80 \times 12) + 1200 \times 16] = 34560 \text{ sq.mils}$$

SOLUTION

From fig. 13, the value for $R_{th(j-a)}$ is 125°C/W for a copper frame package. Comparing figs. 5 and 6, a value of about 240°C/W can be assumed for Alloy 42 packages. The allowed rise in junction temperature is : $\Delta T_{jmax} = 130 - 70 = 60^\circ\text{C}$

Maximum dissipation is given by $\Delta T_{jmax}/R_{th(j-a)}$.

Therefore :

$$60/125 = 0.48W \text{ for Copper frame}$$

$$60/240 = 0.25 \text{ for Alloy 42 frame}$$

EXAMPLE 2 : Junction temperature for an SO20 packaged device soldered on FR4, under the following conditions :

- Ambient temperature $T_a = 70^\circ\text{C}$
- Dissipated Power $P_d = 0.6\text{W}$

SOLUTION

A total trace-area of 200k sq.mils is assumed, this then gives, from fig. 14 :

- Thermal Resistance $R_{th(j-a)} = 90^\circ\text{C/W}$
- $\Delta T_j = P_d \times R_{th(j-a)}$
- $\Delta T_j = 0.6 \times 90 = 54^\circ\text{C}$
- Junction Temperature $T_j = 54 + 70 = 124^\circ\text{C}$

EXAMPLE 3 : To determine the size of an integrated heatsink for a medium power application using a PLCC (33 + 11) under the following conditions :

- Ambient temperature $T_a = 50^\circ\text{C}$
- Max. Junction Temperature $T_{jmax} = 150^\circ\text{C}$
- Dissipated Power $P_d = 2.2\text{W}$

SOLUTION

By calculation the application needs an $R_{th(j-a)}$ of : $(150 - 50)/2.2 = 45.5^\circ\text{C/W}$

From figure 32 the on board heatspreader can thus be defined as needing an area of about 2 sq.cm.

EXAMPLE 4 : Given the application described in example 3 determine the maximum pulse width for a single 4W pulse superimposed on a continuous 1.5W dissipation

SOLUTION

The continuous steady state junction temperature at 1.5W dissipation is :

$$T_{jss} = (1.5 \times 45.5) + 50 = 118.25^\circ\text{C}$$

The single pulse is allowed to cause a maximum increase of $(150 - 118.25^\circ\text{C}) = 31.75^\circ\text{C}$.

The related transient thermal resistance is $(31.75/4) = 7.9^\circ\text{C/W}$

From figure 33, the corresponding pulse width can be interpreted as being in the order of 200ms.

EXAMPLE 5 : In a medium power application using an SO (12 + 4 + 4) calculate the average junction temperature and the peak temperature for repeated pulses under the following conditions :

- Ambient temperature $T_a = 70^\circ\text{C}$
- On board heatsink area $A = 9\text{ sq.cm.}$
- Pulse length = 100ms
- Pulse height = 5W
- Duty cycle = 20%

SOLUTION

From figure 31, the thermal resistance is found to be 49°C/W . Thus the average junction temperature can be calculated :

$$T_{javg} = (5 \times 49 \times 0.2) + 70 = 119^\circ\text{C}$$

From figure 36, the peak thermal resistance is given as around 15°C/W . The peak temperature can thus be calculated as :

$$T_p = (5 \times 15) + 70 = 145^\circ\text{C}$$

THERMAL CHARACTERISTICS OF THE MULTIWATT PACKAGE

By R. TIZIANI

INTRODUCTION

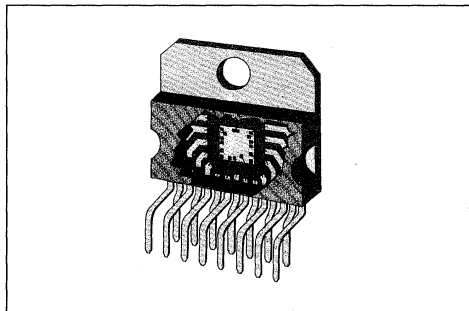
This Application Note provides a complete thermal characterization of the Multiwatt® package (multi-lead double TO-220 - fig. 1).

Characterization is performed according with recommendations included in the G32-86 SEMI guideline, by means of a dedicated test pattern. It refers to :

1. Junction to case thermal resistance $R_{th(j-c)}$
2. Junction to ambient thermal resistance $R_{th(j-a)}$
3. Junction to ambient thermal impedance for single pulses and repated pulses, with different pulse width and duty cycle ;
4. Thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of switching techniques.

Figure 1 : Multiwatt Assembly.



EXPERIMENTAL CONDITIONS

The thermal evaluation was performed by means of the test pattern P432, which is a 20K mils² die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 2K mils² with

a power capability of 20W. Measurement method is described in Appendix A.

Samples with the indicated characteristics were prepared :

Package Multiwatt 15 leads

Frame Material	Copper
Slug Thickness	1.5mm
Slug Thermal Conductivity	3.9W/cm°C
Die Attach	Soft (PbSn)

Measurement of junction to case thermal resistance $R_{th(j-c)}$ is performed by holding the package against a water cooled heat sink, according with fig. 2. A thermocouple placed in contact with the slug measures the reference temperature of the case.

For junction to ambient thermal resistance $R_{th(j-a)}$ the samples are suspended horizontally in a one cubic foot box, to prevent drafts.

Both DC and pulsed conditions are used ; in the second case the contribution of package thermal capacitance is effective and transient thermal resistances much lower than the steady state $R_{th(j-a)}$ can be found, according to pulse length and duty cycle.

The effect of the external heat sink is quantified, using as test vehicle the commercially available heat sink THM7023 especially developed by Thermalloy for the Multiwatt package, whose thermal resistance in still air is about 9°C/W.

The measurement circuit shown in fig. A3 was used for all the thermal evaluations.

JUNCTION TO CASE THERMAL RESISTANCE

The dependance of $R_{th(j-c)}$ on the dissipated power is reported in fig. 3.

It is well known that the main contribution to $R_{th(j-c)}$ of power packages is given by the silicon die.

Figure 2 : Measurement of $R_{th(j-c)}$.

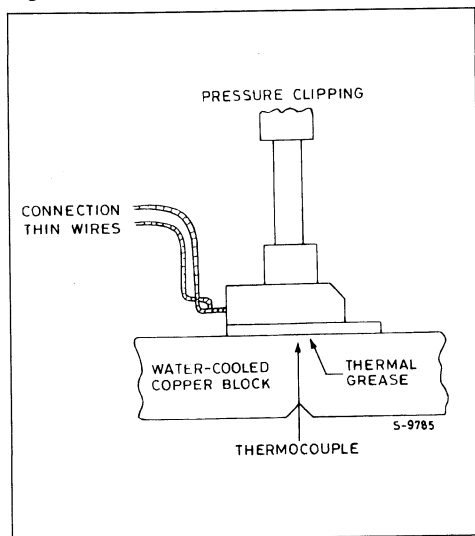
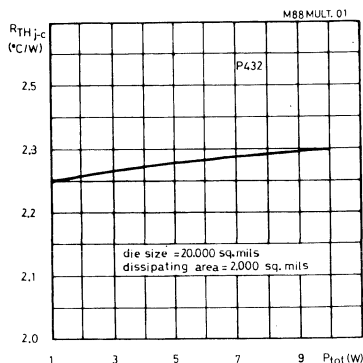


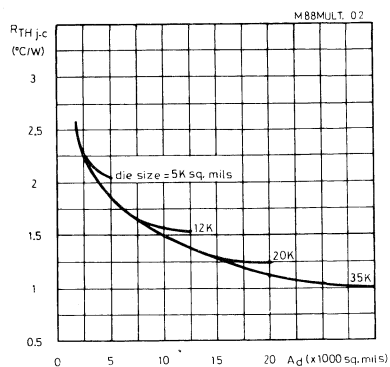
Figure 3 : $R_{th(j-c)}$ of Multiwatt Package vs. Power Level.



FOR DEVICES OTHER THAN THE TEST PATTERN P432 THE CALIBRATION CURVE OF FIG. 4 IS NEEDED.

It shows the relationship between $R_{th(j-c)}$ and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

Figure 4 : $R_{th(j-c)}$ Thermal Resistance vs. Die Size and on Die dissipating Area.



JUNCTION TO AMBIENT THERMAL RESISTANCE

In medium power applications (1.5-2W), the Multiwatt package can be used without external heat sink, thanks to the significant size (about 3.5cm²) of its integrated thermal mass.

Its $R_{th(j-a)}$ has two contributions : the $R_{th(j-c)}$, mainly due to the silicon die (as shown in fig. 4) and the thermal resistance of the copper slug $R_{th(slug)}$.

Figure 5 : $R_{th(j-a)}$ of Multiwatt Package vs. dissipated Power.

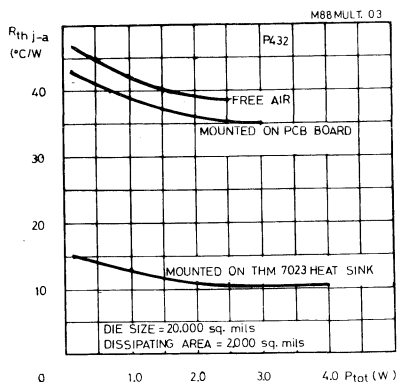


Fig. 5 gives the relationship between $R_{th(j-a)}$ and the power dissipation level for the P432 test pattern is still air, on PC board and on a commercial heat sink. IN ORDER TO HAVE AN ACCURATE VALUE FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 5 SHOULD BE CORRECTED THROUGH THE CALIBRATION CURVE OF FIG. 4 CORRECTION TERM IS ALWAYS IN THE RANGE OF 0.2°C/W ; THEREFORE, IT AFFECTS THE $R_{th(j-a)}$ OF NO MORE THAN 5% IN STILL AIR OR WITH THE PACKAGE MOUNTED ON PC BOARD.

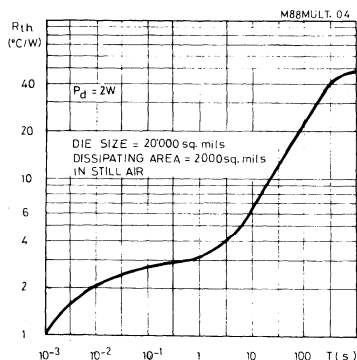
TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (without external heat sink)

The effect of single pulses of different length and height for the Multiwatt package without any external heat sink is shown in fig. 6.

This behaviour is discussed in Appendix B. Due to a significant thermal capacitance ($C = 2J/^{\circ}C$) and correspondingly long risetime ($\tau = 80s$), single pulses up to 30W can be delivered to the Multiwatt package for 1s with acceptable junction temperature increase.

IN ORDER TO HAVE ACCURATE R_{th} (to FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 7 MUST BE CORRECTED AS DESCRIBED IN EXAMPLE 2 OF THE LAST SECTION.

Figure 6 : Transient Thermal Resistance for Single Pulse.



Repetition of pulses with defined P_d , period and duty cycle DC (ratio between pulse length and signal period), gives rise to oscillations in junction temperature as described in Appendix B.

The transient thermal resistance corresponding to the upper limit of the curve of fig. B4 (peak transient thermal resistance) is reported in fig. 7 and depends on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (with external heat sink)

Characterization has been repeated with a commercial heat sink (Thermalloy THM7023) in order to have an example of the effect of an external thermal mass on the impedance of the thermal module.

Relationship between transient R_{th} and pulse length is reported in fig. 8.

The effect of the increased thermal capacitance is evident in fig. 9, where thermal data of fig. 6 and 8 are compared : it can be noticed that the curves are definitely different for pulses longer than 1s, corresponding about to the rise time of the slug. The effect of the thermal mass is to keep low the heating rate of the silicon die thus allowing a better power management of long power pulses. This conclusion has general validity and can be applied to other heat sinks than the one considered in this note.

Figure 7 : Peak Transient R_{th} vs. Pulse width and Duty Cycle.

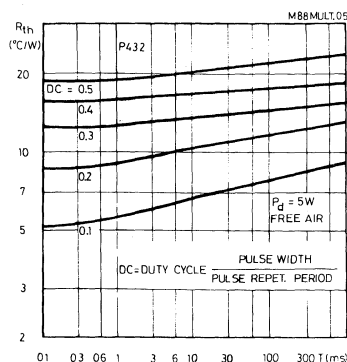
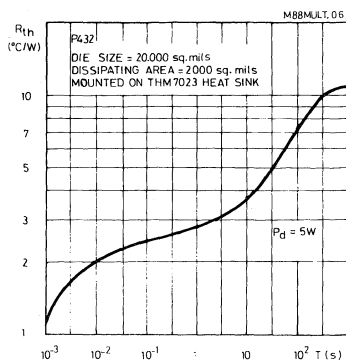


Figure 8 : Transient R_{th} for single pulses, with Heatsink.



APPENDIX A

The thermal resistance evaluation is performed with the especially designed test chip P432 which has two bipolar power transistor and one sensing diode (fig. A1). The active area is about 2000 mils² on a 35000mils² chip. Its lay-out was optimized in order to have a uniform temperature area, once the two transistor are powered ; the sensing diode is placed at the center of this area.

Figure A1 : Test Pattern P432 Lay-out.

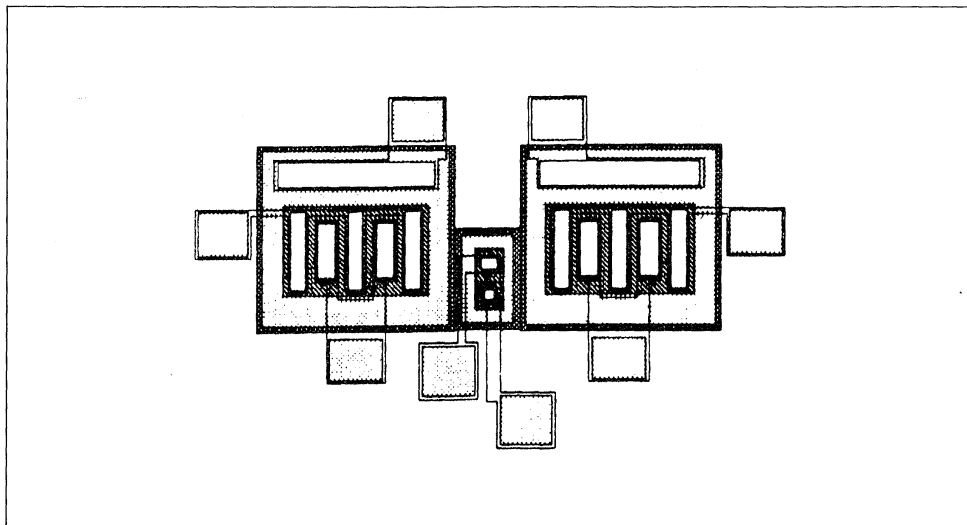
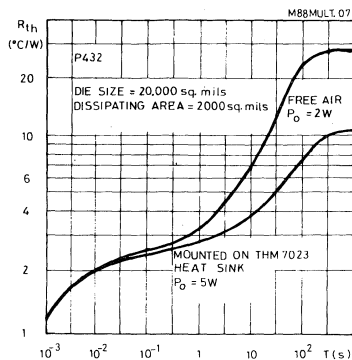


Figure 9 : Comparison of Transient R_{th} for single pulses, with and without Heat Sink.



The relationship between the forward voltage V_f of the diode at the constant current of $100\mu\text{A}$ and the temperature is shown in fig. A2. The curve calibrates the junction temperature through the voltage drop of the diode.

The measurement circuit is shown in fig. A3. A storage oscilloscope or a fast digital voltmeter can be used for recording the V_f value.

Figure A2 : Calibration Curve (sensing diode).

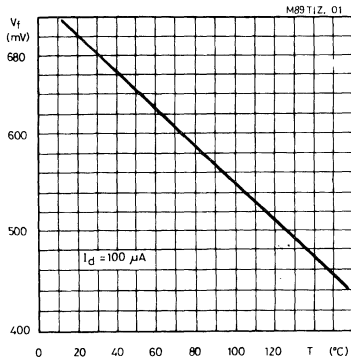
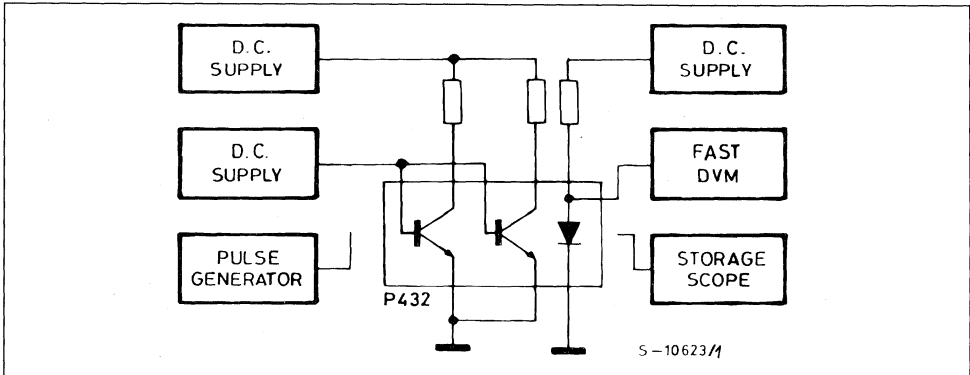


Figure A3 : Measurement Circuits.



APPENDIX B - THERMAL MANAGEMENT IN PULSED CONDITION

THERMAL RESISTANCE AND CAPACITANCE

The electrical equivalent of heat dissipation, for a thermal module formed by the active device with its package and the external heat sink is shown in fig. B1.

To each cell of the thermal chain are associated a value of thermal resistance R_{th} (°C/W) and a value of thermal capacitance C_{th} (J/°C). The former informs about temperature increase due to the element represented by the cell ; as, in the example under consideration, heat transfer is mainly based on conduction for the silicon, the copper integrated heat sink and to metallic body of the external heat sink R_{th} can be calculated from the relationship :

$$R_{th} = \frac{\gamma}{K \times S}$$

where K is the thermal conductivity of the material, the length of the conductive path and S its section.

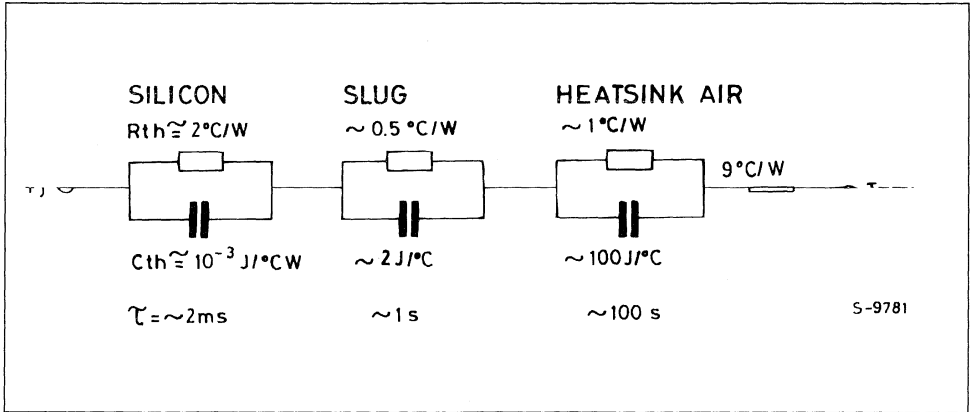
Thermal capacitance C_{th} is the capability of heat accumulation ; it depends on the specific heat of the material and on the volume effectively interested by heat exchange (this means that the parts which are not heated during heat dissipation DO NOT contribute to thermal capacitance). Thermal capacitance is given by :

$$C_{th} = d \times c_t \times V$$

where d is the density of the material, c_t its specific heat and V the volume interested to heat accumulation.

The last element of the network, assumed as purely resistive, is due to convection and radiation from the external heat sink towards the ambient.

Figure B1 : Electrical Equivalent of Multiwatt Package Mounted on the External Heatsink.



Each cell has its own risetime τ , given by the product of the thermal resistance and capacitance :

$$\tau = R_{th} \times C_{th}$$

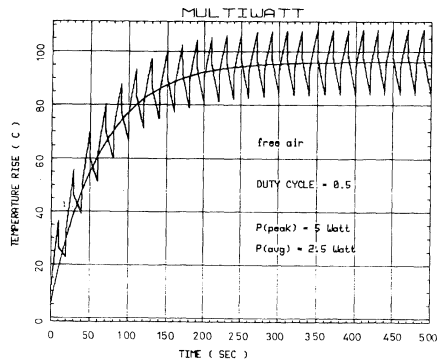
The value of the time constant determines whether a cell approaches equilibrium rapidly or slowly : if R_{th} or C_{th} increases, equilibrium is reached at a slower rate. The following relationship is valid for each cell :

$$\Delta T = R_{th} \times P_d [1 - e^{-t/\tau}] \quad (1)$$

Typical values of R_{th} , C_{th} and τ for Multiwatt application are shown in fig. B1.

When power is switched on, temperature increase is ruled by subsequent charging of thermal capacitances while the value reached in the steady state depends on thermal resistances only. Qualitative behaviour of the network of fig. B1 is shown in fig. B2.

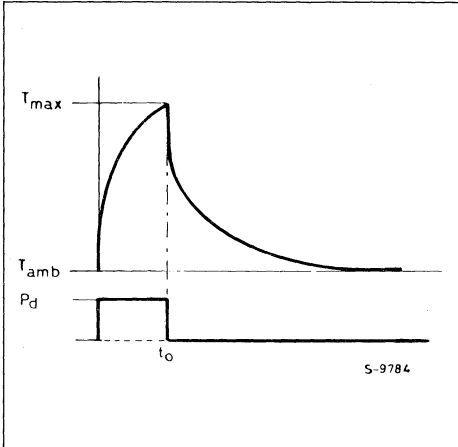
Figure B2 : Qualitative T_j increase (network of fig. B1) for repeated Power Pulse.



SINGLE POWER PULSE

When the pulse length has an assigned value, effective T_j can be significantly lower than the steady state T_j (fig. B3.).

Figure B3 : Effect of a Single Power Pulse.



For any pulse length t_0 , a transient thermal resistance $R_{th}(t_0)$ is defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power. Obviously, for shorted pulses, $R_{th}(t_0)$ is lower and a higher power can be dissipated, without exceeding the maximum junction temperature $T_{j,max}$ allowed to the IC from reliability considerations. Fig. 7 and 9 of this Application Note give experimental values of $R_{th}(t_0)$ for the two cases of the Multiwatt package without and with external heat sink.

REPEATED PULSES

When pulses of the same height P_d are repeated with a defined duty cycle DC and pulse length is short in comparison with the total risetime of the system (many tens of seconds) the train of pulses is seen by the system as a continuous source, at a mean power level of

$$P_{davg} = P_d \times DC$$

The average temperature increase is :

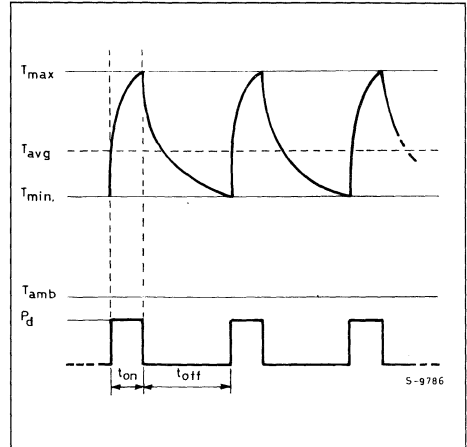
$$\Delta T_{avg} = R_{th} \times P_{davg} = R_{th} \times P_d \times DC$$

On the other hand, the silicon die ($\tau_s = 1-3ms$) is able to follow frequencies of some KHz and junction temperature oscillates about the average as qualitatively shown in fig. B4.

The thermal resistance corresponding to the peak of the oscillation at equilibrium (peak thermal resis-

tance $R_{th(peak)}$) is now given by fig. 5, and can be obtained if pulse length and duty cycle are known ; P_{dmax} is derived from the same figure.

Figure B4 : Junction Temperature increase for repeated Pulses.



APPLICATION EXAMPLES

EXAMPLE 1 - MAXIMUM P_d FOR SINGLE PULSE OF ASSIGNED LENGTH

PROBLEM : define the maximum P_d for a single pulse with a length of 20ms in the case of Multiwatt package used without heat sink. Ambient temperature is $50^\circ C$; maximum temperature is $130^\circ C$. Die size is $20K \text{ mils}^2$, with dissipating area of $2K \text{ mils}^2$ (as in P432 test pattern).

SOLUTION : allowed temperature increase ΔT is $80^\circ C$. Having a $R_{th(j-a)}$ of $39^\circ C/W$, Multiwatt package can dissipate about 2W in steady state. From fig. 7 the transient thermal resistance corresponding to one single pulse of 20ms is $R_{th}(20ms)_{P432} = 2.2^\circ C/W$. A peak of $80/2.2 = 36.3W$ can be applied to the circuit.

EXAMPLE 2 - CORRECTION FOR DIE SIZE AND DISSIPATING AREA

PROBLEM : correct the results obtained in example 1, for assigned die size and dissipating area. Practical case : IC having a die size of $35K \text{ mils}^2$ with a dissipating area of $20k \text{ mils}^2$.

SOLUTION : from fig. 5, thermal resistances of P432 and of the IC under consideration are $R_{th P432} = 2.3^\circ C/W$ and $R_{th(j-c)IC} = 1.2^\circ C/W$.

As the length of the pulse is 10-15 times longer than the rise time of the silicon, the die (first cell of fig. B1) can be assumed to have reached its equilibrium condition.

R_{th} (20ms) found in previous example has to be corrected in order to take into account the new value of $R_{th(j-c)}$:

$$\begin{aligned} R_{th} (20ms)_{IC} &= R_{th} (20ms)_{P432} - \\ &- R_{th(j-c)} P_{432} + R_{th(j-c)}_{IC} = \\ &= 2.2 - 2.3 + 1.2^{\circ}C/W = 1.1^{\circ}C/W \end{aligned}$$

A single pulse of $80/1.1 \cong 72W$ can be delivered to such device.

When the pulse has the same order of silicon rise time τ P432 is about 1ms) another type of correction is needed. In first approximation, τ increase with dissipating area with the relationship :

$$t_{IC} = \sqrt{20K_{IC}/2KP_{432} \times \tau P_{432}} \cong 3.1ms$$

Expansion of the exponential term of relationship (1) limited to the first term term, is :

$$R_{th IC} (t_o) \cong R_{th P432} (t_o) / 3.1$$

for $t_o = 1ms$:

$$R_{th IC} (1ms) = 1.05/3.1^{\circ}C/W \cong 0.34^{\circ}C/W$$

A single pulse of $80/0.34 \cong 235W$ can be delivered to such device.

EXAMPLE 3 – R_{th} WITH REPEATED PULSES

PROBLEM : find the peak power which can be dissipated by Multiwatt package without heatsink, when power is continuously switched on 10ms and switched off 90ms. Ambient temperature is $50^{\circ}C$, maximum temperature is allowed to be $125^{\circ}C$.

SOLUTION : a maximum $\Delta T = 75^{\circ}C$ has to be considered. Fig. 5 indicated that for a pulse width of 10ms and a duty cycle of 0.1, $R_{th peak}$ is $6.7^{\circ}C/W$. Maximum P_d is $75/6.7 = 11.2W$, with an average temperature increase ΔT_{peak} of $39 \times 0.1 \times 11.2 \cong 43^{\circ}C$.

THERMAL CHARACTERISTICS OF THE PENTAWATT-HEPTAWATT PACKAGES

By R. TIZIANI

INTRODUCTION

This Application Note is aimed to give a complete thermal characterization of the Heptawatt and Pentawatt package (fig. 1, 2).

Characterization is performed according with recommendations included in the G32-86 SEMI guideline, by means of a dedicated test pattern. It refers to :

1. Junction to case thermal resistance $R_{th(j-c)}$
2. Junction to ambient thermal resistance $R_{th(j-a)}$
3. Junction to ambient thermal impedance for single pulses and repeated pulses, with different pulse width and duty cycle ;
4. thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of switching techniques.

Figure 1 : Pentawatt.

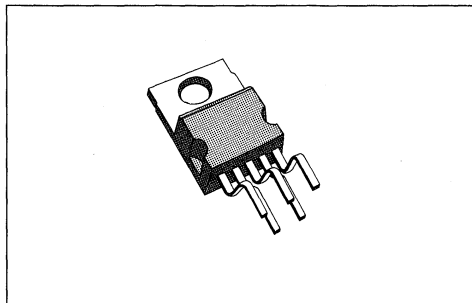
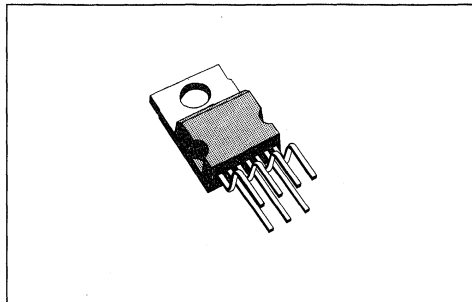


Figure 2 : Heptawatt.



EXPERIMENTAL CONDITIONS

The thermal evaluation was performed by means of the test pattern P432, which is a 15k mils² die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 2k mils² with a power capability of 20W. Measurement method is described in Appendix A.

Samples with the indicated characteristics were prepared :

Package	Pentawatt - Heptawatt
Frame Material	Copper
Slug Thickness	1.25mm Typ.
Slug Thermal Conductivity	3.9W/cm°C
Die Attach	Soft (PbSn)

Measurement of junction to case thermal resistance $R_{th(j-c)}$ is performed by holding the package against a water cooled heat sink, according with fig. 3. A thermocouple placed in contact with the slug measures the reference temperature of the case.

For junction to ambient thermal resistance $R_{th(j-a)}$ the samples are suspended horizontally in a one cubic foot box, to prevent drafts.

Both DC and pulsed conditions are used ; in the second case the contribution of package thermal capacitance is effective and transient thermal resistances much lower than the steady state $R_{th(j-a)}$ can be found, according with pulse length and duty cycle.

The effect of the external heat sink is quantified, using as test vehicle the commercially available heat sink THM7023 (Thermalloy) whose thermal resistance in still air is about 9°C/W.

The measurement circuit shown in fig. A3 was used for all of the thermal evaluations.

JUNCTION TO CASE THERMAL RESISTANCE

The dependance of $R_{th(j-c)}$ on the dissipated power is reported in fig. 4. The absolute value and the behaviour with the dissipated power are the same for

both packages as the slug thickness and the die - attach are equal.

Figure 3 : Measurement of $R_{th(j-c)}$.

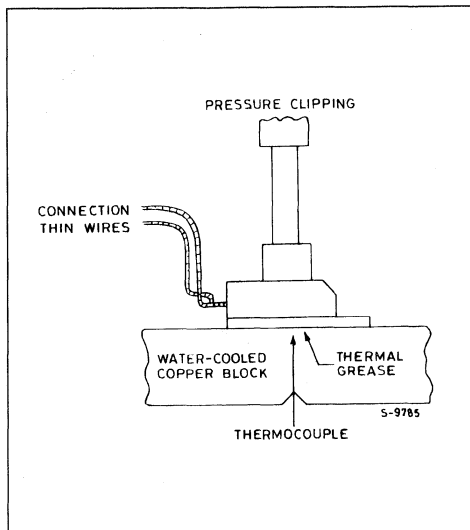
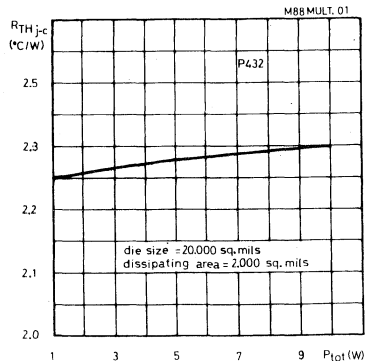


Figure 4 : $R_{th(j-c)}$ of Pentawatt and Heptawatt Package vs. Power Level.

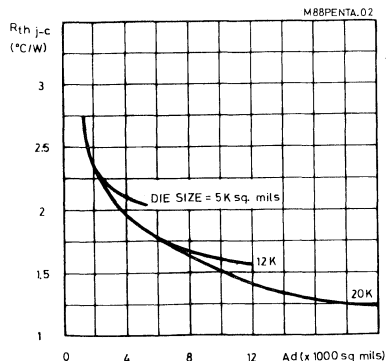


It is well known that the main contribution to $R_{th(j-c)}$ of power packages is given by the silicon die.

FOR OTHER DEVICES THAN THE TEST PATTERN P432 THE CALIBRATION CURVE OF FIG. 5 IS NEEDED.

It shows the relationship between $R_{th(j-c)}$ and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

Figure 5 : $R_{th(j-c)}$ Thermal Resistance vs. Die Size and on Die dissipating Area.



JUNCTION TO AMBIENT THERMAL RESISTANCE

In medium power application (1W), the Pentawatt and Heptawatt packages can be used without external heat sink thanks to the significant size (about $1.5cm^2$) of its integrated thermal mass.

An effective cost solution for higher power application (1.5-2.0W) is using a copper area heat sink.

An board with the external leads bent down as shown in fig. 7.

Fig. 6 gives the relationship between $R_{th(j-a)}$ and the power dissipation level for the P432 test pattern in still air, on PC board, on integrated heat sink on board and on a commercial heat sink.

IN ORDER TO HAVE AN ACCURATE VALUE FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 6 SHOULD BE CORRECTED THROUGH THE CALIBRATION CURVE OF FIG. 5. CORRECTION TERM IS ALWAYS IN THE RANGE OF $0-2^{\circ}C/W$; THEREFORE, IT AFFECTS THE $R_{th(j-a)}$ OF NO MORE THAN 5% IN STILL AIR OR WITH THE PACKAGE MOUNTED IN PC BOARD.

Figure 6 : $R_{th(j-a)}$ vs. dissipated Power (heptawatt).

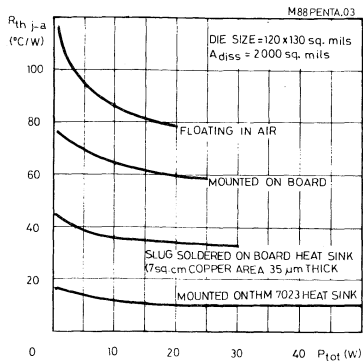
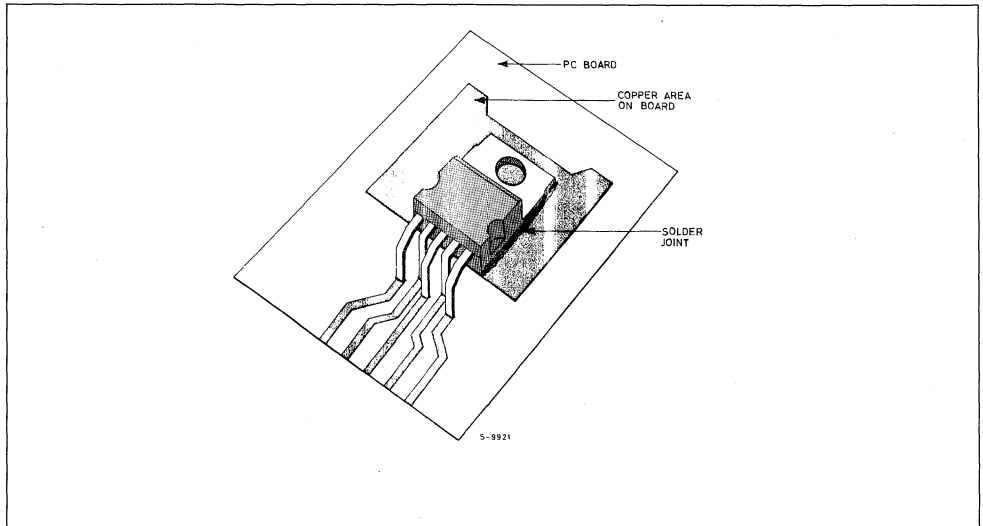


Figure 7 : Pentawatt Soldered on Copper Heatsink on P.C Board.

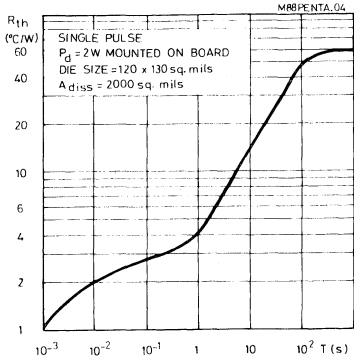


TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (without external heat sink)

The effect of single pulses of different length and height without any external heat sink is shown in fig. 8.

This behaviour is discussed in Appendix B. Due to a significant thermal capacitance ($C = 1J/^{\circ}C$) and a correspondingly long risetime ($\tau = 80s$), single pulses up to 20W can be delivered for 1 s with acceptable junction temperature increase.

Figure 8 : Transient Thermal Resistance for Single Pulses (heptawatt).



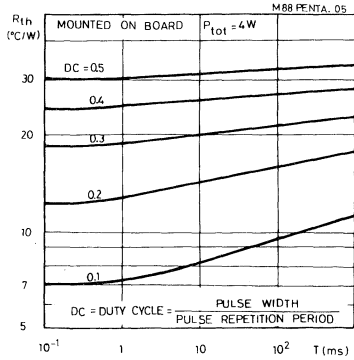
IN ORDER TO HAVE ACCURATE $R_{th}(t_0)$ FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 7 MUST BE CORRECTED AS DESCRIBED IN EXAMPLE 2 OF THE LAST SECTION.

Repetition of pulses with defined Pd, period and duty cycle DC (ratio between pulse length and signal period), gives rise to oscillations in junction temperature as described in Appendix B.

The transient thermal resistance corresponding to the upper limit of the curve of fig. B4 (peak transient thermal resistance) is reported in fig. 9 and depends

on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

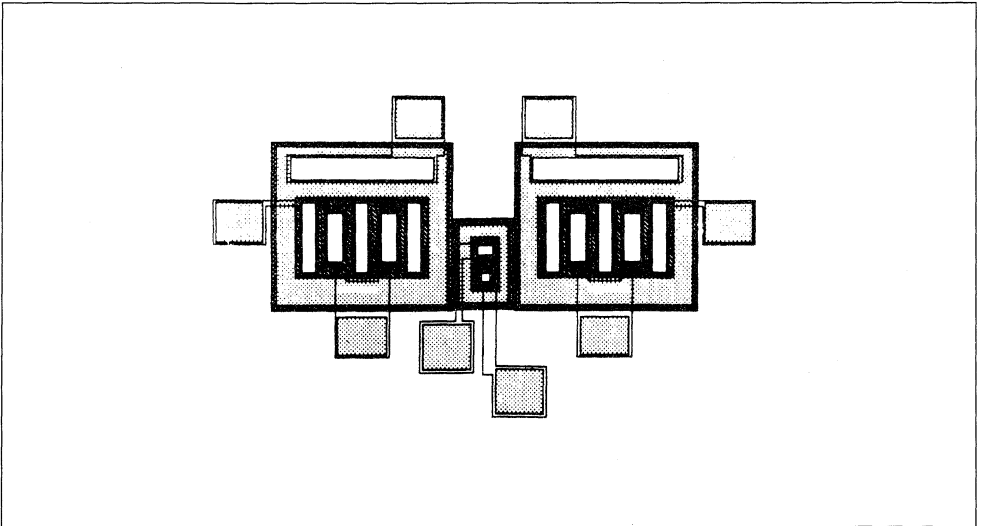
Figure 9 : Peak Transient R_{th} vs Pulse width and Duty Cycle (heptawatt).



APPENDIX A

The thermal resistance evaluation is performed with the especially designed test chip P432 which has two bipolar power transistor and one sending diode (fig. A1). The active area is about 2000 mils² on a 15000 mils² chip. Its lay-out was optimized in order to have a uniform temperature area, once the two transistor are powered ; the sensing diode is placed at the center of this area.

Figure A1 : Test Pattern P432 Lay-out.



The relationship between the forward voltage V_f of the diode at a constant current of $100\mu\text{A}$ and the temperature is shown in fig. A2. The curve calibrates the junction temperature through the voltage drop of the diode.

The measurement circuit is shown in fig. A3. A storage oscilloscope or a fast digital voltmeter can be used for recording the V_f value.

Figure A2 : Calibration Curve (sensing diode).

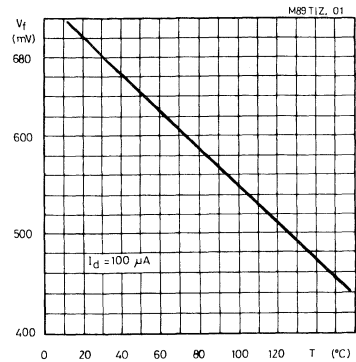
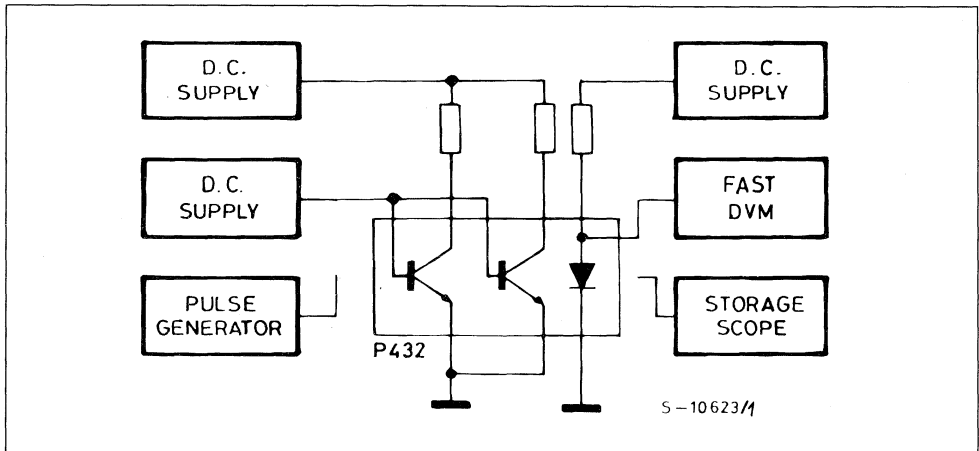


Figure A3 : Measurement Circuit.



APPENDIX B - THERMAL MANAGEMENT IN PULSED CONDITION

THERMAL RESISTANCE AND CAPACITANCE

The electrical equivalent of heat dissipation, for a thermal module formed by the active device with its package and the external heat sink is shown in fig. B1.

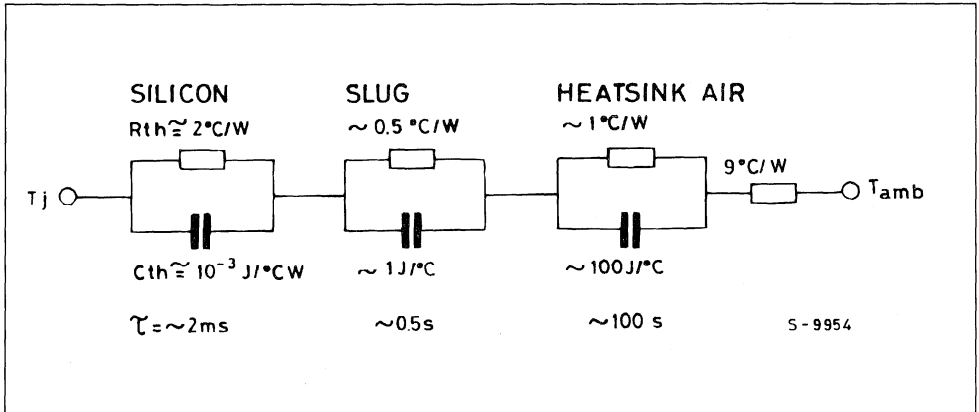
To each cell of the thermal chain are associated a value of thermal resistance R_{th} (C/W) and a value of thermal capacitance C_{th} (J/°C). The former in-

forms about temperature increase due to the element represented by the cell ; as, in the example under consideration, heat transfer is mainly based on conduction for the silicon, the copper integrated heat sink and to metallic body of the external heat sink R_{th} can be calculated from the relationship :

$$R_{th} = \frac{1}{K \times S}$$

Where K is the thermal conductivity of the material, l the length of the conductive path and S its section.

Figure B1 : Electrical Equivalent of Pentawatt and Heptawatt Package mounted on the External Heatsink.



Thermal capacitance C_{th} is the capability of heat accumulation ; it depends on the specific heat of the material and on the volume effectively interested by heat exchange (this means that the parts which are not heated during heat dissipation DO NOT contribute to thermal capacitance). Thermal capacitance is given by :

$$C_{th} = d \times c_t \times V$$

where d is the density of the material, c_t its specific heat and V the volume interested to heat accumulation.

The last element of the network, assumed as purely resistive, is due to convection and radiation from the external heat sink towards the ambient.

Each cell has its own risetime τ , given by the product of thermal resistance and capacitance :

$$\tau = R_{th} \times C_{th}$$

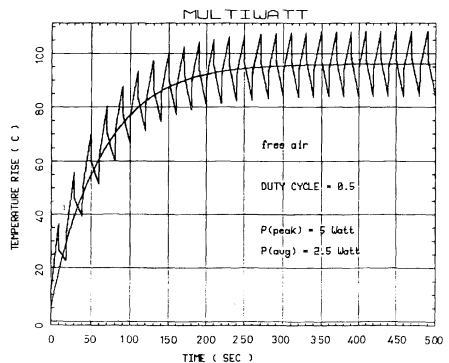
The value of the time constant determines whether a cell approaches equilibrium rapidly or slowly : if R_{th} or C_{th} increases, equilibrium is reached at a slower rate. The following relationship is valid for each cell :

$$\Delta T = R_{th} \times P_d \times [1 - e^{-t/\tau}] \quad (1)$$

Typical values of R_{th} , C_{th} and τ for Heptawatt and Pentawatt application are shown in fig. B1.

When power is switched on, temperature increase is ruled by subsequent charging of thermal capacitance while the value reached in the steady state depends on thermal resistance only. Qualitative behaviour of the network of fig. B1 is shown in fig. B2.

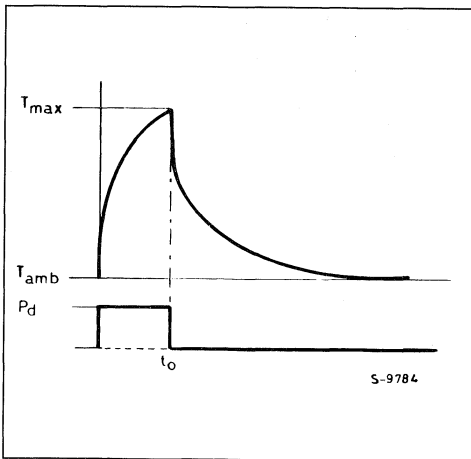
Figure B2 : Qualitative T_j increase (network of fig. B1) for repeated power pulse (heptawatt).



SINGLE POWER PULSE

When the pulse length has an assigned value, effective T_j can be significantly lower than steady state T_j (fig. B3.).

Figure B3 : Effect of a Single Power Pulse.



For any pulse length t_0 , a transient thermal resistance $R_{th}(t_0)$ is defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power. Obviously, for shorter pulses, $R_{th}(t_0)$ is lower and a higher power can be dissipated, without exceeding the maximum junction temperature T_{jmax} allowed to the IC from reliability considerations. Fig. 7 and 9 of this Application Note give experimental values of $R_{th}(t_0)$ for the two cases of the Heptawatt package without and with external heat sink.

REPEATED PULSES

When pulses of the same height P_d are repeated with a defined duty cycle DC and pulse length is short in comparison with the total risetime of the system (many tens of seconds) the train of pulses is seen by the system as a continuous source, at a mean power level of

$$P_{davg} = P_d \times DC$$

The average temperature increase is :

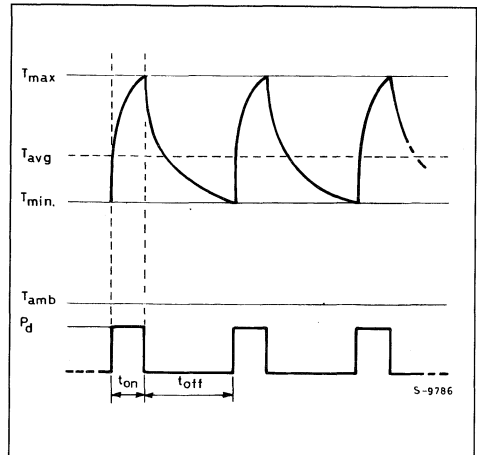
$$\Delta T_{avg} = R_{th} \times P_{davg} = R_{th} \times P_d \times DC$$

On the other hand, the silicon die ($\tau_{SI} = 1 \div 2ms$) is able to follow frequencies of some kHz and junction temperature oscillates about the average, as qualitatively shown in fig. B4.

The thermal resistance corresponding to the peak of the oscillation at equilibrium (peak thermal resistance $R_{th(peak)}$) is now given by fig. 5, and can be ob-

tained if pulse length and duty cycle are known ; P_{dmax} is derived from the same figure.

Figure B4 : Junction Temperature increase for operated Pulses.



APPLICATION EXAMPLES

EXAMPLE 1 - MAXIMUM P_d FOR SINGLE PULSE OF ASSIGNED LENGTH

PROBLEM : define the maximum P_d for a single pulse with a length of 20ms in the case of Heptawatt package used without heat sink. Ambient temperature is 50°C ; maximum temperature is 130°C. Die size is 15k mils², with dissipating area of 2k mils² (as in P432 test pattern).

SOLUTION : allowed temperature increase ΔT is 80°C. Having a $R_{th(j-a)}$ of 60°C/W, Heptawatt package can dissipate about 1.3W in steady state. From fig. 8 the transient thermal resistance corresponding to one single pulse of 20ms is $R_{th}(20ms)_{P432} = 2.2^\circ C/W$. A peak of $80/2.2 = 36.3W$ can be applied to the circuit.

EXAMPLE 2 - CORRECTION FOR DIE SIZE AND DISSIPATING AREA

PROBLEM : correct the results obtained in example 1, for assigned die size and dissipating area.

Practical case : IC having a die size of 15k mils² with a dissipating area of 10k mils².

SOLUTION : from fig. 5, thermal resistance of P432 and of the IC under consideration are $R_{th P432} = 2.3^\circ C/W$ and $R_{th(j-c)IC} = 1.5^\circ C/W$.

As the length of the pulse is 10-15 times longer than the risetime of the silicon, the die (first cell of fig. B1)

can be assumed to have reached its equilibrium condition.

R_{th} (20ms) found in previous example has to be corrected in order to take into account the new value of $R_{th(j-c)}$.

$$\begin{aligned} R_{th} (20ms)_{IC} &= R_{th} (20ms)_{P432} - \\ &\quad - R_{th(j-c)} P_{432} + R_{th(j-c)}_{IC} = \\ &= 2.2 - 2.3 + 1.5^{\circ}\text{C/W} = 1.4^{\circ}\text{C/W} \end{aligned}$$

A single pulse of $80/1.4 \equiv 57\text{W}$ can be delivered to such a device.

EXAMPLE 3 - CORRECTION FOR SINGLE PULSES OF 1–3ms

PROBLEM : Correct the results of example 2, for pulse length of 1ms.

SOLUTION : when the pulse has the same order of magnitude of silicon rise time (τ_{P432} is about 1ms) another type of correction is needed. In first approximation it is considered that remains constant when the dissipating area gets higher and the R_{th} for the silicon die decreases as the reciprocal of the dissipating area. From relationship (1) :

$$\Delta T = R_{th} (1ms)_{P432} \times 2K/10K \times P_d \times [1 - e^{-t/\tau}] \text{ for } t_0 = 1ms :$$

$$R_{thIC} (1ms) = 1.05/0.5^{\circ}\text{C/W} \equiv 0.21^{\circ}\text{C/W}$$

A single pulse of $80/0.21 \equiv 380\text{W}$ can be delivered to such a device.

EXAMPLE 4 - R_{th} REPEATED PULSES

PROBLEM : find the peak power which can be dissipated by Heptawatt package without heatsink, when power is continuously switched on 10ms and switched off 90ms. Ambient temperature is 50°C . maximum temperature is allowed to be 125°C .

SOLUTION : a maximum $\Delta T = 75^{\circ}\text{C}$ has to be considered. Fig. 9 indicated that for a pulse width of 10ms and a duty cycle of 0.1, $R_{th_{peak}}$ is 8.5°C/W . Maximum P_d is $75/8.5 = 8.8\text{W}$, with an average temperature increase ΔT_{peak} of $60 \times 0.1 \times 8.8 \equiv 68^{\circ}\text{C}$.

REFERENCES

"Improved thermal evaluation, by means of a simple integrated structure" T. Hopkins, C. Cognetti, R. Tiziani - SEMI THERM (USA, 1986).

THERMAL CHARACTERISTICS OF THE POWER DIP (12+3+3) PACKAGE

By R. Tiziani

INTRODUCTION

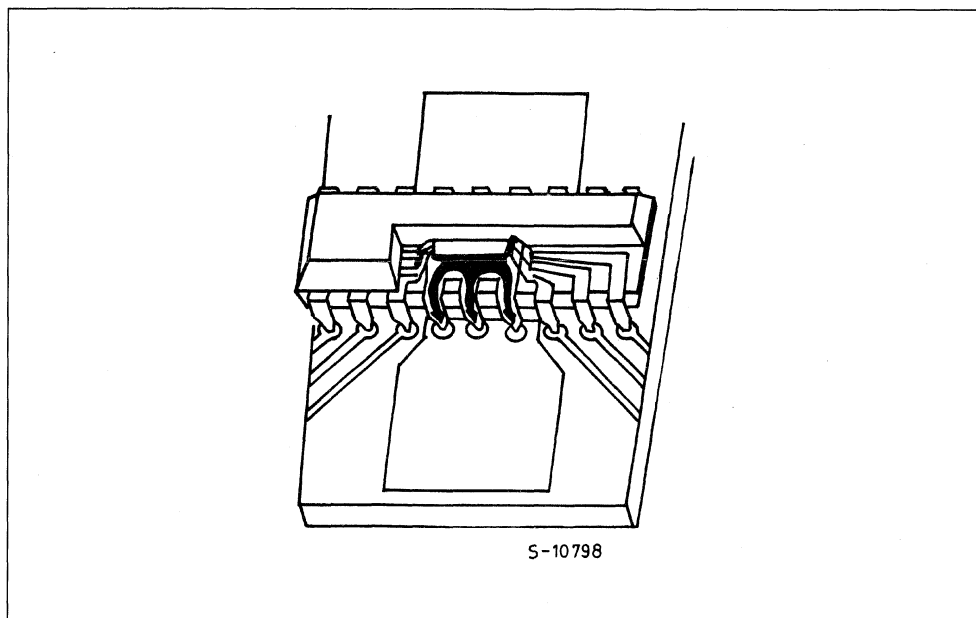
This Application Note provides a complete thermal characterization of the (12+3+3) power DIP (modified 18 lead DIP with 6 heat transfer leads) in association with thermal modules integrated on the PCB.

Characterization is performed according with recommendations included in the G32-86 SEMI guideline, by means of a dedicated test pattern developed by SGS-THOMSON Microelectronics. It refer to :

1. Junction to pin thermal resistance $R_{th(j-p)}$
2. Junction to ambient thermal resistance $R_{th(j-a)}$
3. Thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of the switching techniques.

Figure 1 : DIP 12+3+3 Application.



EXPERIMENTAL CONDITIONS

The thermal evaluation was performed by means of the test pattern P432, which is a 30K mils² die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 2K mils² with a power capability of 20W. Measurement method is described in Appendix A.

Samples with the indicated characteristics were prepared :

Package	DIP (12+3+3)
Frame Material	Copper
Slug Thickness	0.4mm
Slug Thermal Conductivity	3.9W/cm°C

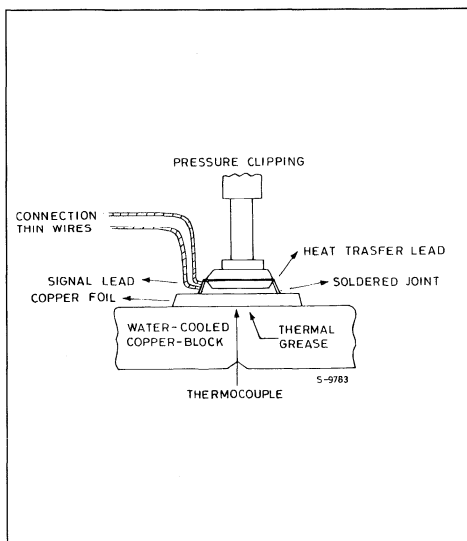
Measurement of junction to pin thermal resistance $R_{th(j-p)}$ is performed by holding the package (with the heat transfer leads soldered on a copper plate) against a water cooled heat sink, according with fig. 2. A thermocouple placed in contact with the plate measures the reference temperature.

For junction to ambient thermal resistance $R_{th(j-a)}$ the samples are suspended horizontally in a one cubic foot box, to prevent drafts.

The effect of "on board" external heat sinks is shown in fig. 1 is quantified, using a test board which has two $4 \times 4 \text{ cm}^2$ dissipating areas, one of each side of the package. These areas mechanically reduced in order to study the effect of their size on thermal performance.

The measurement circuit shown in fig. A3 is used for all the thermal evaluations.

Figure 2 : Measurement of $R_{th(j-p)}$.

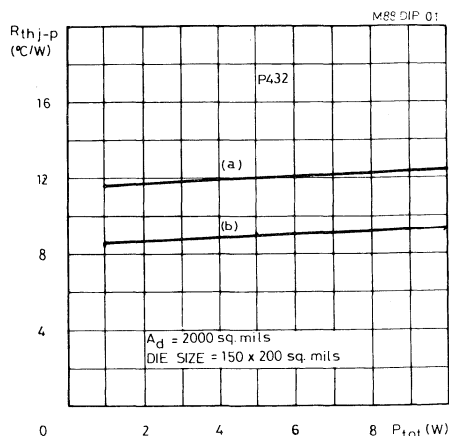


JUNCTION TO PIN THERMAL RESISTANCE

The dependance of $R_{th(j-p)}$ on the dissipated power is reported in fig. 3.

Some contribution to $R_{th(j-p)}$ is given by the silicon die.

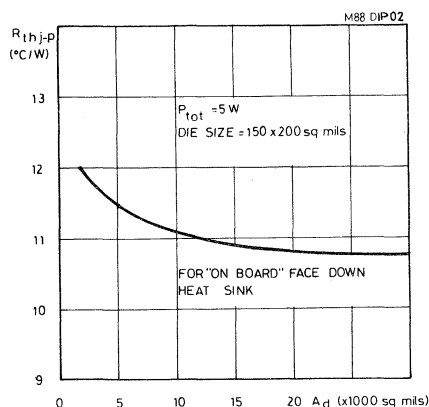
Figure 3 : $R_{th(j-p)}$ of (12+3+3) DIP vs. Power Level, for "on board" Face Up (a) and Face Down (b) Heatsink.



FOR DEVICES OTHER THAN THE TEST PATTERN P432 THE CALIBRATION CURVE OF FIG. 4 IS NEEDED.

It shows the relationship between $R_{th(j-p)}$ and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

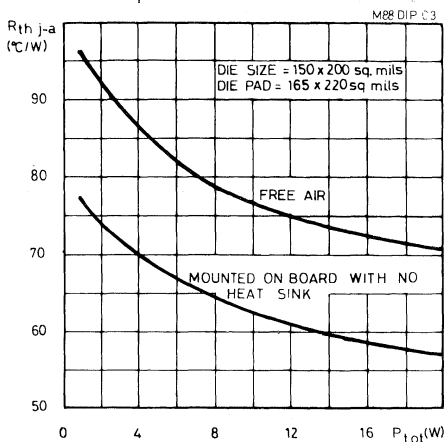
Figure 4 : $R_{th(j-p)}$ Thermal Resistance vs. Die Size and On Die Dissipating Area.



JUNCTION TO AMBIENT THERMAL RESISTANCE WITHOUT EXTERNAL HEATSINK

Fig. 5 gives the junction to ambient thermal resistance $R_{th(j-a)}$ of the package vs. dissipated power ; it evidences the effect of the board (which has NO dissipating area) in improving the exchange of the heat towards the ambient. The upper curve refers to samples suspended in air, with eight thin wire connecting the dissipating transistors and the sensing diode.

Figure 5 : $R_{th(j-a)}$ of DIP (12+3+3) Package vs. Dissipated Power.



THERMAL RESISTANCE WITH "ON BOARD" HEAT SINK

The effect of on-board heat sinks with different size and height, referred to a total "on board" dissipating area is summarized in fig. 6 : thermal resistance is given vs the side l of the two 35μ thick copper squares, obtained in the lower side of the test board and dedicated to heat dissipation.

TRANSIENT THERMAL RESISTANCE

The effect of single pulses of different length and height, referred to a total "on board" dissipating area of 6cm^2 (which is a good compromise between performance and cost) is shown in fig. 7.

Due to a significant thermal capacitance ($C = 0.7\text{J}/^\circ\text{C}$) and a correspondingly long risetime ($\tau = 30\text{s}$), single pulses up to 8W can be delivered to the system for 1s with acceptable junction temperature increase.

Figure 6 : R_{th} with two "on board" Square Heat Sinks vs. Side l .

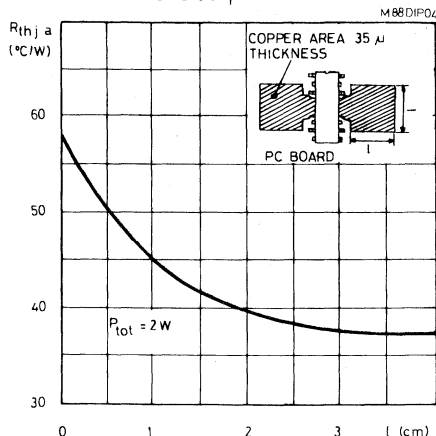
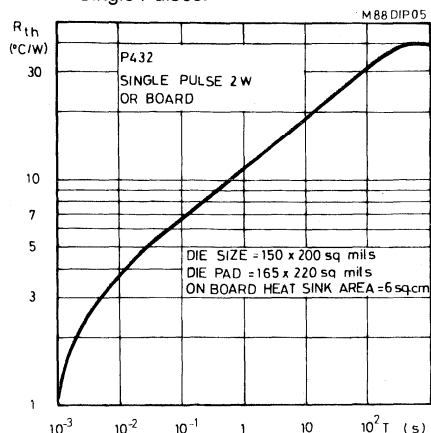


Figure 7 : Transient Thermal Resistance for Single Pulses.



Repetition of pulses with defined P_d , period and duty cycle DC (ratio between pulse length and signal period), is discussed in Appendix B. Junction temperature oscillates about the average value as qualitatively shown in fig. B3.

The transient thermal resistance corresponding to the upper limit of the curve of fig. B3 (peak transient thermal resistance) is reported in fig. 8 and depends on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

Figure 8 : Peak Transient R_{th} vs. Pulse Width and Duty Cycle.

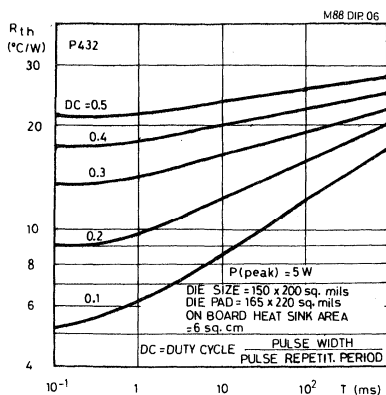
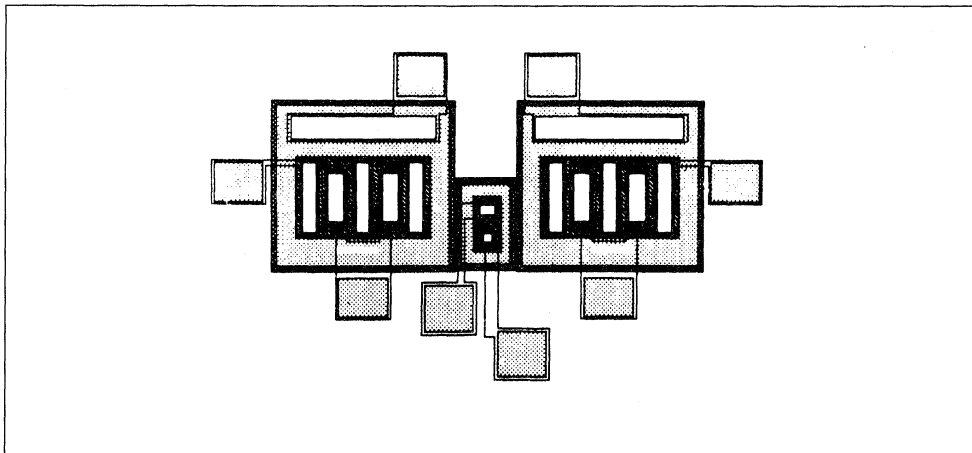


Figure A1 : Test Pattern P432 Lay-out.

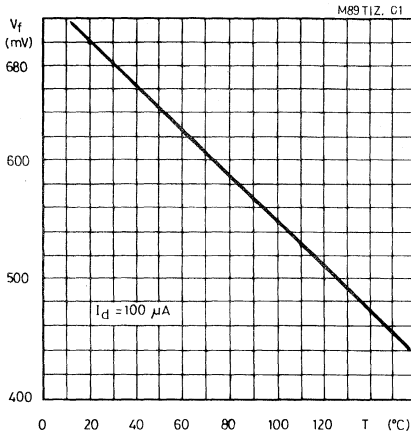
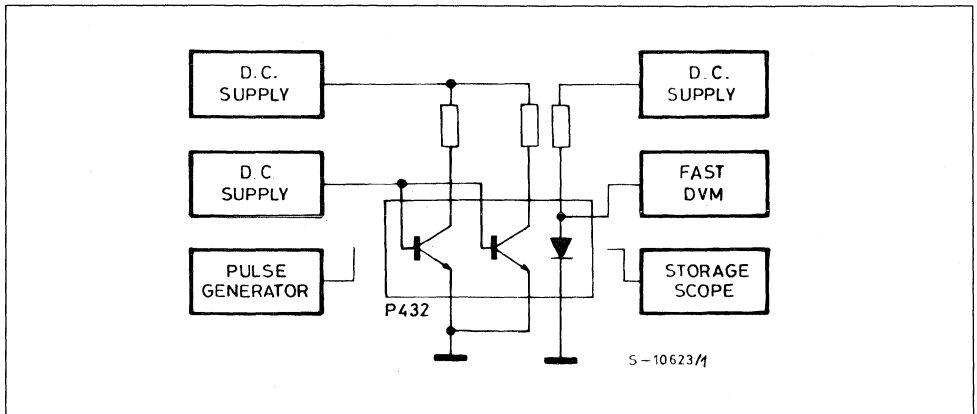


APPENDIX A - MEASUREMENT METHOD

The thermal resistance evaluation is performed with the especially designed test chip P432 which has two bipolar power transistor and one sensing diode (fig A1). The active area is about 2000 mils² on a 3000 mils² chip. Its lay-out was optimized in order to have a uniform temperature area, once the two transistors are powered ; the sensing diode is placed at the center of this area.

The relationship between the forward voltage V_f of the diode at a constant current of 100 μ A and the temperature is shown in fig. A2. The curve calibrates the junction temperature through the voltage drop of the diode.

The measurement circuit is shown in fig. A3. A storage oscilloscope or a fast digital voltmeter can be used for recording the V_f value..

Figure A2 : Calibration Curve (sensing diode).**Figure A3 : Measurement Circuit.**

APPENDINX B - THERMAL MANAGEMENT IN PULSED CONDITION

THERMAL RESISTANCE AND CAPACITANCE

The electrical equivalent of heat dissipation, for a thermal module formed by the active device with its package and the external heat sink is shown in fig. B1.

To each cell of the thermal chain are associated a value of thermal resistance R_{th} (°C/W) and a value of thermal capacitance C_{th} (J/°C). The former informs about temperature increase due to the element represented by the cell ; as, in the example

under consideration, heat transfer is mainly based on conduction for the silicon, the copper integrated heat sink and to metallic body of the external heat sink R_{th} can be calculated from the relationship :

$$R_{th} = \frac{\phi}{K \times S}$$

where K is the thermal conductivity of the material, ϕ the length of the conductive path and S its section.

Thermal capacitance C_{th} is the capability of heat accumulation ; it depends on the specific heat of the material and on the volume effectively interested by

heat exchange (this means that the parts which are not heated during heat dissipation DO NOT contribute to thermal capacitance). Thermal capacitance is given by :

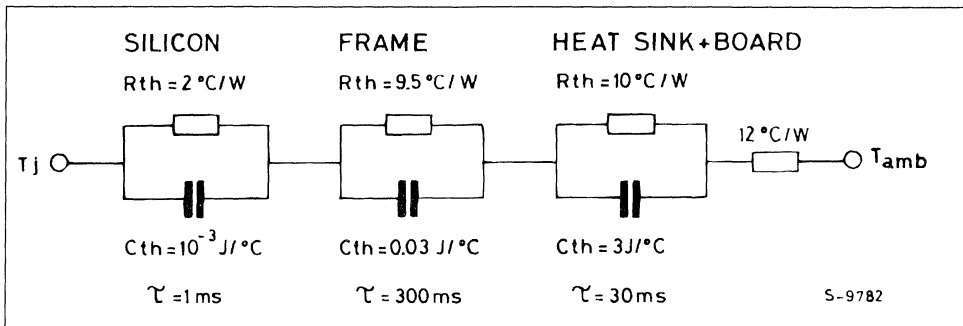
$$C_{th} = d \times c_t \times V$$

where d is the density of the material, c_t its specific

heat and V the volume interested to heat accumulation.

The last element of the network, assumed as purely resistive, is due to convection and radiation from the external heatsink towards the ambient.

Figure B1 : Electrical Equivalent of DIP (12+3+3) Package Mounted on the External Heatsink.



Each cell has its own risetime τ , given by the product of the thermal resistance and capacitance :

$$\tau = R_{th} \times C_{th}$$

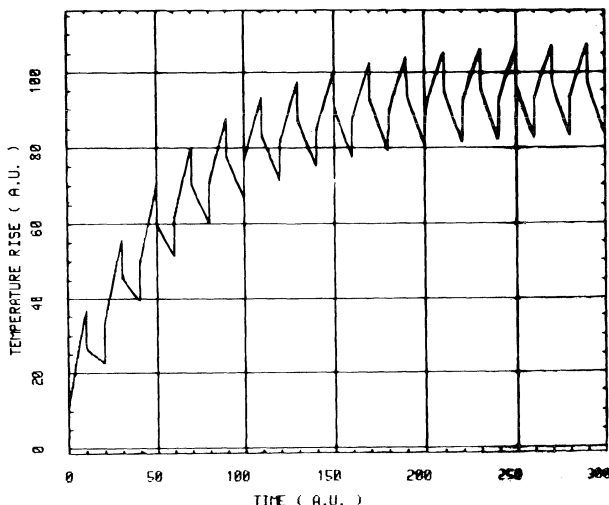
The value of the time constant determines whether a cell approaches equilibrium rapidly or slowly : if R_{th} or C_{th} increases, equilibrium is reached at a slower rate. The following relationship is valid for each cell :

$$\Delta T = R_{th} \times P_d \times [1 - e^{-t/\tau}]$$

Typical values of R_{th} , C_{th} and τ for DIP (12+3+3) application are shown in fig. B1.

When power is switched on, temperature increase is ruled by subsequent charging of thermal capacitance while the value reached in the steady state depends on thermal resistance only. Qualitative behaviour of the network of fig. B1 is shown in fig. B2.

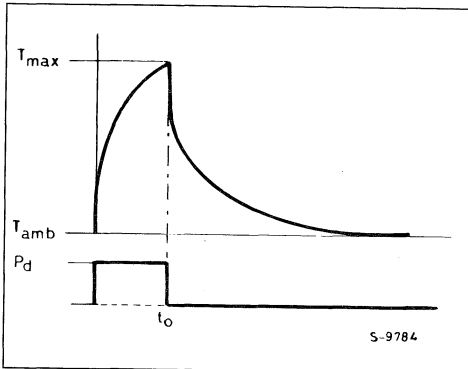
Figure B2 : Qualitative T_j Increase for Repeated Power Pulse.



SINGLE POWER PULSE

When the pulse length has an assigned value, effective T_j can be significantly lower than steady state T_j (fig. B3.)

Figure B3 : Effect of a Single Power Pulse.

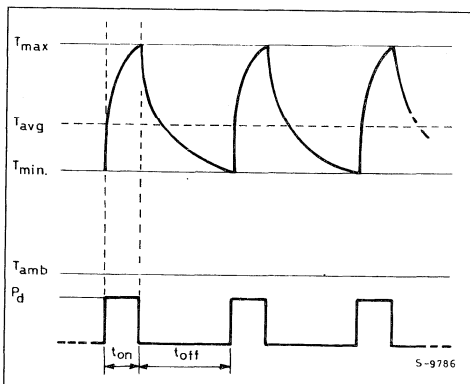


For any pulse length t_o , a transient thermal resistance $R_{th}(t_o)$ is defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power. Obviously, for shorter pulses, $R_{th}(t_o)$ is lower and a higher power can be dissipated, without exceeding the maximum junction temperature T_{jmax} allowed to the IC from reliability considerations. Fig. 6 of this Application Note gives experimental values of $R_{th}(t_o)$.

REPEATED PULSES

When pulses of the same height P_d are repeated with a defined duty cycle DC and pulse length is short in comparison with the total risetime of the system (many tens of seconds) the train of pulses is

Figure B4 : Junction Temperature Increase for Operated Pulses.



seen by the system as a continuous source, at a mean power level of

$$P_{davg} = P_d \times DC$$

The average temperature increase is :

$$\Delta T_{avg} = R_{th} \times P_{davg} = R_{th} \times P_d \times DC$$

On the other hand, the silicon die ($t_{si} = 1-2ms$) is able to follow frequencies of some KHz and junction temperature oscillates about the average, as qualitatively shown in fig. B4.

The thermal resistance corresponding to the peak of the oscillation at equilibrium (peak thermal resistance R_{thpeak}) is now given by fig. 8, and can be obtained if pulse length and duty cycle are known ; P_{dmax} is derived from the same figure.

APPENDIX C - APPLICATION EXAMPLES

EXAMPLE 1 - MAXIMUM P_d FOR SINGLE PULSE OF ASSIGNED LENGTH

PROBLEM : define the maximum P_d for a single pulse with a length of 20ms in the case of DIP (12+3+3) package used with heat sink of $6cm^2$. Ambient temperature is $50^\circ C$; maximum temperature is $50^\circ C$; maximum temperature is $130^\circ C$. Die size is $30K\text{ mils}^2$, with a dissipation area of $2K\text{ mils}^2$ (as in P432 test pattern).

SOLUTION : allowed temperature increase ΔT is $80^\circ C$. Having a $R_{th(j-a)}$ of $39^\circ C/W$, the system can dissipate about 2W in steady state. From fig. 7 the transient thermal resistance corresponding to one single pulse of 20ms is $R_{th}(20ms)_{P432} = 5^\circ C/W$. A peak of $80/5 = 16W$ can be applied to the circuit.

EXAMPLE 2 - R_{th} WITH REPEATED PULSES

PROBLEM : find the peak power which can be dissipated by the system of example 1 without heatsink, when power is continuously switched on 10ms and switched off 90ms. Ambient temperature is $50^\circ C$, maximum temperature is allowed to be $125^\circ C$.

SOLUTION : a maximum $\Delta T = 75^\circ C$ has to be considered. Fig. 8 indicated that for a pulse width of 10ms and a duty cycle of 0.1, R_{thpeak} is $8.5^\circ C/W$. Maximum P_d is $75/8.5W$, with an average temperature increase ΔT_{avg} of $40 \times 0.1 \times 8.8 \approx 36^\circ C$.

ALTERNATIVE TO THE DIP (12+3+3)

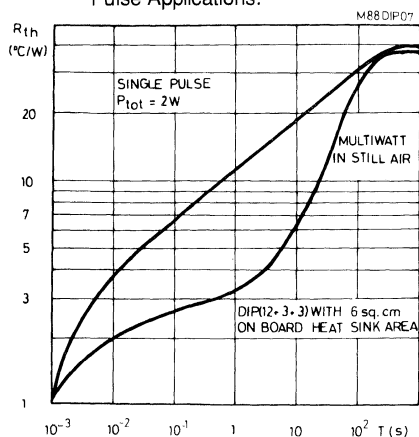
A cost effective application of DIP (12+3+3) for the dissipation of 1.5-2W is given by an "on board" heat sink of $6-7cm^2$. Thermal resistance is about $40^\circ C/W$ in DC condition. A comparison with Multiwatt® package in pulsed condition is summarized in fig. C1 and fig. C2.

It can be concluded that, due to its larger thermal mass, the Multiwatt® package is more suitable for the management of high power pulses.

Figure C1 : Thermal Resistance ($^{\circ}\text{C}/\text{W}$) of DIP (12+3+3) and Multiwatt Packages in Different Applications.

Case Examples	DIP (12+3+3) + 6cm ² on Board	Multiwatt® in Still Air
$R_{th(j-a)}$	40	39
Single Pulse		
$t_{on} = 20\text{ms}$	4.5	2.2
$t_{on} = 1\text{s}$	12	3.2
Repeated Pulse		
$t_{on} = 20\text{ms}$, $t_{off} = 180\text{ms}$	9.5	7.0
$t_{on} = 1\text{s}$, $t_{off} = 9\text{s}$	17	9.5

Figure C2 : Comparison Between DIP (12+3+3) and Multiwatt Packages in Single Pulse Applications.



RESISTANCE TO SOLDERING HEAT AND THERMAL CHARACTERISTICS OF PLASTIC SMDs

By C. Cognetti, E. Stroppolo and R. Tiziani

INTRODUCTION

Surface Mount Technology (SMT) has introduced a number of new technical problems, which have delayed the conversion from insertion assembly.

This is not strange : what readily available source of expertise existed a few years ago ?

Plastic SO packages were introduced in Europe in the early '70s and widely used in hybrids, but hybrid assembly has little relationship with the placement, soldering, handling tools now considered for SM PCB production. Was it surprising that even the semiconductor suppliers with sound experience in SO production could not give all of the answers needed by the PCB manufacturer ?

Japanese experience in SMT based consumer products is impressive : 87% of components used for cameras are in SM versions. However, the degree of complexity and performance of consumer products are somewhat different from the industrial, automotive and telecoms applications the Western world is interested in. On the other hand, in 1985 the percentage of SMDs (active and passive) used in industrial systems produced in Japan was 16.6% in telephones, 5.5% in automotive applications, 5.1% in cable communication, 0.7% in minicomputers¹ ; that is, a level similar to US and European production, presumably with a similar level of expertise.

In the past few years confidence in SMT has increased. More experience exists, which is the result of an expensive learning phase covered by both SMD manufacturers and users.

The reliability of plastic SMDs has an important place in this work. It needs a new approach in comparison with equivalent insertion devices, due to the completely different use.

In 14 years of production, no distinction was made in the authors' company between SO and DIP, from the point of view of reliability. They had the same reliability targets and similar evaluation methodology ; the former was often hot plate soldered on leaded ceramics for more convenient handling but no difference in long-term reliability existed.

With SMT, this is inadequate. Negative effects due to the various assembly processes, and to some

thermomechanical influence of the board, can limit the device life.

The present work is focused on SMDs soldered onto a plastic substrate, by means of the most common industrial processes, and takes into account two aspects of reliability :

1. Resistance to soldering heat, i.e., the suitability to withstand the thermal shock associated with the soldering cycle, without reducing reliability. This information is obtained by performing moisture resistance tests. Data about SO packages will be presented. For PLCCs, evaluation is in progress and will be concluded in the first half of 1988.
2. Heat dissipation, which influences the failure rate. This information is obtained with test patterns and test boards designed by SGS-THOMSON Microelectronics and includes thermal impedance in pulsed conditions. A few case studies will be included in this paper but complete characterizations are available elsewhere.²

RESISTANCE TO SOLDERING HEAT

In through-hole technology, devices are inserted from the upper side of the board and wave soldered from its lower side.

Only the lead extremities reach the temperature (250-260°C) of the molten solder ; the maximum specified soldering time of 10s is short enough to avoid over-heating of the package body, which generally does not exceed 120-130°C during the whole process.

This temperature is lower than the moulding compound glass transition temperature (160-170°C) and the risk of permanent damage to the package structure or to the silicon die is excluded.

Device reliability is defined almost independently of the soldering time and temperature ; devices under reliability test are mounted on sockets, thus neglecting the effect of the assembly process.

On the contrary, in all industrial SMT processes, devices are soldered in a high temperature ambient (215-260°C), with high heating rate, and the plastic package is kept in glass transition conditions

(figure 1) for a relatively long time (up to 60s). This situation was never encountered before.

Concern over reduced reliability is justified and explains the trend towards defining SMD reliability after the soldering cycle, in order to include the effects summarised in table 1.

Figure 1 : Thermal Expansion of Moulding Compounds, Compared with the Temperature of Different Soldering Techniques.

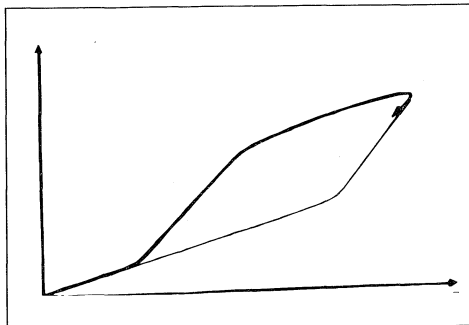


Table 1 : Factors Affecting SMD Reliability on Printed Board.

SMD Package	
Design and Structure	Volume and Thermal Inertia
Internal Contamination	Water Content
Thermomechanical Properties	Lead Solderability
Assembly Process	
Soldering Method	Contamination Level (flux)
Soldering Time/temperature	Rinsing
Substrate	
Thermomechanical Properties	Thermal Dissipation

EXPERIMENTAL

Reliability tests are performed on parts soldered onto test boards (4.5 in. x 6.5 in. FR-4 substrates).

SM PCB1 test board can accept SO-8, 14, 16. It is pre-grooved, in order to be cut in 35 positions, having the lay-out shown in figure 2 ; the SMD footprints are electrically connected to through-holes, with a pitch of 100 mils and placed in two parallel rows, 600 mils apart. Commercial pins inserted in the through-holes give the possibility of using the same equipment needed by DIPs.

The soldering processes from table 2 were used for SO packaged bipolar Operational Amplifiers and C-Mos Standard Logic. In order to simulate a rework, the soldering cycle was repeated on a number of devices. Soldering is followed by the usual rinsing in water or Freon, with or without ultrasonics.

Figure 2 : SM PCB1 Test Board.

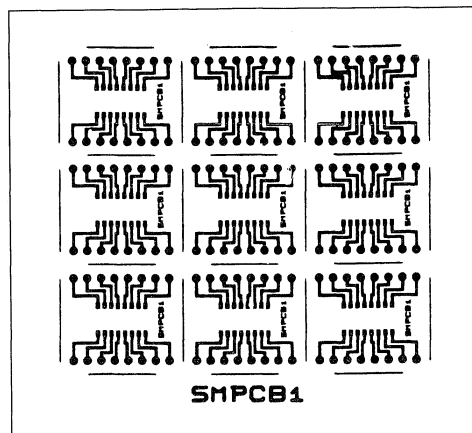


Table 2 : Soldering Processes Evaluated with SO Packaged Devices.

	Pre-heating	Soldering	Number of Cycles
Double Wave	120°C/30s	225°C/4s	1
Double Wave	120°C/30s	250°C/4s	1
Double Wave	110°C/30s	250°C/3.4s	1, 2, 3, 4
Triple Wave	110°C/30s	260°C/3s	1, 2, 3
Vapour Phase		215°C/20s	1, 2
Infra-red	160°C/30s	> 210°C/60s	1

The reliability evaluation was performed by means of the following tests :

Operating Life	150°C
Pressure Pot	121°C/2atm
THB	85°C/85% RH
	15V (bips)
	6V (CMos)
HAST	130°C/85% RH
	15V (bips)
	6V (CMos)
Thermal Cycles	- 55/+ 150°C
	(30/5/30 min)
Thermal Shocks	- 55/+ 150°C
	(5/1/5 min liquid)

130°C/85%RH Highly Accelerated Steam Test (HAST) has an acceleration factor of about 18-20 (ref. 3) in comparison with 85°C/85%RH, and the concrete possibility of reaching wear-out exists with this test, after an acceptable time.

For PLCC packages a similar methodology is followed. At the time of writing, only partial data are available, which will not be included here.

EXPERIMENTAL RESULTS

Experimental results are summarised in tables 3-6.

Table 3 : Cumulative Reliability Data after Multiple Wave Soldering.

Test Vehicles : LM2904 (SO-8), LM2901 (SO-14) and M74HC74 (SO-14)		
Double Wave	225°C/4s	250°C/4s
Triple Wave	260°C/3s	
Operating Life 1000h	0/154	0/32
Pressure Pot 96h	0/104	0/62
THB 85°C/85%RH 1000h 2000h	1/105*	0/32 0/32
HAST 130°C/85%RH 100h 200h		0/64 0/64
Thermal Shocks 500	0/231	0/77
* Parametric Failure		

Table 4 : Reliability Data after Vapour Phase Reflow.

Test Vehicle : LM2901 (SO-14)		
	215°C/20s	215°C/40s
Operating Life 1000h		0/32
Pressure Pot 96h		0/32
THB 85°C/85%RH 1000h 2000h		0/32 0/32
HAST 130°C/85%RH V = 15V 100h 200h 372h 458h 635h	0/56 0/56 0/24 2/24 5/22	0/12 0/12 1/12 1/11 3/10
Thermal Cycles 500		0/32
All failures due to pad corrosion		

Table 5 : Cumulative Reliability Data after Infra-red Reflow.

Test Vehicles : M74HC00 and M74HC74 (SO-14)	
	> 210°C/60s
Operating Life 1300h	0/34
THB 85°C/85%RH 1300h	0/34
HAST 130°C/85%RH 100h 200h 500h 672h	0/32 0/32 0/32 0/32
Thermal Cycles 750	0/70

Table 6 : Cumulative Reliability Data in Multiple Wave Soldering with Repetition of the Soldering Cycle.

Test Vehicles : LM2903 (SO-8), LM2901 and M74HC00 (SO-14)								
	Double Wave 250°C/3.4s				Triple Wave 260°C/3s			
Number of Cycles	1	2	3	4	1	2	3	
Pressure Pot 96h 504h		0/56 0/56						
100 Thermal Cycles (- 40/150°C) Followed by Pressure Pot 96h 168h 240h								
HAST 130°C/85%RH V = 6V 100h 500h 1000h 1150h 1300h	0/32	0/32	0/32 0/18 0/18 1/18 17/17	1/32* 0/18 0/18 1/18** 17/17**		0/30 0/30 0/30 0/30	0/60 0/30 0/60 0/60	
* Parametric Failure ** Pad Corrosion								

COMMENTS ON THE RELIABILITY RESULTS

Previous results do not reveal negative effects due to the exposure of SM devices to the soldering heat, for all of the industrial SMT soldering methods, in combination with the most common solders and cleaning solvents (Freon, water with and without ultrasonics).

Wear-out in the HAST test (130°C/85%RH) is between 1100 and 1300 hours when the soldering cycle is repeated up to 4 times with high temperature (250-260°C) multiple wave soldering, which is considered to transfer the highest thermal stress to the package body.

Pad corrosion is the final failure mechanism for all samples.

This performance is about 7-10 times better than the 2000-3000 h THB 85°C/85%RH, which is currently requested as qualification target in moisture resistance biased tests. Therefore, the reliability of surface mounted devices considered in this work is high enough to meet the most stringent requirements of the professional market.

No evidence of cracks in the plastic case was found in the previous evaluations. This effect (referred to also as 'pop corn' effect) is attributed to some anom-

alous thermal expansion of the package in the soldering phase, caused by water absorbed by the plastic encapsulation : a thermal treatment at a temperature higher than 100°C for a few hours is suggested in order to remove the absorbed water.⁴

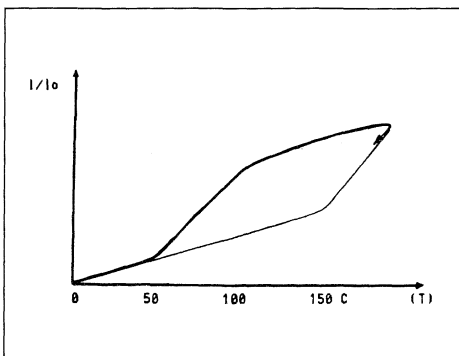
As this thermal pre-conditioning should be performed shortly before soldering, a serious problem arises in the assembly line. Such thermal annealing is not practical when the parts are supplied in plastic tapes or sticks : they should be removed from the packs by the user, heat treated, and packed again with additional costs and risks (co-planarity).

In this company's experience, the 'pop corn' effect can be completely avoided by controlling the frame-encapsulant interface, which is the easiest path for the water. Furthermore, experience has indicated that water at that interface does change the expansion characteristics of the package. About five years ago, the curve of figure 3 was found in some parts (coming from lots affected by the 'pop corn' problem) using Thermo-Mechanical Analysis (TMA). Devices under test were placed between the probes of the TMA transducer and their expansion characteristics recorded.

In the first ramp (5°C/min), package expansion was much higher than the moulding compound expansion between 50 and 100°C ; over 100°C, it returned on the curve typical of the encapsulant. Cooling down and repeating the measurement, only the lower curve of figure 3 was covered.

This behaviour was attributed to water having penetrated between the frame and the plastic body, whose expansion was responsible for the package deformation during the slow heating in TMA. When the parts were soldered on the substrate, cracks could occur due to the much faster heating rate.

Figure 3 : Thermal Expansion of SO Packages.



The problem was solved when the possibility of controlling the water content was found, by means of an improved frame design and some dedicated production steps.

Millions of parts assembled in recent years showed no evidence of the 'pop corn' effect, without any pre-conditioning before use.

The same solutions are successfully adopted for PLCC packages.

THERMAL CHARACTERISTICS

Correlation between reliability and junction temperature T_j is known :

the device lifetime is roughly halved when T_j is increased by 10°C.

Mainly due to this fact, thermal dissipation is a second factor which can influence SMD reliability : a reduced body means worse dissipation and higher power density on the board.

As careful thermal design is the key to improved reliability, a systematic characterisation of SM packages was performed, in order to study the main factors affecting thermal dissipation at both levels of package design and board design.

In the course of this work, the need for some critical revision of the way of producing and using thermal data was evident.

A point which cannot be under-evaluated is the choice of measurement method, as will be discussed later.

Another important point is the following : the common way of specifying the junction to ambient thermal resistance $R_{th(j-a)}$ is to associate one value of $R_{th(j-a)}$ to each device.

In the majority of data books, including this company's previous literature, little information is given on the experimental conditions used to obtain that value : the dissipated power and, above all, the kind of interconnection between the package and the measurement set-up (wires, socket or board), which in some cases can become a far from negligible heat transfer element.

Ignoring this contribution was probably justifiable with packages having a low thermal conductivity frame, such as Alloy 42 or Kovar.

For those packages, heat spreading was limited to the silicon die and to the die pad ; thermal dissipation was little affected by the surroundings and the measurement assembly had little influence on the final value of $R_{th(j-a)}$.

This is not the case concerning the same packages with a copper frame, introduced a few years ago to achieve a higher power capability ; due to better thermal conductivity of the leads they are much more sensitive to external dissipating media, eventually used for the measurement.

Similar statements are valid for SMDs and become more important on account of their reduced dimensions.

The concept is summarised in table 7, where the thermal resistance of some dual-in-line (DIP), Small Outline (SO) and Plastic Leaded Chip Carrier (PLCC) packages is given. The influence of the frame thermal conductivity is remarkable ; but likewise remarkable are the differences obtained for the same package, when it is connected by thin wires (and 'floating' in still air) or soldered on a PC board during the measurement.

Table 7 : Junction to Ambient Thermal Resistance (C/W) for DIP and SM Packages in Different Experimental Conditions.

	Power Pd[W]	'Floating' in Air	On SGS Test Board	Ratio
DIP 14 Leads (*)				
Alloy 42 0.25mm	0.5	156	138	1.13
Cu 0.25mm	0.6	125	90	1.39
SO-14 Leads (**)				
Alloy 42 0.25mm	0.4	280	195	1.43
Cu 0.25mm	0.6	190	105	1.80
PLCC-44 Leads (***)				
Cu 0.25mm	1.0	70	52	1.35
die size : (*) = 0.095 in. x 0.110 in. (**) = 0.060 in. x 0.090 in. (***) = 0.180 in. x 0.180 in.				

Especially for SO packages the influence of the substrate on thermal dissipation is noticeable. This fact can help to explain the following points :

1. The $R_{th}(j-a)$ values published by different SMD suppliers are distributed in too wide a range (more than 70°C/W for SO packages) which handicaps a correct thermal design. Most of the difference is probably due to different test boards, and the availability of standardised measurement methodology should help to give more accurate information.
2. The board lay-out contribution should be studied, in order to quantify the effect of device density : a suitable distance between two or more dissipating elements can be an effective solution for improved reliability.

3. Specification of thermal characteristics should include more elements (power level, board density, package design) which cannot be summarised in one single thermal resistance value, as was commonly the case with Alloy 42 DIPs.

A set of experimental curves was obtained for each SM package,² which gives the relationship between these factors ; if used to feed back the board design, they should help to achieve a better thermal performance.

The most significant results will be discussed here.

Moreover, two other factors will be considered.

1. The thermal capacitance of the package, which is significant especially in higher pin count PLCCs ; it delays T_j increase during power transients and is important in switching applications.
2. The frame design in association with a suitable board design ; a low resistance thermal path can be obtained with modified frames ; heat is then conveyed to copper areas obtained on the board and dissipated power can be increased to 2W with SOs and PLCCs.

EXPERIMENTAL METHOD

When thermal measurements on plastic packages are performed, the first consideration is the lack of a standard method : at present, only draft specifications⁵ exist, proposed in 1986 and not yet standardised.

The experimental method used in this company since 1984 has anticipated these preliminary recommendations to some extent, as it is based on the P432 thermal test pattern (figure 4) having two npn transistors, with 10W each power capability. A sensing diode is placed on the thermal plateau arising when the transistors are operating in parallel and gives the actual value of T_j , through the calibration curve of its forward voltage V_f (at constant current) vs temperature.

Transistor size, which is not fixed by the documents proposed for standardisation, was intentionally limited to 1000 mils², in order to simulate a high power density and characterise the worst case. Die size, which is found to have some influence on thermal resistance when copper frame is used, is slightly smaller than the die pad size and never exceeds 30000 mils² in larger packages, such as high pin count PLCCs.

The measurement set-up is shown in figure 5. It is compatible with DC and AC power supply and has an accuracy better than 5%.

The advantages offered by the test pattern are :

- (i) high power capability (wider evaluation range) ;
- (ii) repeatable electrical characteristics (V_f) and temperature coefficient (1.9mV/C) of the sensing element (accuracy) ;
- (iii) high resolution in pulsed conditions (evaluation down to 100s pulses) ;
- (iv) better correlation from one package to another.

Alloy 42 frames and copper frames were used for narrow SO packages (150 mils body) ; only copper frames were considered for the others : wide SO (300 mils body) and PLCC packages.

Suitable FR-4 test boards were developed, which will be described case by case.

Figure 4 : Test Pattern P432 Layout.

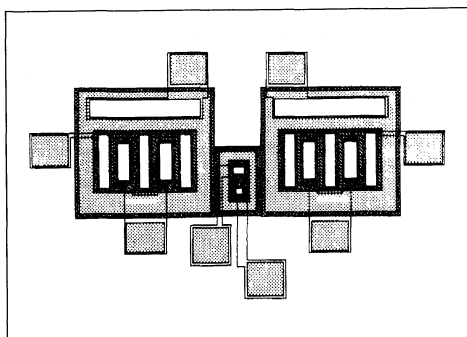
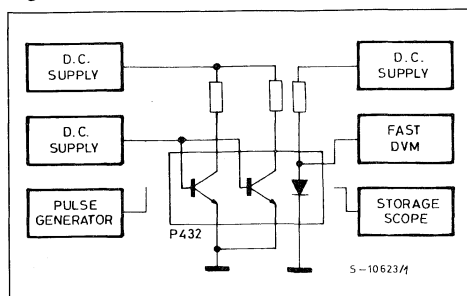


Figure 5 : Measurement System.



THERMAL CHARACTERISTICS IN DC CONDITIONS

Thermal characteristics of the SO-14 package in DC conditions are shown in figure 6.

The upper curve is related to samples floating in still air and connected to 8 thin wires needed for biasing the dissipating transistors and the sensing diode of the P432 test pattern.

Samples soldered on the FR-4 test board shown in figure 2 have an approximately halved thermal resistance ; by reducing the copper pattern length of the test board, different component densities are simulated : thermal resistance is increased by about 30% when the track length has the minimum value.

Dependence of the thermal resistance on the total area of the traces connected to the package is represented by the curve of figure 7. It quantifies the effectiveness of the board lay-out to spread the heat and dissipate it towards the ambient and can be conveniently used for determining the thermal resistance value associated with a given board design.

Figure 6 : $R_{th(j-a)}$ of SO-14 Package vs. Power Level.

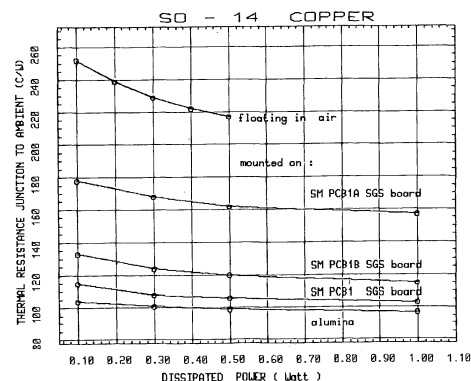


Figure 7 : $R_{th(j-a)}$ of SO-14 vs. on Board Trace Area.

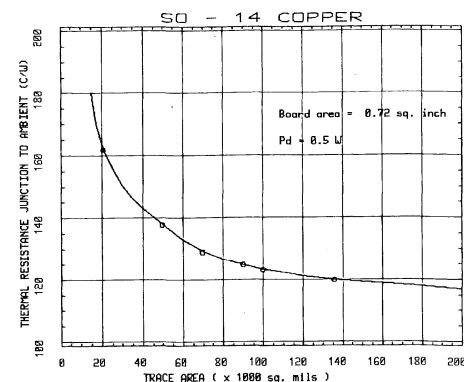
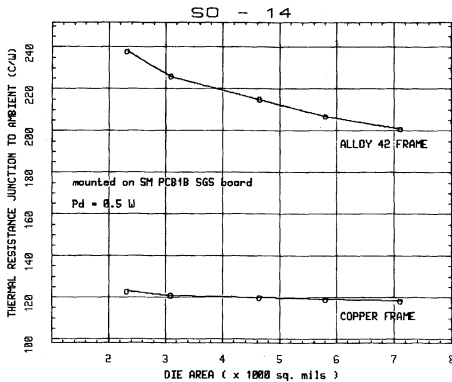


Figure 8 : Rth(j-a) of SO-14 with Copper (SGS-THOMSON) and Alloy 42 Frame.



Comparison of low conductivity (Alloy 42) and high conductivity (copper) frames is shown in figure 8.

The data obtained for the different SM packages are summarised in table 8 ; the two thermal resistance values refer to the two extreme cases of a low density and a high density board.

Table 8 : Summary of Junction to Ambient Thermal Resistance in Steady State Power Dissipation (SGS-THOMSON test boards)

	Die Pad Size (milinches)	Power Pd [W]	Rth(j-a) [°C/W] on Board
SO-8 Alloy 42	90 x 100	0.2	250-310
Copper	95 x 100	0.2	160-210
SO-14 Alloy 42	98 x 118	0.3	200-240
Copper	78 x 118	0.5	120-160
Copper	98 x 125	0.7	105-145
SO-16 Alloy 42	98 x 118	0.3	180-215
Copper	94 x 185	0.5	95-135
SO-16W Copper	120 x 160	0.7	90-112
SO-20 Copper	140 x 220	0.7	77-97
PLCC-20 Cu	180 x 180	0.7	90-110
PLCC-44 Cu	260 x 260	1.5	50-60
PLCC-68 Cu	425 x 425	1.5	40-46
PLCC-84 Cu	450 x 450	2.0	36-41

Rth(j-a) values correspond to low and high board density

THERMAL IMPEDANCE IN PULSED CONDITIONS

The electrical equivalent of heat dissipation for a module formed by the active device, its package, the board and the external ambient is a chain of RC cells each having a characteristic risetime $\tau = RC$.

Thermal capacitance is the capability of heat accumulation and depends on the heat capacitance of the materials, their volume and their density.

When the power is switched on, the junction temperature after a time t is the result of the subsequent charge of the RC cells, according to the well known exponential relationship :

$$\Delta T_j = R_{th} \times P_d \times (1 - e^{-t/\tau})$$

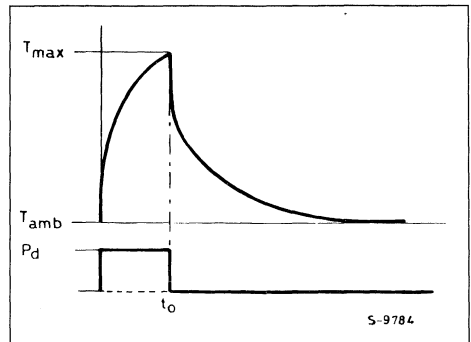
When the pulse length t_0 is an assigned value, effective T_j can be significantly lower than the steady state T_j (figure 9) and a transient thermal resistance $R_{th}(t_0)$ can be defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power.

Obviously, for shorter pulses, transient thermal resistance is lower and a higher power can be dissipated without exceeding the maximum junction temperature defined in reliability considerations.

In a similar way, when pulses of the same height P_d are repeated with a defined duty cycle DC and the pulse is short in comparison with the total risetime of the system, the train of pulses is seen as continuous source at a mean power level :

$$P_{d_{avg}} = P_d \times DC$$

Figure 9 : Qualitative T_j Increase for Single Power Pulse.



APPLICATION NOTE

On the other hand, the silicon die has a risetime of 1-2ms and is able to follow frequencies of some kHz : junction temperature oscillates about the average value :

$$\Delta T_{javg} = R_{th} \times P_{davg}$$

as qualitatively shown in figure 10.

The thermal resistance corresponding to the peak of the oscillation at the equilibrium (peak thermal resistance) gives information on the maximum temperature reached by the device and, depending on DC and pulse width, can be much lower than DC thermal resistance.

Figure 10 : Qualitative T_j Increase for Repeated Power Pulse.

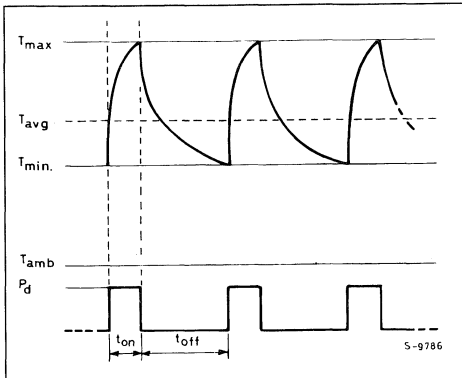
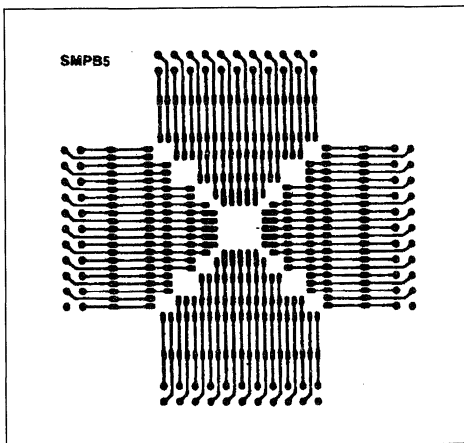
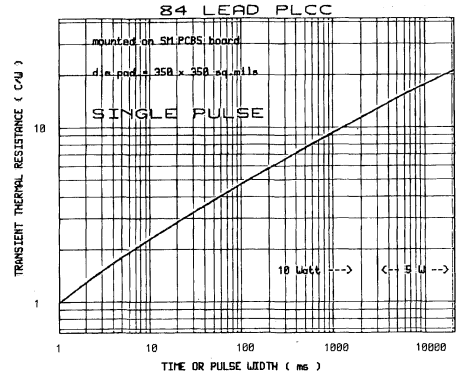


Figure 11 : Test Board for PLCC.



The knowledge of thermal characteristics in the AC condition is a valid tool to reduce redundancy (and cost) in the thermal design of pulsed applications.

Figure 12 : Transient Thermal Resistance for PLCC-84 on Board.



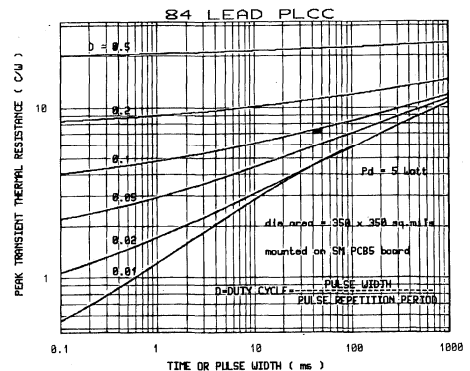
The example is now given of a high pin count PLCC, which has a large thermal capacitance, due to its volume and weight.

Temperature increase for 84 lead PLCCs soldered on the SMPB5 test board (figure 11) for single pulses of different length is given in figure 12. A rise-time of 50-60s is typical for this package, having a thermal resistance of 38°C/W in steady state (see table 8).

For single pulses, the effective thermal resistance is much reduced and acceptable junction temperature is observed even for high power pulses. 10W can be delivered for about 1s (9°C/W) and 5W for 10s (18°C/W).

Peak thermal resistance for repeated pulses, with different duty cycles, is represented in figure 13 and the above considerations are valid in this case also.

Figure 13 : Peak Transient R_{th} for PLCC-84 on The Board.



MEDIUM POWER APPLICATION

The lack of power packages suitable for SMT requirements (standard outline, automatic handling) is known.

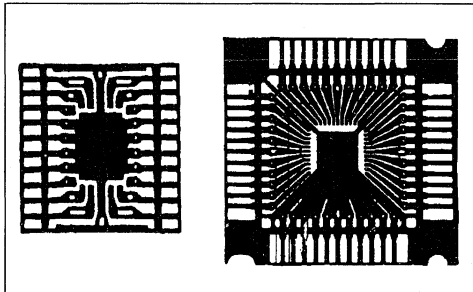
A simple way to achieve power dissipation in the medium range (1-2W) is to transform the available signal packages and modify their frame to obtain a high conduction path.

In figure 14 the frame of medium power SO and PLCC packages is shown : some leads are connected to the die pad, in order to have a low junction-to-pin thermal resistance $R_{th(j-p)}$. Typical values of this parameter are in the range of 12-15°C/W, with a high conductivity lead frame.

Modification involves the internal part of the frame only, while the external dimensions of the package are not changed ; the solution offers the undoubted advantage of being compatible with existing handling and testing tools.

The heat produced by the IC, and conveyed externally by the heat transfer leads, can be cost effectively transferred to the ambient by means of dedicated copper heatsinks, integrated on the board.

Figure 14 : Medium Power SO and PLCC Frame.



In figure 15, the layout of test boards used for the thermal characterisation of medium power SO-20s (with 8 heat transfer leads) and PLCC-44s (with 11 heat transfer leads) is represented.

The area of the integrated heatsink can be optimised for cost reduction, depending on the dissipation level. In figure 16 the relationship between the $R_{th(j-a)}$ of the PLCC-44s and the total dissipating area is given.

It can be noticed that, with 6-7 sq cm of substrate, the thermal resistance of PLCC-44s can be decreased from 55°C/W to 40°C/W, for 1.5-2W dissipation.

A similar performance is possible with the medium power SOs.

Figure 15 : Test Boards for Medium Power SO-20 and PLCC-44 Package.

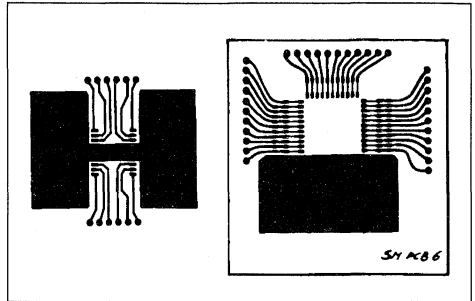
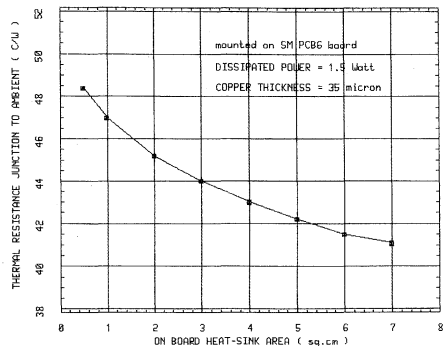


Figure 16 : $R_{th(j-a)}$ of Medium Power PLCC-44 vs. Dissipating Area on Board.



CONCLUSIONS

In SMT, two main reliability related concerns are resistance to soldering heat and heat dissipation.

RESISTANCE TO SOLDERING HEAT

After extensive evaluation of devices soldered on plastic substrates by means of the three industrial soldering methods (multiple wave soldering, vapour phase and IR reflow), no reliability degradation was found.

The following soldering conditions are possible with SO packaged devices :

- Multiple Wave : $T = 250 - 260^{\circ}\text{C}/t = 4\text{s}$ (repetition allowed)
- Vapour Phase : $T = 215^{\circ}\text{C}/t = 20\text{s}$ (repetition allowed)
- Infra-red : $T > 210^{\circ}\text{C}/t = 60\text{s}$ ($T_{\text{max}} = 225^{\circ}\text{C}$)

No crack in the plastic case was evidenced during the above work or in the field, in recent years of production, and no thermal preconditioning was needed. However, this result was obtained after optimisation of the frame design and of the production process. Its extension to the totality of the products existing on the market might be too arbitrary, but it is possible to conclude that the structure of SM packages, when associated with suitable materials and processes, is able to meet the user's requirements. A similar evaluation is running for PLCC packages and will be completed in the first half of 1988.

HEAT DISSIPATION

Some considerations have been made about the consequence of the lack of some standard evaluation methodology. To standardise test chips and test boards is very important, in order to reach a better knowledge and a better information exchange.

By means of an internally developed test pattern and suitable test boards, three points have been studied :

1. The influence of the substrate on thermal dissipation, whose effect has to be taken into account much more than for insertion packages. With a proper layout it is effective in reducing thermal resistance. For example, dissipation of copper

frame SO package can become better than the equivalent Alloy 42 DIP and only 10-20% higher than the equivalent copper DIP.

2. The thermal impedance, whose value is much more suitable for the thermal design of switching applications and can contribute to reduce the cost of the system.
3. The new medium power SO and PLCC packages, which offer the possibility of cost-effective power dissipation in the range of 1.5-2W, still maintaining a standard outline.

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4. Fukuzawa, I. et al, 'Moisture Resistance Degradation of Plastic LSI by Reflow Soldering', Proceedings IRPS, p. 192 (1985).
5. SEMI Draft Specifications 1377 and 1449 (1986).

HANDLING AND MOUNTING ICs IN PLASTIC POWER PACKAGES

Integrated circuits mounted in plastic power packages can be damaged, or reliability compromised, by inappropriate handling and mounting techniques. Avoiding these problems is simple if you follow the suggestions in this section.

Advances in power package design have made it possible to replace metal packages with more economical plastic packages in many high power applications. Most of SGS-THOMSON Microelectronics power driver circuits, for example, are mounted in the innovative MULTIWATT® package, developed originally for high power audio amplifiers. Though the intrinsic reliability of these packages is now excellent the use of inappropriate techniques or unsuitable tools during mechanical handling can affect the long term reliability of the device, or even damage it. With a few simple precautions, careful designers and production engineers can eliminate these risks, saving both time and money.

BENDING AND CUTTING LEADS

The first danger area is bending and cutting the leads. In these processes it is important to avoid

straining the package and particularly the area where the leads enter the encapsulating resin. If the package/lead interface is strained the resistance to humidity and thermal stress are compromised, affecting reliability.

There are five basic rules to bear in mind :

- Clamp the leads firmly between the package and the bend/cut point (figure 1).
- Bend the leads at least 3mm from the package (figure 2a).
- Never bend the leads more than 90° and never bend more than once (figure 2b).
- Never bend the leads laterally (figure 2c).
- Make sure that the bending/cutting tool does not damage the leads.

Figure 1 : Clamp the Leads between the Package and Bend/cut Point.

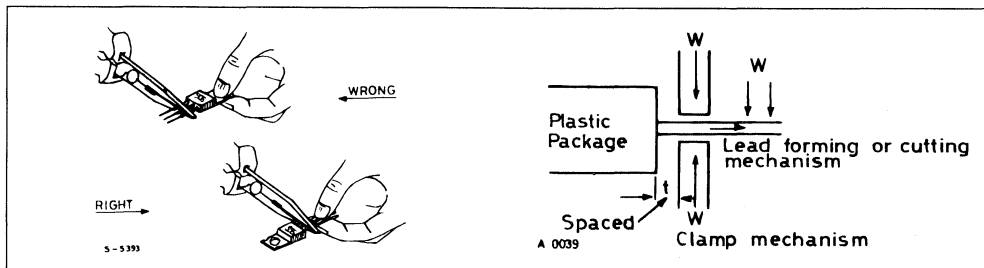
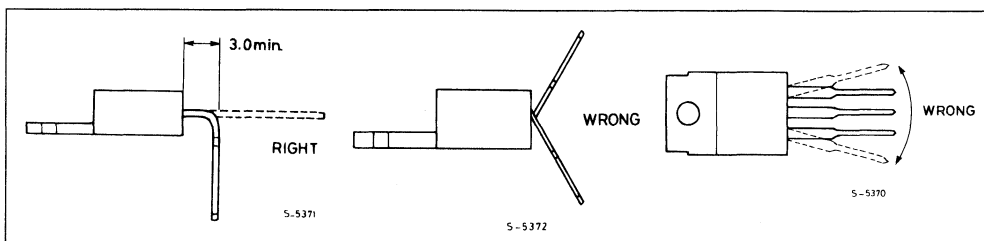


Figure 2 : Bend the Leads at Least 3mm. from the Package, never Bend Leads more than 90° and never Attempt to Splay the Leads Out.



INSERTION

When mounting the IC on a printed circuit board the golden rule is, again, to avoid stress. In particular :

- Adhere to the specified pin spacing of the device ; don't try to bend the leads to fit non-standard hole spacing.
- Leave a suitable space between the IC and the board. If necessary use a spacer.
- Take care to avoid straining the device after soldering. If a heatsink is used and it is mounted on the PC board it should be attached to the IC before soldering.

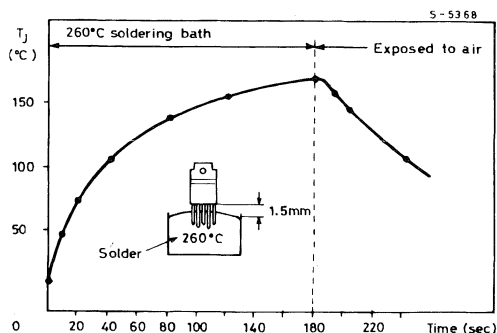
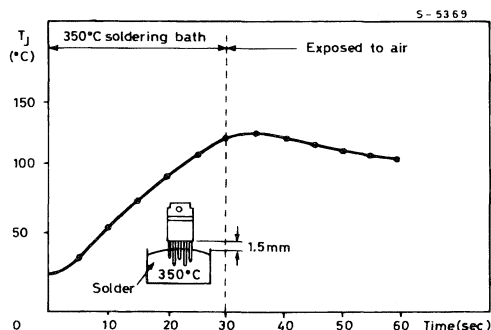
SOLDERING

The greater danger during soldering is overheating. If an IC is exposed to high temperature for an excessive period it may be damaged or reliability reduced.

Recommended soldering conditions are 260°C for ten seconds or 350°C for three seconds. Figure 3 shows the excess junction temperature of a PENTAWATT package for both methods.

It is also important to use suitable fluxes for the soldering baths to avoid deterioration of the leads or package resin. Residual flux between the leads or in contact with the resin must be removed to guarantee long term reliability. The solvent used to remove excess flux should be chosen with care. In particular, trichloroethylene ($\text{CHCl}_3 : \text{CCl}_2$) - base solvents should be avoided because the residue can corrode the encapsulant resin.

Figure 3 : The Excess Junction Temperature of a PENTAWATT Package in the suggested Soldering Conditions.



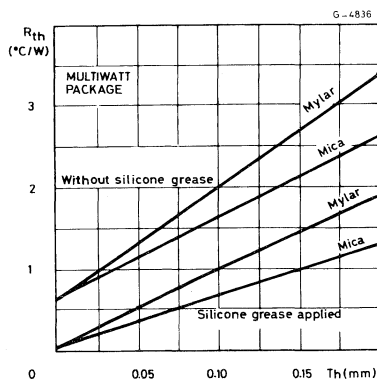
HEATSINK MOUNTING

To exploit the full capability of a power device a suitable heatsink must be used. The most important aspect from the point of view of reliability is that the heatsink is dimensioned to keep the junction temperature as low as possible. From a mechanical point of view, however, the heatsink must be designed so that it does not damage the IC. Care should also be taken in attaching the IC to the heatsink.

The contact thermal resistance between the device and the heatsink can be improved by adding a thin layer of silicon grease with sufficient fluidity to ensure uniform distribution. Figure 4 shows how the thermal resistance of a MULTIWATT package is improved by silicone grease.

An excessively thick layer or an excessively viscous silicon grease may have the opposite effect and could cause deformation of the tab.

Figure 4 : The Thermal Resistance of a MULTIWATT Package is improved by Silicon Grease. Here Thermal Resistance is plotted against Grease Thickness.



SGS-THOMSON plastic power packages - MULTI-WATT, PENTAWATT and VERSAWATT - are attached to the heatsink with a single screw. A spring clip may also be used as shown in figure 5. The screw should be properly tightened to ensure that the package makes good contact with the heatsink. It should not be too tight or the tab may be deformed, breaking the die or separating the resin from the tab.

The appropriate tightening torque can be found by plotting thermal resistance against torque as shown in figure 6.

Suggested tightening torques for 3MA screws are 8Kg/cm for VERSAWATT, PENTAWATT and MULTI-WATT packages. If different screws, or spring clips, are used the force exerted by the tab must be equivalent to the force produced with these recommended torques.

Even if the screw is not overtightened the tab can be deformed, with disastrous results. If the surface of the heatsink is not sufficiently flat. The planarity of the contact surface between device and heatsink must be better than 50µm for PENTAWATT and VERSAWATT packages and less than 40µm for MULTI-WATT packages.

Figure 5 : MULTI-WATT, PENTAWATT and VERSAWATT Packages are attached to the Heatsink with a Single Screw or a Spring Clip.

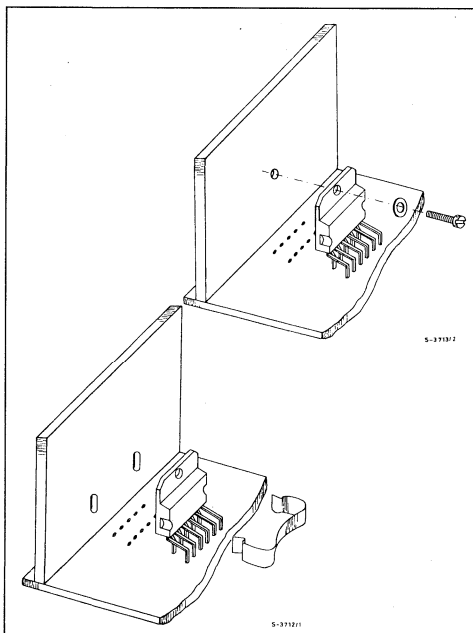


Figure 6 : Contact Thermal Resistance depends on Tightening Torque.

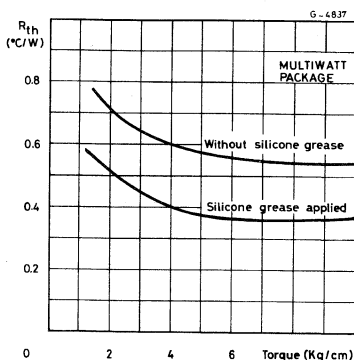
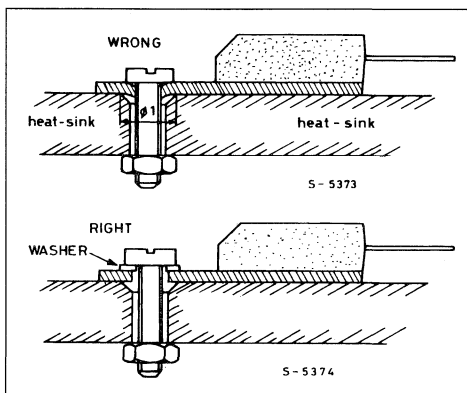


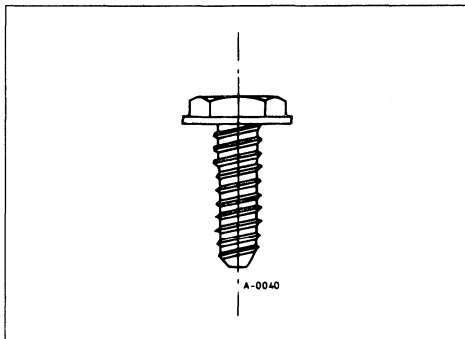
Figure 7 : The Heatsink Tab may be deformed if a Washer or a Wide-headed Screw is not used.



Similar problems may arise if the screwhead is too narrow compared to the hole in the heatsink (figure 7).

The solution here is to use a washer to distribute the pressure over a wider area. An alternative is to use screws of the type shown in figure 8 which have a wide flat head. When self-tapping screws are used it is also important to provide an outlet for the material deformed as the thread is formed. Poor contact will result if this is not done. Another possible hazard arises when the hole in the heatsink is formed with a punch: a circular depression may be formed around the hole, leading to deformation of the tab. This may be cured by using a washer or by modifying the punch.

Figure 8 : The recommended Screw Type Looks Like this.



Serious reliability problems can be encountered if the heatsink and printed circuit board are not rigidly connected. Either the heatsink must be rigidly attached to the printed circuit board or both must be securely attached to the chassis. If this is not done the stresses and strains induced by vibration will be applied to the device and in particular to the lead/resin interface. This problem is more likely to arise when large boards and large heatsinks are used or whenever the equipment is subjected to heavy vibrations.

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